STHS4257A, STHS4257A1
STHS4257L, STHS4257L1

IEEE 802.3af PoE Powered Device (PD) interface controller with integrated signature resistor

Features

- IEEE 802.3af-compliant interface for Powered Devices (PDs)
- Integrated 100V, 450mA power MOSFET low side switch
- Inrush current limit
- Normal operation current limit
- Integrated 25kΩ signature resistor
- Signature disable (STHS4257A1/L1)
- Resistor-programmable classification current (Class 0-4)
- Power Good output, open drain
- Undervoltage Lockout (UVLO)
- Thermal overload protection (two-step for the STHS4257A/L)
- Latch (L) or auto-retry (A) after repetitive thermal overload
- Industrial temperature range: –40 to +85°C
- SO8 and DFN8 (3mm x 3mm) packages
- RoHS compliant

SO8 (M)

DFN8 3mm x 3mm (DB)

Applications

- Voice over IP (VoIP) phones
- Web cameras
- WLAN access points
- Internet appliances
- POS terminals
- RFID readers

Table 1. Device options

Order code	Signature disable	UVLO threshold, rising (V)	UVLO threshold, falling (V)	Protection mode	Thermal overload protection	Inrush current limit (mA, typ)	Normal operation current limit (mA, typ)
STHS4257A		39.2	30.5	Auto	2 steps	350/188 (1)	
STHS4257A1	✔	36.0	30.5	Auto	1 step	140	375
STHS4257L		39.2	30.5	Latch	2 steps	350/188 (1)	
STHS4257L1	✔	36.0	30.5	Latch	1 step	140	375

1. Current limit is common for both modes and gets reduced only in case of thermal overload. See *Table 5: Electrical parameters*.

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1 Summary description

The STHS4257 is an IEEE802.3af-compliant family of interface controllers for Power over Ethernet (PoE) Powered Device (PD) applications. The devices consist of two main sections:

- The IEEE802.3af interface to the PoE powered RJ-45 wall socket, and
- the Hot Swap Controller (HSC) functions required to protect the PD during insertion, operation, and withdrawal from the RJ-45 socket.

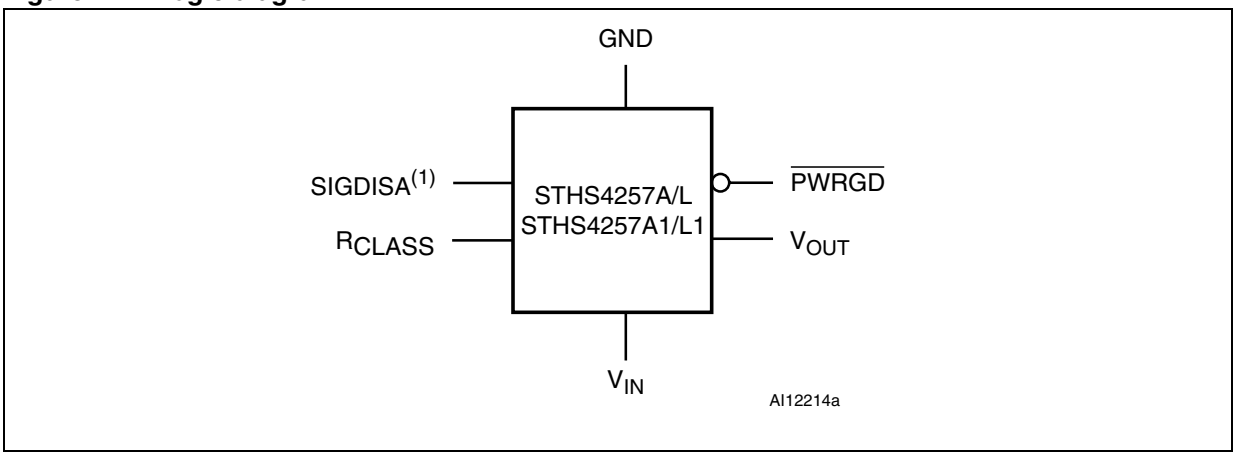
These devices have an integrated high voltage power MOSFET (low-side switch) with low R_{ON} and the capability to accept transients as high as 100V. Since the pins (such as GND and V_{IN}) which interface to the RJ-45 socket can routinely see high peak voltages in excess of 100V, it is strongly recommended that board designers protect the PD device with a transient voltage suppressor, such as the SMAJ58A (available from STMicroelectronics), connected between the GND and V_{IN} pins (see *Figure 4 on page 8*).

The IEEE802.3af-compliant interface includes the basic PD detection and Classification functions, whereas the 'Hot Swap' functions include other basic features, such as Inrush Current Limiting, Undervoltage Lockout (UVLO), and Thermal Overload Protection. All of the devices include an open drain Power Good ($\overline{PWRGD}$) signal to indicate normal steady operation (see *Figure 1 on page 6* and *Table 2 on page 6*). The STHS4257 family also incorporates a 1.5V voltage offset (two series diodes) to accommodate the input diode bridge used to make the PD polarity insensitive.

The STHS4257A1/L1 includes a dual level current limit circuit. This allows the STHS4257A1/L1 to interface with legacy Power over Ethernet (LAN) systems while maintaining compatibility with the current IEEE 802.3af specification.

Each of the two basic part types, the STHS4257A/L and the STHS4257A1/L1, is available either with Latched Operation (L) Mode or with Automatic Retry (A) Mode after fault conditions. For product options overview see *Table 1 on page 1*.

Figure 1. Logic diagram



1. STHS4257A1 and STHS4257L1 devices only.

Table 2. Signal names

Pin		Symbol	Description
STHS4257A/L	STHS4257A1/L1		
1, 3, 7	1, 3	NC	No Connect
2	2	R_{CLASS}	Classification pin
4	4	V_{IN}	Negative return power line to PSE
5	5	V_{OUT}	Power Output (negative rail)
6	6	$\overline{PWRGD}$	Power Good Output, open drain, active-low (referenced to V_{IN})
—	7	SIGDISA	Signature Disable Input, internally pulled to V_{IN}
8	8	GND	Positive Power Supply; common input/output power rail

Figure 2. Pin connections (STHS4257A/L, top view)

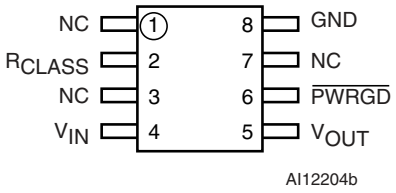
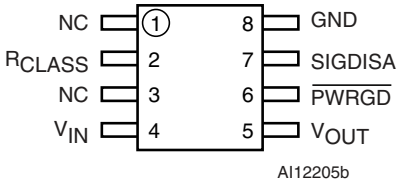


Figure 3. Pin connections (STHS4257A1/L1, top view)



1.1 Pin descriptions

1.1.1 Classification (R_{CLASS})

This is the Classification pin. Connect a Classification resistor between this pin and V_{IN} to tell the PSE which power class will be connected. Leave it open for Class 0.

Note: Do not connect this pin directly to V_{IN}. For power classes and R_{CLASS} resistor values, see *Table 3*.

1.1.2 V_{IN}

This is negative return power line to PSE.

1.1.3 Power supply (GND)

This is the Power Input/Output, positive rail.

1.1.4 Signature disable input (SIGDISA)

This pin is internally pulled down to V_{IN} to present a valid signature to PSE. Connect to V_{IN} if it is unused. Tie to GND to present an invalid signature.

Note: This signal is available for STHS4257A1 and STHS4257L1 only.

1.1.5 Power Good output ($\overline{PWRGD}$)

This pin indicates that the STHS4257x/x1 power MOSFET is fully on and works in normal operation mode (Power Good). Open drain, low impedance means that the power is good; in all other cases, the impedance is high (referenced to V_{IN}).

1.1.6 Negative power output (V_{OUT})

This is the Power Output, negative rail.

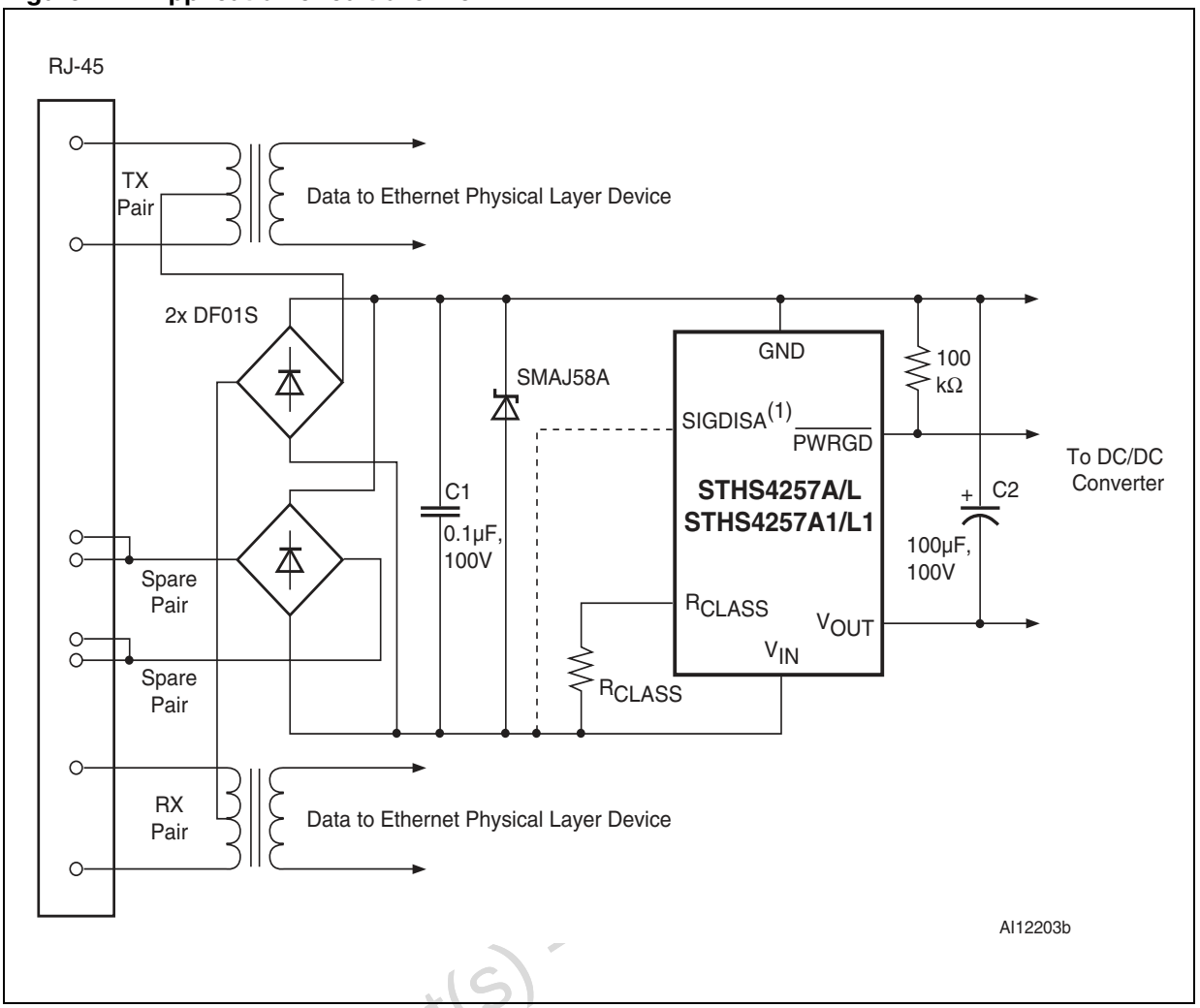
1.2 IEEE802.3af PD power classes

Table 3. IEEE802.3af PD power classes and corresponding R_{CLASS} values

Class	Usage	Max. power levels at input of PD (W)	Nominal classification load current (mA)	R_{CLASS} Resistor (Ω, 1%)
0	Default	0.44 to 12.95	< 5	Open
1	Optional	0.44 to 3.84	10.5	124
2	Optional	3.84 to 6.49	18.5	68.1
3	Optional	6.49 to 12.95	28	45.3
4	Reserved	Reserved (1)	40	30.9

1. Class 4 is currently reserved and should not be used.

Figure 4. Application circuit overview



1. STHS4257A1 and STHS4257L1 devices only. To disable signature, tie this pin to GND.
2. This configuration uses either data wires or spare wires for DC power.

Figure 5. Block diagram (STHS4257A/L)

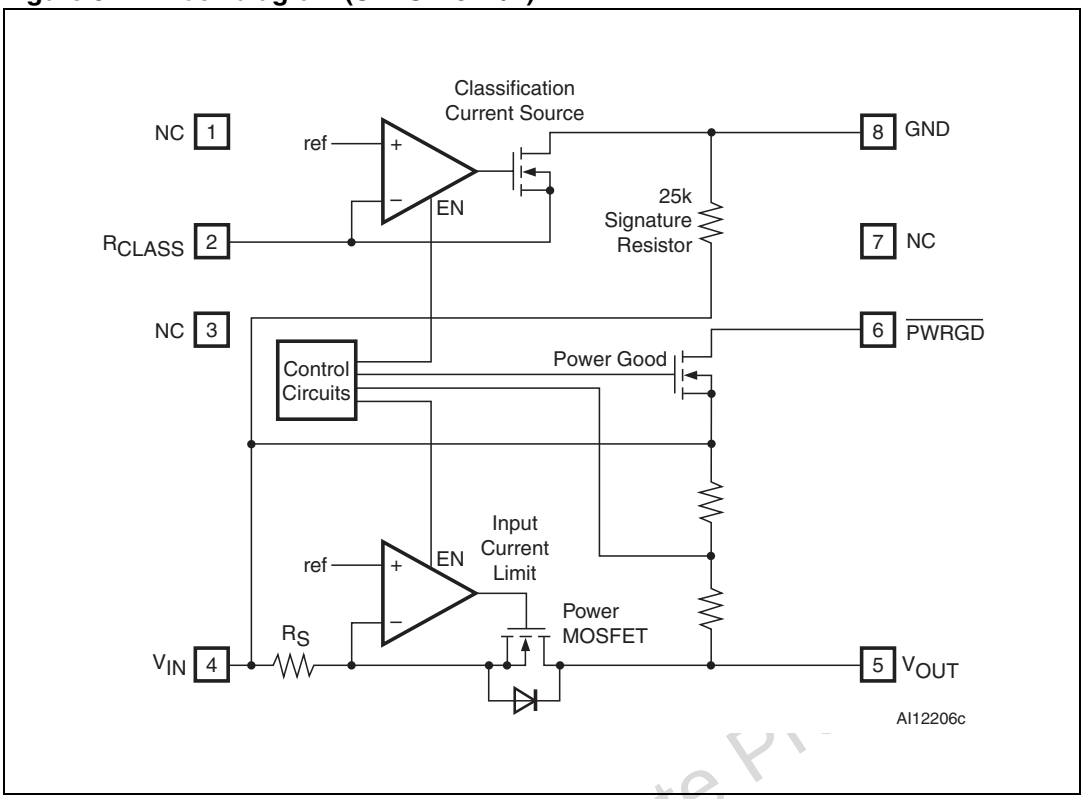


Figure 6. Typical application circuit (STHS4257A/L) with a DC/DC converter

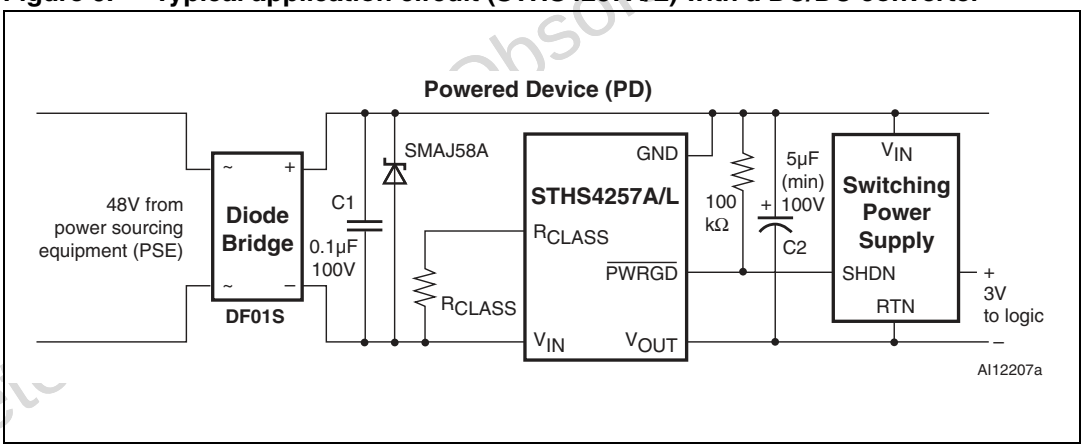
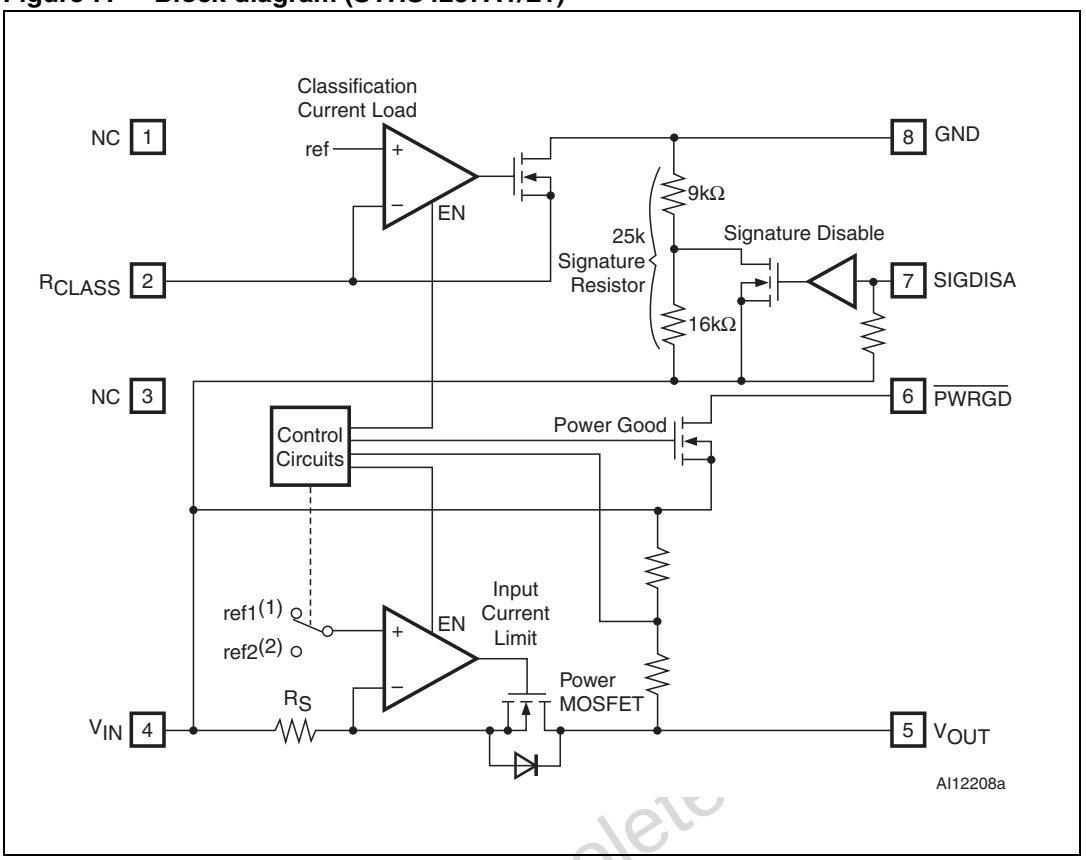
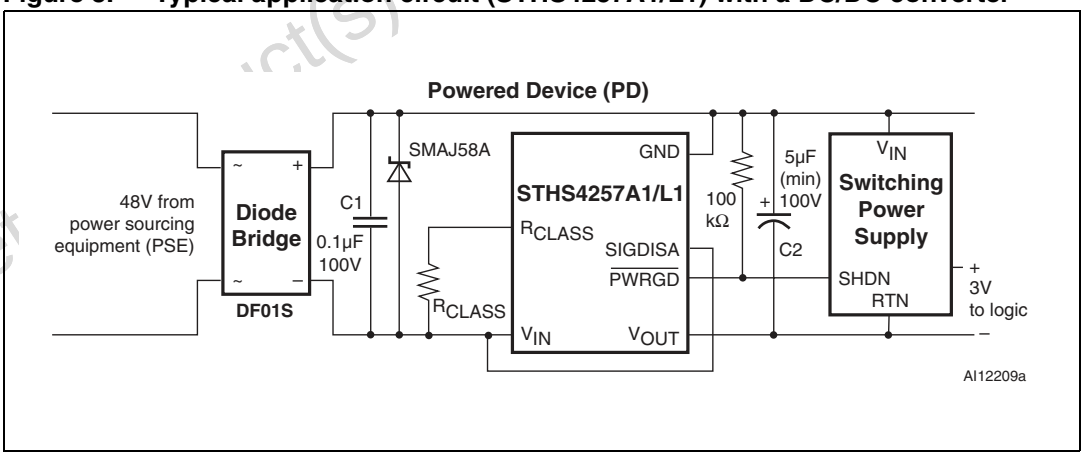


Figure 7. Block diagram (STHS4257A1/L1)



1. Ref.1 = $I_{LIMIT\ HIGH}$
2. Ref. 2 = $I_{LIMIT\ LOW}$

Figure 8. Typical application circuit (STHS4257A1/L1) with a DC/DC converter



2 Absolute maximum ratings

Stressing the device above the rating listed in the *Table 4: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input/supply voltage (1)	+0.3 to –100	V
V_{OUT}	Voltage on V_{OUT} pin	V_{IN} +100 to V_{IN} –0.3	V
$V_{SIGDISA}$, $V_{\overline{PWRGD}}$	Voltage on the respective pins	V_{IN} +90 to V_{IN} –0.3	V
V_{RCLASS}	Voltage on R_{CLASS} pin	V_{IN} +7 to V_{IN} –0.3	V
$I_{\overline{PWRGD}}$	Power Good output current	10	mA
I_{RCLASS}	R_{CLASS} pin current	100	mA
T_A	Operating ambient temperature range	–40 to 85	°C
T_{STG}	Storage temperature	–55 to 150	°C
T_{SLD}	Lead solder temperature for 10 seconds, lead-free lead finish (2)	260	°C

1. With respect to the GND pin.
2. Reflow at peak temperature of 260°C (total thermal budget not to exceed 245°C for more than 30 seconds).

3 Electrical parameters

Over the full operating temperature range, unless otherwise noted. Specifications common for both STHS4257x (=STHS4257A, STHS4257L) and STHS4257x1 (=STHS4257A1, STHS4257L1) product families unless otherwise noted.

Table 5. Electrical parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Maximum Operating Voltage	Input/supply voltage - with respect to GND pin (1), (2), (3)			–57	V
	Signature Range		–1.5		–9.5	V
	Classification Range		–12.5		–21	V
	UVLO Turn-On Voltage, **STHS4257x1**		–34.8	–36.0	–37.2	V
	UVLO Turn-On Voltage, **STHS4257x**		–37.7	–39.2	–40.2	V
	UVLO Turn-Off Voltage		–29.3	–30.5	–31.5	V
$I_{IN\ ON}$	Supply Current when on	V_{IN} = –48V, pins 5, 6, 7 floating		0.33	0.5	mA
$I_{IN\ CLASS}$	Supply Current During Classification	V_{IN} = –17.5V, pins 2, 7 floating, V_{OUT} tied to GND (4)	0.12	0.25	0.38	mA
ΔI_{CLASS}	Current Accuracy During Classification	10mA < I_{CLASS} < 40mA, –12.5V ≤ V_{IN} ≤ –21V (5)			±3.5	%
$R_{SIGNATURE}$	Signature Resistance	–1.5V ≤ V_{IN} ≤ –9.5V, V_{OUT} tied to GND, IEEE 802.3af 2-point measurement (2), (6)	23.25		26.00	kΩ
$R_{INVALID}$	Invalid Signature Resistance	–1.5V ≤ V_{IN} ≤ –9.5V, SIGDISA and V_{OUT} tied to GND, IEEE 802.3af 2-point measurement (2), (6), (7)		9	11.8	kΩ
V_{IH}	Signature Disable High Level Input Voltage	With respect to V_{IN}, high level invalidates signature (7)	3		57	V
V_{IL}	Signature Disable Low Level Input Voltage	With respect to V_{IN}, low level enables signature (7)			0.45	V
R_{INPUT}	Signature Disable Input Resistance	With respect to V_{IN}	100			kΩ
$V_{PG\ OUT}$	Power Good Output Low Voltage	I_{PG} = 1mA, V_{IN} = –48V, $\overline{PWRGD}$ referenced to V_{IN}			0.5	V
$V_{PG\ TH\ RISE}$ (8)	Power Good Trip Point, power good signal going inactive	V_{IN} = –48V, voltage between V_{IN} and V_{OUT}, V_{OUT} rising	2.7	3.0	3.3	V
$I_{PG\ LEAK}$	Power Good Leakage Current	$V_{\overline{PWRGD}}$ - V_{IN} = 57V, $\overline{PWRGD}$ MOSFET off, $V_{\overline{PWRGD}}$ = V_{GND} (9)			1	µA
R_{ON}	On-Resistance	I = 350mA, V_{IN} = –48V, measured from V_{IN} to V_{OUT}		0.72	1.0	Ω
$I_{OUT\ LEAK}$	V_{OUT} Pin Leakage Current	V_{IN} = 0V, power MOSFET off, V_{OUT} = 57V (10)			1	µA
$I_{LIMIT\ HIGH}$	Input Current Limit, High Level, **STHS4257x1** (normal operation mode)	V_{IN} = –48V, V_{OUT} = –43V (11), (12) 0°C ≤ T_A ≤ 70°C	340	375	400	mA
		–40°C ≤ T_A ≤ 85°C	330	375	400	mA

Table 5. Electrical parameters (continued)

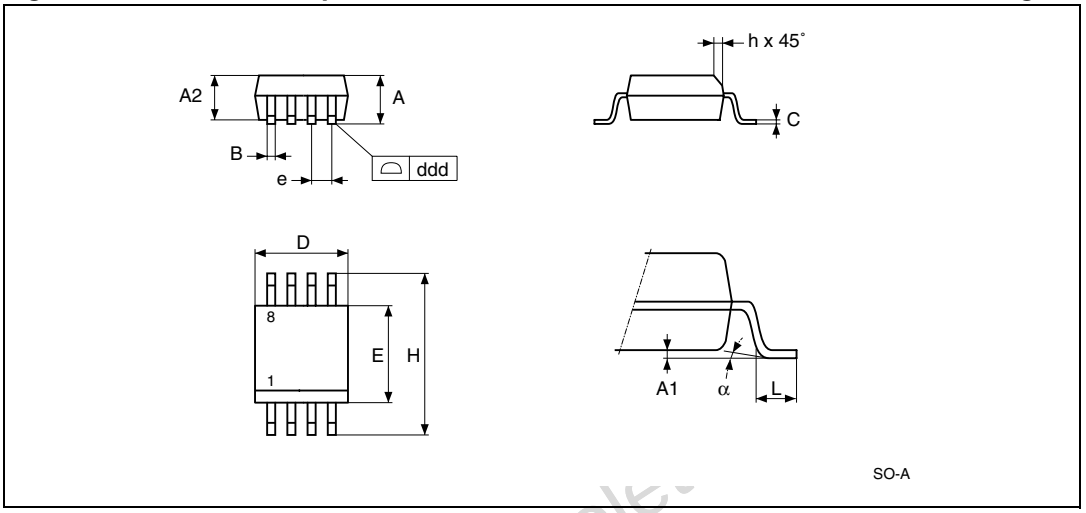
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{LIMIT\ LOW}$	Input Current Limit, Low Level, **STHS4257x1** (inrush mode)	V_{IN} = –48V, V_{OUT} = –43V (11), (12)	100	140	180	mA
I_{LIMIT}	Input Current Limit, **STHS4257x**	V_{IN} = –48V, V_{OUT} = –43V (14)	300	350	400	mA
$I_{LIMIT\ WARM}$	Overtemperature Input Current Limit, **STHS4257x**	(14)		188		mA
$T_{OVERTEMP}$	Overtemperature Trip Temperature, **STHS4257x**	(14)		120		°C
$T_{SHUTDOWN}$	Thermal Shutdown Trip Temperature	(11), (13), (14)		140		°C

1. The STHS4257 family of PoE products operates with a negative supply voltage (with respect to the GND pin, unless otherwise noted). Voltages in this data sheet are always referred to in terms of absolute magnitude, thus "maximum negative voltage" means the most negative voltage and analogically "rising negative voltage" refers to a voltage that is becoming more negative.
2. The STHS4257 family of products is designed to work with two series diode drops caused by diode bridge that makes the PD input polarity-insensitive. Parameter ranges specified in the Electrical Parameters Table are with respect to STHS4257x/x1 pins and are designed to meet the IEEE 802.3af specifications when these diode drops are included. See *Figure 4 on page 8*.
3. The STHS4257x/x1 devices include hysteresis in the UVLO voltages to avoid any start-up oscillation. As required by IEEE 802.3af, the STHS4257 family devices will power up from a voltage source with 20Ω series resistance on the first trial.
4. The Supply Current During Classification ($I_{IN\ CLASS}$) does not include classification current programmed at pin 2. Total supply current in classification mode will be $I_{IN\ CLASS}$ + I_{CLASS} (see also *Note 5*).
5. I_{CLASS} is the measured current flowing through R_{CLASS}. ΔI_{CLASS} accuracy is with respect to the ideal current defined as I_{CLASS} = 1.237/R_{CLASS}. The current accuracy specification does not include variations in R_{CLASS} resistance. The total classification current seen by PSE also includes the quiescent current ($I_{IN\ CLASS}$). See *Figure 4 on page 8*.
6. Signature resistance is measured via the 2-point ΔV/ΔI method as defined by IEEE 802.3af standard. The STHS4257 device family signature resistance is offset from standard 25kΩ to account for the series diode bridge resistance. With two series diodes, the total PD resistance will be between 23.75kΩ and 26.25kΩ which meets IEEE 802.3af specifications. The minimum probe voltages measured at the STHS4257x/x1 pins are –1.5 and –2.5V. The maximum probe voltages are –8.5 and –9.5V.
7. To disable the 25kΩ signature, tie SIGDISA to GND (±0.1V) or hold SIGDISA high with respect to V_{IN}. See *Figure 4 on page 8*.
8. $V_{PG\ TH\ FALL}$ is not used: To eliminate the current peak during the transition from inrush to normal operation mode, the power MOSFET (between V_{OUT} and V_{IN} - see *Figure 5 on page 9*) turns fully on only after the inrush current decreases by 10% from its initial value (i.e. when the output capacitor is fully charged).
9. GND pin at the same potential as $\overline{PWRGD}$ pin to prevent ESD protection from impacting the measured results. To keep $\overline{PWRGD}$ MOSFET off under this condition, maintain uninterrupted inrush current e.g. by applying 1V voltage between V_{OUT} and V_{IN} pin. This will keep the device in inrush mode, thus preventing $\overline{PWRGD}$ from going active (on).
10. To significantly reduce $I_{OUT\ LEAK}$ and eliminate its impact on total current during detection and classification, the resistor divider used to provide feedback on V_{OUT} - V_{IN} voltage is disconnected below the UVLO threshold.
11. The STHS4257x1 includes thermal protection. In the event of an overtemperature condition ($T_{SHUTDOWN}$ is reached), the STHS4257x1 will turn off the power MOSFET until the part cools below the overtemperature limit ($T_{OVERTEMP}$). The STHS4257x1 is also protected against thermal damage from incorrect classification probing by the PSE: If the STHS4257x1 temperature exceeds the shutdown trip point ($T_{SHUTDOWN}$), the classification load current is disabled.
12. The STHS4257x1 includes dual level input current limit. At turn-on, before output capacitor C2 is charged, the STHS4257x1 current level is set to the low level. After the output capacitor C2 is charged, the STHS4257x1 switches to high level current limit and remains there until the input voltage drops below the UVLO turn-off threshold.
13. The STHS4257 family devices include overtemperature protection that is intended to protect the device during momentary overload conditions only. Continuous operation close to overtemperature limits may impair device reliability.
14. The STHS4257x includes smart thermal protection. In the event of an overtemperature condition, the STHS4257x will reduce the input current limit by 50% to reduce the power dissipation in the package. If the part continues heating and reaches the shutdown temperature ($T_{SHUTDOWN}$), the current is reduced to zero until the part cools below the overtemperature limit ($T_{OVERTEMP}$). The STHS4257x is also protected against thermal damage from incorrect classification probing by the PSE: If the STHS4257x temperature exceeds the shutdown trip point ($T_{SHUTDOWN}$), the classification load current is disabled.

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 9. SO8 – 8-lead plastic small outline, 150mils width, mechanical drawing

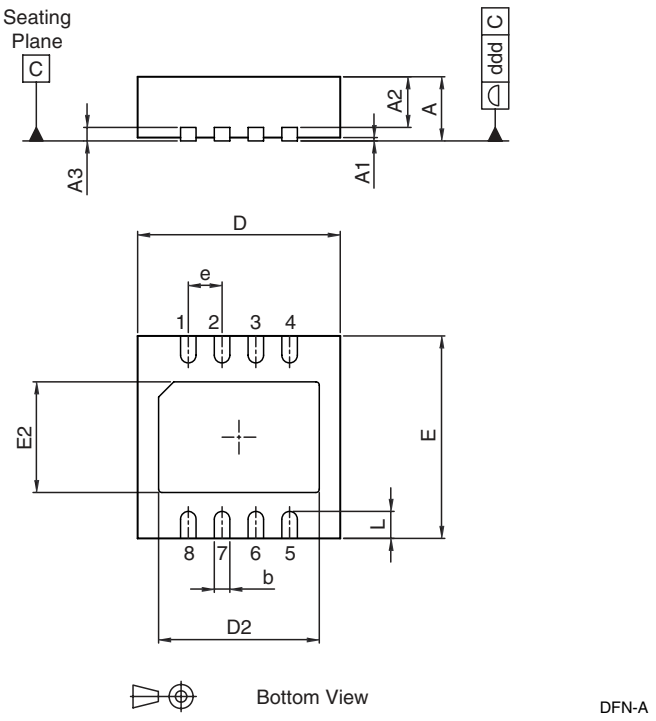


1. Drawing is not to scale.

Table 6. SO8 – 8-lead plastic small outline, 150mils width, mechanical data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	–	1.35	1.75	–	0.053	0.069
A1	–	0.10	0.25	–	0.004	0.010
B	–	0.33	0.51	–	0.013	0.020
C	–	0.19	0.25	–	0.007	0.010
D	–	4.80	5.00	–	0.189	0.197
ddd	–	–	0.10	–	–	0.004
E	–	3.80	4.00	–	0.150	0.157
e	1.27	–	–	0.050	–	–
H	–	5.80	6.20	–	0.228	0.244
h	–	0.25	0.50	–	0.010	0.020
L	–	0.40	0.90	–	0.016	0.035
α	–	0°	8°	–	0°	8°
N	8			8		

Figure 10. DFN8 – 8-lead dual flat no-lead outline, package mechanical drawing



1. Drawing is not to scale.

Table 7. DFN8 – 8-lead dual flat no-lead outline, package mechanical data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	0.90	0.80	1.00	0.035	0.031	0.039
A1	0.02	–	0.05	0.001		0.002
A2	0.70	–	–	0.028		
A3	0.20	–	–	0.008		
b	0.23	0.18	0.30	0.009	0.007	0.012
D	3.00	–	–	0.118		
D2	2.38	2.23	2.48	0.094		
ddd	–	–	0.08			0.003
E	3.00	–	–	0.118		
E2	1.64	1.49	1.74	0.065	0.059	0.069
e	0.50	–	–	0.020	–	–
L	0.40	0.30	0.50	0.016	0.012	0.020
N	8			8		

5 Part numbering

Table 8. Ordering information scheme

Example: STHS 4257A1 M 6 F

Device type

STHS

Product options

4257A

4257A1

4257L

4257L1

Package

M = SO8 (150mils width)

DB(1) = DFN8 (3mm x 3mm)

Temperature range

6 = –40 to 85°C

Shipping method

F = ECOPACK Package, Tape & Reel

E = ECOPACK Package, Tube

1. Contact local sales office for availability.

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
12-Jul-2006	1	Initial release.
19-Dec-2006	2	Updated *Features* and *Table 4*.
24-May-2007	3	Formatting changes and updated *Table 5*.
26-Jul-2007	4	Document status upgraded to full datasheet, updated cover page and *Table 8*.

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