- **10KH Compatible**

- **ECL and TTL Control Inputs**

- **Noninverting Outputs**

- **Flow-Through Architecture Optimizes PCB Layout**

- **Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**

- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)

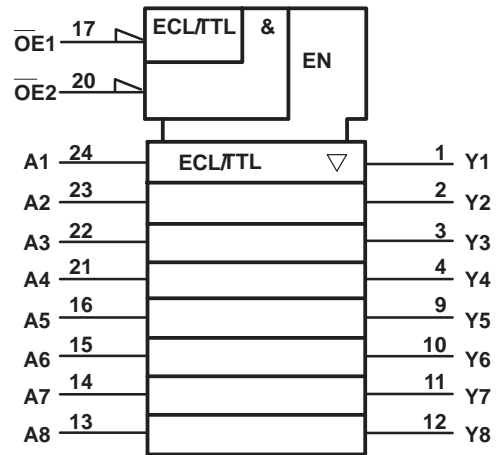|			
Y1	1	24	A1
Y2	2	23	A2
Y3	3	22	A3
Y4	4	21	A4
V_{CC}	5	20	$\overline{OE}2$ (TTL)
GND	6	19	V_{EE}
GND	7	18	GND
GND	8	17	$\overline{OE}1$ (ECL)
Y5	9	16	A5
Y6	10	15	A6
Y7	11	14	A7
Y8	12	13	A8
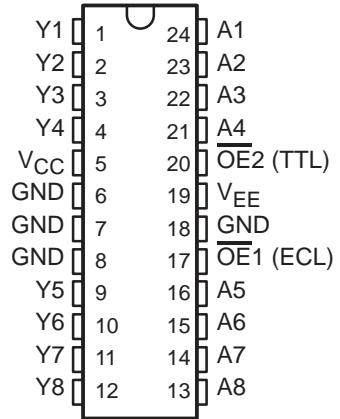
description

This octal ECL-to-TTL translator is designed to provide a efficient translation between a 10KH ECL signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

Two output-enable pins, $\overline{OE}1$ and $\overline{OE}2$, are provided. These control inputs are ANDed together with $\overline{OE}1$ being ECL compatible and $\overline{OE}2$ being TTL compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

The SN10KHT5541 is characterized for operation from 0°C to 75°C.

logic symbol†

ECL/TTL	&	EN
$\overline{OE}1$ — 17		
$\overline{OE}2$ — 20		

A1	24	ECL/TTL ▽	1	Y1
A2	23		2	Y2
A3	22		3	Y3
A4	21		4	Y4
A5	16		9	Y5
A6	15		10	Y6
A7	14		11	Y7
A8	13		12	Y8

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

OUTPUT ENABLE		DATA INPUT	OUTPUT (TTL)
$\overline{OE}1$	$\overline{OE}2$	A	Y
X	H	X	Z
H	X	X	Z
L	L	L	L
L	L	H	H

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

1

logic diagram (positive logic)

A1	24	ECL/TTL		1	Y1
A2	23	ECL/TTL		2	Y2
A3	22	ECL/TTL		3	Y3
A4	21	ECL/TTL		4	Y4

$\overline{OE1}$ (ECL) 17 ECL/TTL

$\overline{OE2}$ (TTL) 20

A5	16	ECL/TTL		9	Y5
A6	15	ECL/TTL		10	Y6
A7	14	ECL/TTL		11	Y7
A8	13	ECL/TTL		12	Y8

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	−0.5 V to 7 V
Supply voltage, V_{EE}	−8 V to 0 V
Input voltage (TTL) (see Note 1)	−1.2 V to 7 V
Input voltage (ECL)	V_{EE} to 0 V
Voltage applied to any output in the disabled or power-off state	−0.5 V to 5.5 V
Voltage applied to any output in the high state	−0.5 V to V_{CC}
Input current (TTL)	−30 mA to 5 mA
Current into any output in the low state	96 mA
Operating free-air temperature range	0°C to 75°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage		4.5	5	5.5	V
V_{EE}	ECL supply voltage		−4.94	−5.2	−5.46	V
V_{IH}	TTL high-level input voltage		2			V
V_{IL}	TTL low-level input voltage				0.8	V
V_{IH}‡	ECL high-level input voltage	T_A = 0°C	−1170		−840	
		T_A = 25°C	−1130		−810	mV
		T_A = 75°C	−1070		−735	
V_{IL}‡	ECL low-level input voltage	T_A = 0°C	−1950		−1480	
		T_A = 25°C	−1950		−1480	mV
		T_A = 75°C	−1950		−1450	
I_{IK}	TTL input clamp current				−18	mA
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current				48	mA
T_A	Operating free-air temperature		0		75	°C

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{OE}2$ only	$V_{CC} = 4.5$ V,	$V_{EE} = -4.94$ V,	$I_I = -18$ mA				−1.2	V
I_I	$\overline{OE}2$ only	$V_{CC} = 5.5$ V,	$V_{EE} = -5.46$ V,	$V_I = 7$ V				0.1	mA
I_{IH}	$\overline{OE}2$ only	$V_{CC} = 5.5$ V,	$V_{EE} = -5.46$ V,	$V_I = 2.7$ V				20	µA
I_{IL}	$\overline{OE}2$ only	$V_{CC} = 5.5$ V,	$V_{EE} = -5.46$ V,	$V_I = 0.5$ V				−0.5	mA
I_{IH}	Data inputs and $\overline{OE}1$	$V_{CC} = 5.5$ V,	$V_{EE} = -5.46$ V,	$V_I = -840$ mV	$T_A = 0°C$			350	µA
		$V_{CC} = 5.5$ V,	$V_{EE} = -5.46$ V,	$V_I = -810$ mV	$T_A = 25°C$			350	
		$V_{CC} = 5.5$ V,	$V_{EE} = -5.46$ V,	$V_I = -735$ mV	$T_A = 75°C$			350	
I_{IL}	Data inputs and $\overline{OE}1$	$V_{CC} = 5.5$ V,	$V_{EE} = -5.46$ V,	$V_I = -1950$ mV	$T_A = 0°C$	0.5			µA
					$T_A = 25°C$	0.5			
					$T_A = 75°C$	0.5			
V_{OH}		$V_{CC} = 4.5$ V,	$V_{EE} = -5.2$ V ± 5%,	$I_{OH} = -3$ mA		2.4	3.3		V
		$V_{CC} = 4.5$ V,	$V_{EE} = -5.2$ V ± 5%,	$I_{OH} = -15$ mA		2	3.1		
V_{OL}		$V_{CC} = 4.5$ V,	$V_{EE} = -5.2$ V ± 5%,	$I_{OL} = 48$ mA			0.38	0.55	V
I_{OZH}		$V_{CC} = 5.5$ V,	$V_{EE} = -5.46$ V,	$V_O = 2.7$ V				50	µA
I_{OZL}		$V_{CC} = 5.5$ V,	$V_{EE} = -5.46$ V,	$V_O = 0.5$ V				−50	µA
I_{OS}‡		$V_{CC} = 5.5$ V,	$V_{EE} = -5.46$ V,	$V_O = 0$		−100		−225	mA
I_{CCH}		$V_{CC} = 5.5$ V,	$V_{EE} = -5.46$ V				64	97	mA
I_{CCL}		$V_{CC} = 5.5$ V,	$V_{EE} = -5.46$ V				80	120	mA
I_{CCZ}		$V_{CC} = 5.5$ V,	$V_{EE} = -5.46$ V				77	116	mA
I_{EE}		$V_{CC} = 5.5$ V,	$V_{EE} = -5.46$ V				−22	−33	mA
C_i		$V_{CC} = 5$ V,	$V_{EE} = -5.2$ V				5		pF
C_o		$V_{CC} = 5$ V,	$V_{EE} = -5.2$ V				7		pF

† All typical values are at $V_{CC} = 5$ V, $V_{EE} = -5.2$ V, $T_A = 25°C$.
‡ Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50$ pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP§	MAX	
t_{PLH}	A	Y	1.7	4	6.2	ns
t_{PHL}			1.6	4	6.2	
t_{PZH}	$\overline{OE}1$	Y	2.6	4.7	6.7	ns
t_{PZL}			3.2	5.9	8.5	
t_{PHZ}	$\overline{OE}1$	Y	2.9	5.4	7.8	ns
t_{PLZ}			1.9	4.9	7.8	
t_{PZH}	$\overline{OE}2$	Y	1.7	4	6.2	ns
t_{PZL}			2.5	5.1	7.7	
t_{PHZ}	$\overline{OE}2$	Y	2.1	4.3	6.4	ns
t_{PLZ}			1.1	3.7	6.3	

§ All typical values are at $V_{CC} = 5$ V, $V_{EE} = -5.2$ V, $T_A = 25°C$.

TEXAS
INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION
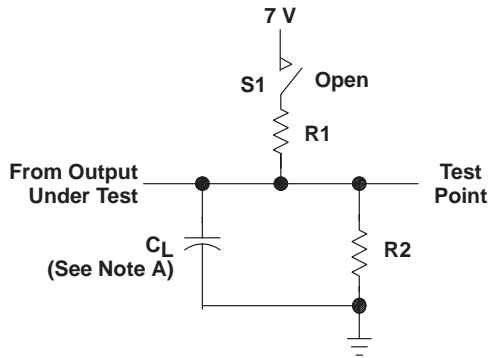
SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

LOAD CIRCUIT
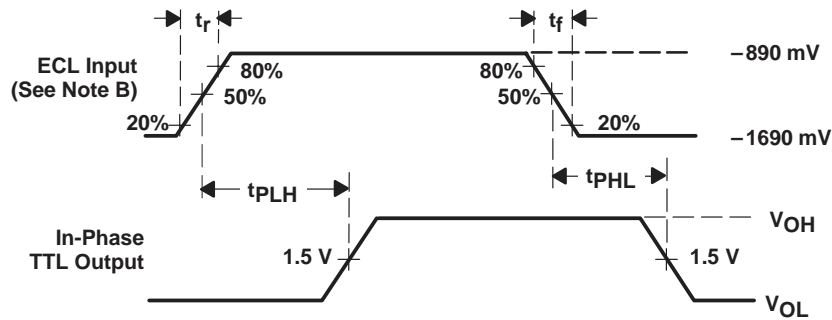
ECL- INPUT PROPAGATION DELAY TIMES
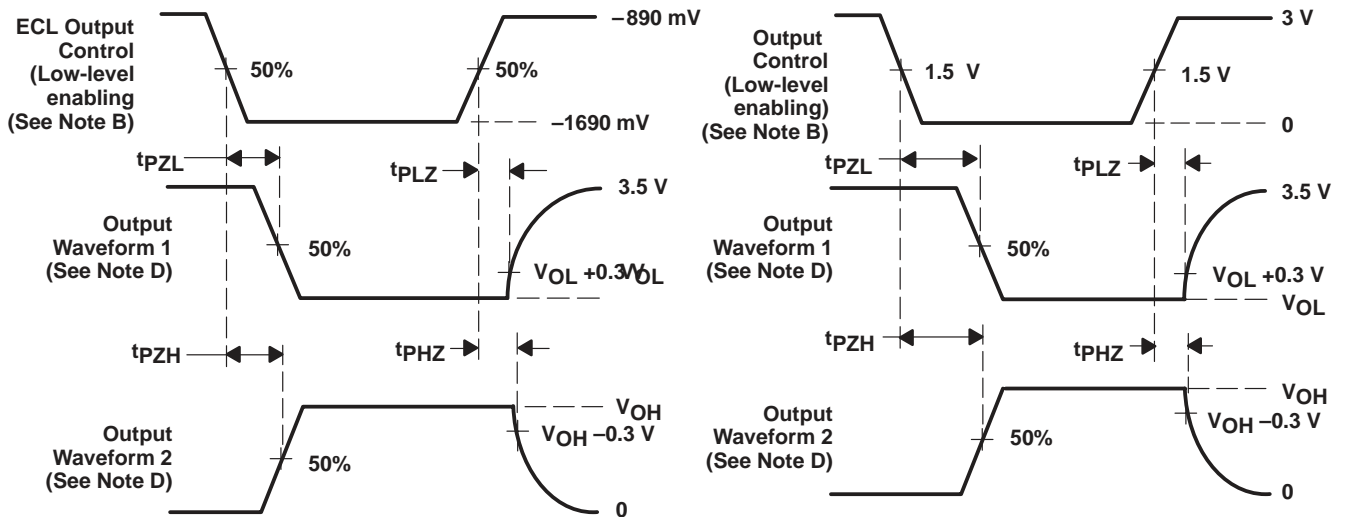
ECL ENABLE AND DISABLE TIMES

TTL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
  B. For TTL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
  C. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 0.7 ns, t_f ≤ 0.7 ns.
  D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  E. The outputs are measured one at a time with one transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN10KHT5541DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	10KHT5541	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
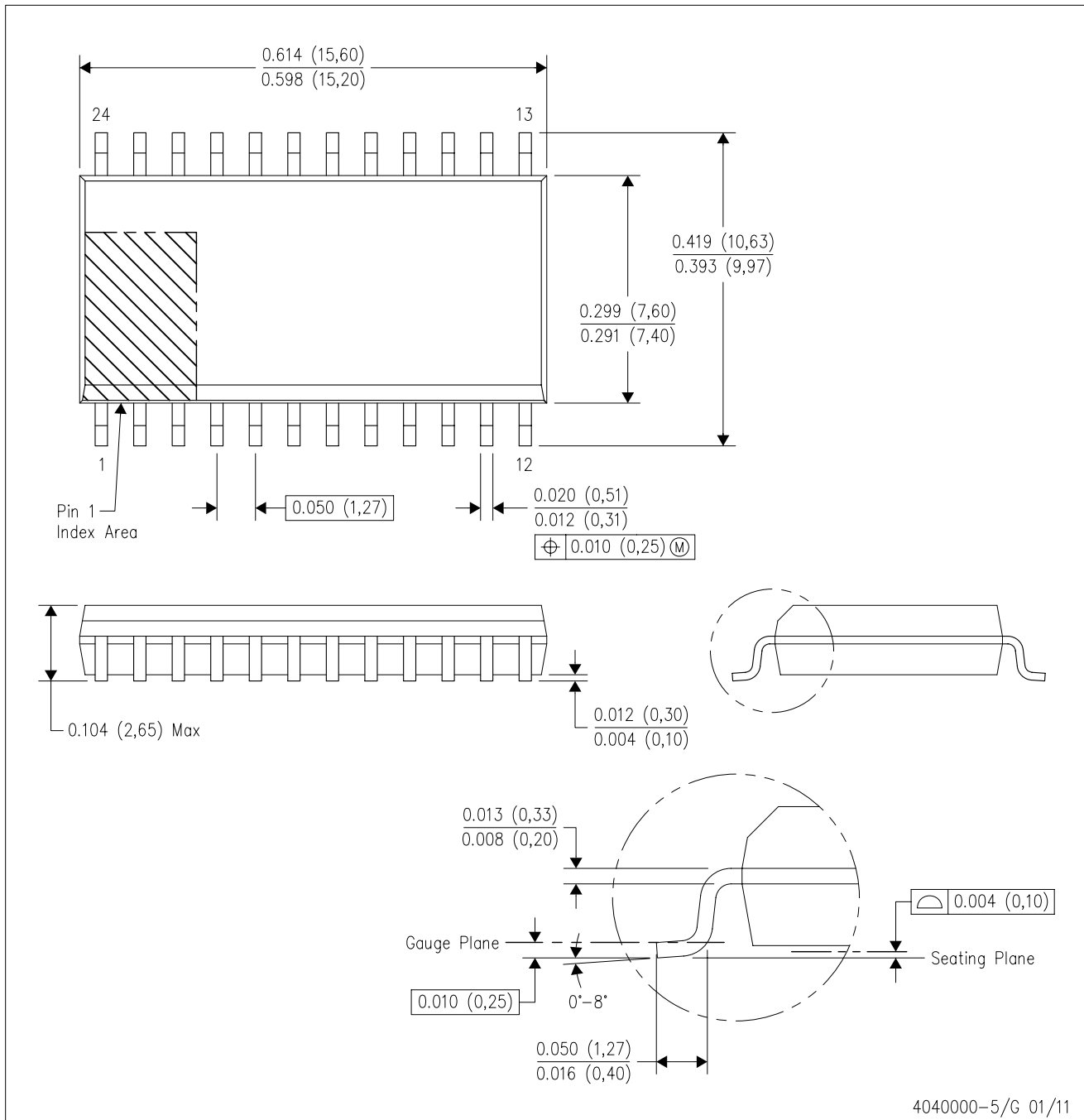
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DW (R−PDSO−G24)   PLASTIC SMALL OUTLINE

0.614 (15,60)
0.598 (15,20)

24   13

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   12

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−5/G 01/11

NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
          D.   Falls within JEDEC MS−013 variation AD.