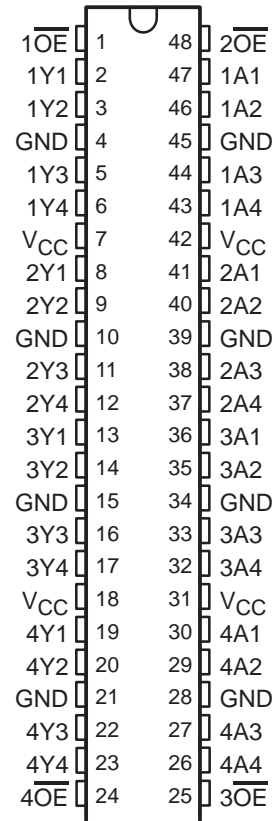


# SN54ABT162244, SN74ABT162244 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS238D – JUNE 1992 – REVISED MAY 1997

- Members of the Texas Instruments *Widebus*™ Family
- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABT162244 . . . WD PACKAGE  
SN74ABT162244 . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## description

The 'ABT162244 are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide noninverting outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT162244 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT162244 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# SN54ABT162244, SN74ABT162244

## 16-BIT BUFFERS/DRIVERS

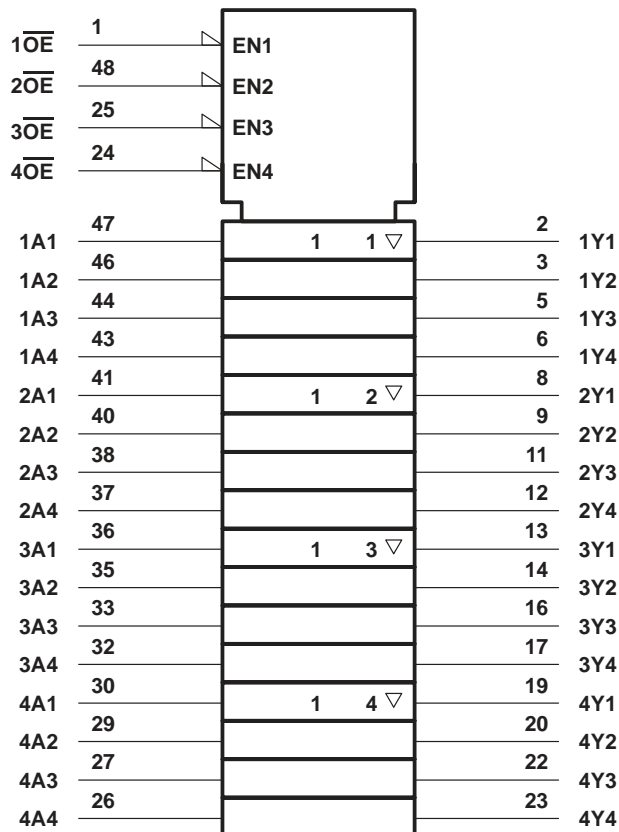
### WITH 3-STATE OUTPUTS

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FUNCTION TABLE  
(each 4-bit buffer)

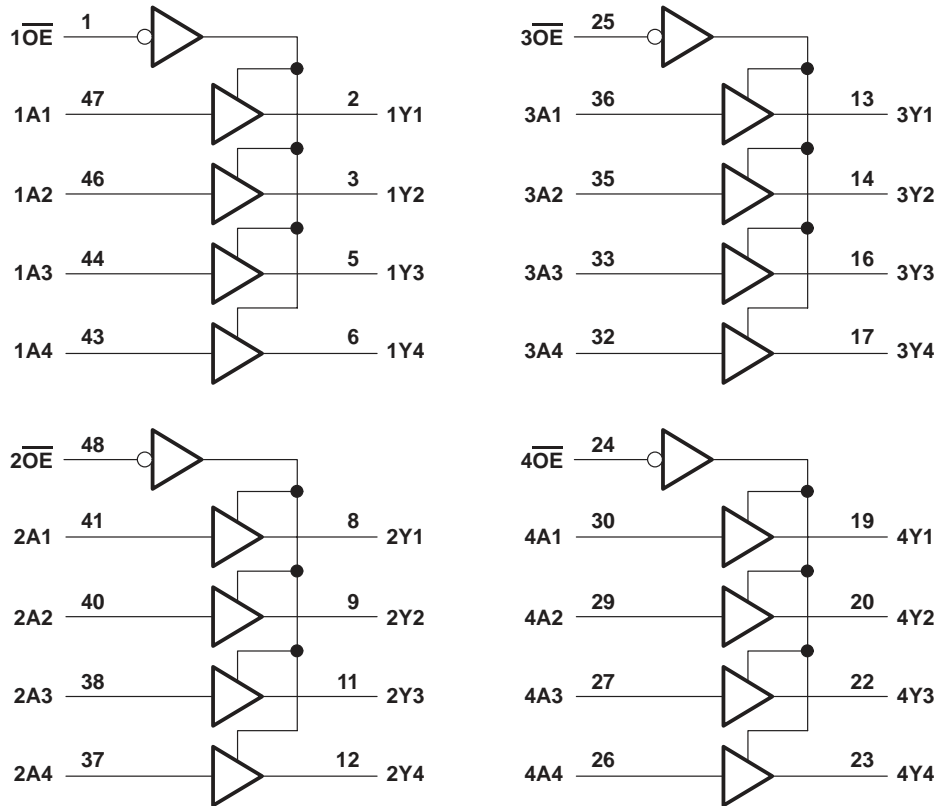
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

#### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	-0.5 V to 5.5 V
Current into any output in the low state, $I_O$ .....	30 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DGG package .....	89°C/W
DGV package .....	93°C/W
DL package .....	94°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

**SN54ABT162244, SN74ABT162244**  
**16-BIT BUFFERS/DRIVERS**  
**WITH 3-STATE OUTPUTS**

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**recommended operating conditions (see Note 3)**

		SN54ABT162244		SN74ABT162244		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-12		-12	mA
$I_{OL}$	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		$\mu s/V$
$T_A$	Operating free-air temperature	-55	125	-40	85	$^{\circ}C$

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



**SN54ABT162244, SN74ABT162244**  
**16-BIT BUFFERS/DRIVERS**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT162244		SN74ABT162244		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -1 mA	3.35			3.35			3.35	V
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -1 mA	3.85			3.85			3.85	
	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -3 mA	3.1			3.1			
I <sub>OH</sub> = -12 mA		2.6*						2.6	
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 8 mA	0.4	0.8		0.8		0.65	V
		I <sub>OL</sub> = 12 mA						0.8	
V <sub>hys</sub>			100						mV
I <sub>I</sub>	V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±1		±1		±1	μA
I <sub>OZPU</sub> ‡	V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA
I <sub>OZPD</sub> ‡	V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA
I <sub>OZH</sub>	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2$ V			10		10		10	μA
I <sub>OZL</sub>	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2$ V			-10		-10		-10	μA
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100				±100	μA
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V			50		50		50	μA
I <sub>O</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	-25	-55	-100	-25	-100	-25	-100	mA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high		2		2		2	mA
		Outputs low		30		30		30	
		Outputs disabled		2		2		2	
ΔI <sub>CC</sub> ¶	Data inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	Outputs enabled		50		50		μA
			Outputs disabled		50		50		
	Control inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND		50		50		50	
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V			3					pF
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V			8					pF

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ This parameter is characterized, but not production tested.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



**SN54ABT162244, SN74ABT162244**

**16-BIT BUFFERS/DRIVERS**

**WITH 3-STATE OUTPUTS**

SCBS238D – JUNE 1992 – REVISED MAY 1997

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

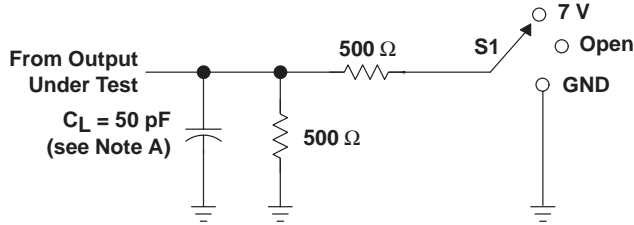
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT162244					UNIT
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX	
			MIN	TYP	MAX			
$t_{PLH}$	A	Y	1	2.5	3.6	1	4.1	ns
$t_{PHL}$			1	3.1	4.7	1	5.3	
$t_{PZH}$	$\overline{OE}$	Y	1	3.2	4.8	1	5.6	ns
$t_{PZL}$			1	3.2	4.7	1	5.5	
$t_{PHZ}$	$\overline{OE}$	Y	1	3.2	5.3	1	6.3	ns
$t_{PLZ}$			1	3.1	4.6	1	4.9	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT162244					UNIT
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX	
			MIN	TYP	MAX			
$t_{PLH}$	A	Y	1	2.5	3.2	1	3.9	ns
$t_{PHL}$			1	3.1	4	1	4.8	
$t_{PZH}$	$\overline{OE}$	Y	1	3.2	4.2	1	5.4	ns
$t_{PZL}$			1	3.2	4.1	1	5.1	
$t_{PHZ}$	$\overline{OE}$	Y	1	3.2	4	1	4.6	ns
$t_{PLZ}$			1	3.1	3.9	1	4.5	

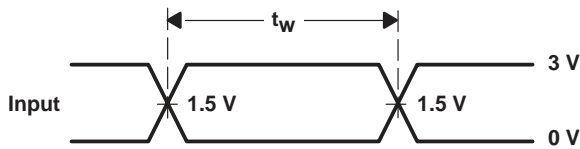


PARAMETER MEASUREMENT INFORMATION

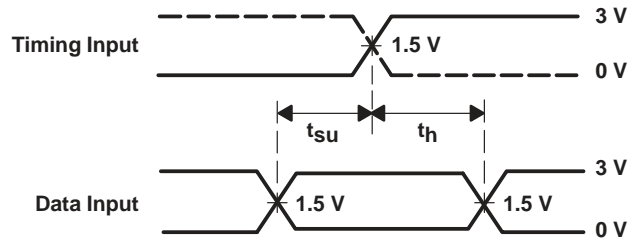


LOAD CIRCUIT

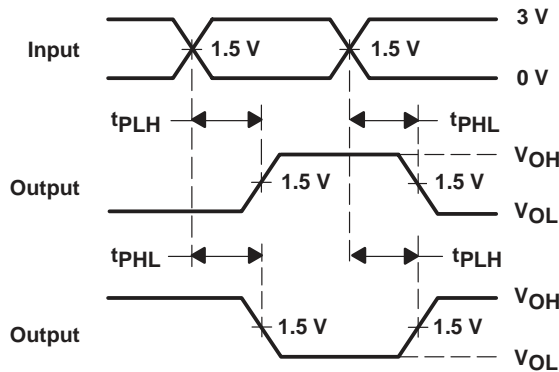
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



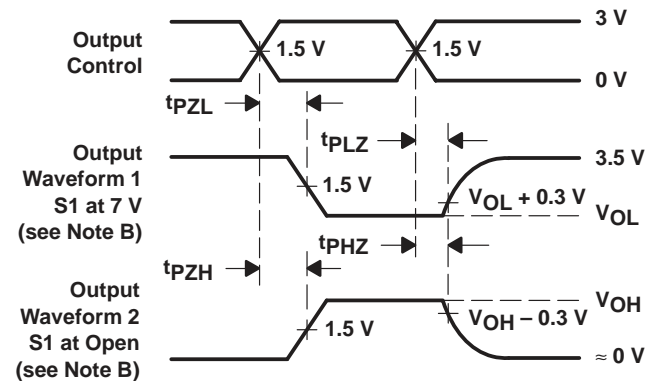
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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PRODUCT SUPPORT: [TRAINING](#)

SN54ABT162244, 16-Bit Buffers/ Drivers With 3-State Outputs  
 DEVICE STATUS: ACTIVE

PARAMETER NAME	SN54ABT162244	SN74ABT162244
Voltage Nodes (V)	5	5
V <sub>CC</sub> range (V)	4.5 to 5.5	4.5 to 5.5
Input Level	TTL	TTL
Output Level	TTL	TTL
No. of Outputs	16	
Output Drive (mA)		-12/12
t <sub>pd</sub> max (ns)		4.8
Static Current		16
Logic	True	

## FEATURES

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## DESCRIPTION

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The 'ABT162244 are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide noninverting outputs and symmetrical active-low output-enable (OE) inputs.

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The SN54ABT162244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT162244 is characterized for operation from -40°C to 85°C.

## TECHNICAL DOCUMENTS

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**DATASHEET**

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Full datasheet in Acrobat PDF: [sn54abt162244.pdf](#) (117 KB, Rev.D) (Updated: 05/01/1997)

**APPLICATION NOTES**

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View Application Notes for [Digital Logic](#)

- [Advanced BiCMOS Technology \(ABT\) Logic Characterization Information \(Rev. B\)](#) (SCBA008B - Updated: 06/01/1997)
- [Advanced BiCMOS Technology \(ABT\) Logic Enables Optimal System Design \(Rev. A\)](#) (SCBA001A - Updated: 03/01/1997)
- [Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs \(Rev. A\)](#) (SCBA012A - Updated: 08/01/1997)
- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Family of Curves Demonstrating Output Skews for Advanced BiCMOS Devices \(Rev. A\)](#) (SCBA006A - Updated: 12/01/1996)
- [Implications of Slow or Floating CMOS Inputs \(Rev. C\)](#) (SCBA004C - Updated: 02/01/1998)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
- [Power-Up 3-State \(PU3S\) Circuits in TI Standard Logic Devices](#) (SZZA033 - Updated: 05/10/2002)
- [Quad Flatpack No-Lead Logic Packages \(Rev. C\)](#) (SCBA017C - Updated: 11/22/2002)
- [TI IBIS File Creation, Validation, and Distribution Processes](#) (SZZA034 - Updated: 08/29/2002)
- [Understanding Advanced Bus-Interface Products Design Guide](#) (SCAA029, 253 KB - Updated: 05/01/1996)
- [Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh \(Rev. A\)](#) (SZZA036A - Updated: 02/27/2003)

**MORE LITERATURE**

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- [Enhanced Plastic Portfolio Brochure](#) (SGZB004, 387 KB - Updated: 08/19/2002)
- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [Military Brief](#) (SGYN138, 803 KB - Updated: 10/10/2000)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet \(Rev. A\)](#) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- [Palladium Lead Finish User's Manual](#) (SDYV001, 2041 KB - Updated: 11/01/1996)
- [QML Class V Space Products Military Brief \(Rev. A\)](#) (SGZN001A, 257 KB - Updated: 10/07/2002)

**USER GUIDES**

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- [LOGIC Pocket Data Book](#) (SCYD013, 4837 KB - Updated: 12/05/2002)

**PRICING/ AVAILABILITY/ PKG**

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DEVICE INFORMATION Updated Daily								TI INVENTORY STATUS As Of 09:00 AM GMT, 17 Apr 2003			REPORTED DISTRIBUTOR INVENTORY As Of 09:00 AM GMT, 17 Apr 2003		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE   PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY   \$US	STD PACK QTY	IN STOCK	IN PROGRESS QTY   DATE	LEAD TIME	DISTRIBUTOR COMPANY   REGION	IN STOCK	PURCHASE
5962-9458701QXA	ACTIVE	<a href="#">CFP (WD)</a>   48	-55 TO 125		<a href="#">View Contents</a>	1KU   22.39	1	<u>2</u> *	81   12 May	8 WKS	<a href="#">Avnet</a>   Americas	66	<b>BUY NOW</b>
									33   19 May				
									> 10k   20 May				
SNJ54ABT162244WD	ACTIVE	<a href="#">CFP (WD)</a>   48	-55 TO 125	5962-9458701QXA	<a href="#">View Contents</a>	1KU   22.39	1	<u>0</u> *	94   21 Apr	8 WKS	None Reported <a href="#">View Distributors</a>		
									> 10k   20 May				

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