

5V/3.3V Dual Differential 2:1 Multiplexer

Features

- 3.3V and 5V Power Supply Option
- 440 ps Typical Propagation Delay
- Separate and Common Select
- High Bandwidth Output Transitions
- Internal 75 k Ω Input Pull Down Resistors
- Available in 20-Pin SOIC Package

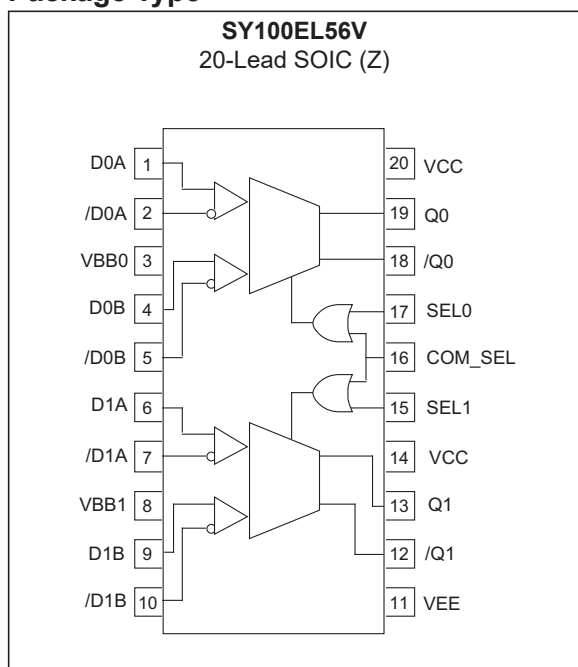
General Description

The SY100EL56V is a dual, fully differential 2:1 multiplexer. The differential data path makes the device ideal for multiplexing low skew clock or other skew sensitive signals. Multiple VBB pins are provided to ease AC coupling input signals.

The device features both individual and common select inputs to address both data path and random logic applications.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the D input will pull down to V_{EE} , the /D input will bias around $V_{CC}/2$ forcing the Q output LOW.

Package Type



SY100EL56V

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

| | |
|---|---------|
| PECL Power Supply Voltage (V_{CC}) (Note 1) | +8V |
| NECL Power Supply Voltage (V_{EE}) (Note 2) | -8V |
| PECL Mode Input Voltage (V_{IN}) (Note 3) | +6V |
| NECL Mode Input Voltage (V_{IN}) (Note 4) | -6V |
| Continuous Output Current (I_{OUT}) | 50 mA |
| Surge Output Current (I_{OUT}) | 100 mA |
| ESD Rating (Note 5) | >1.5 kV |

† **Notice:** Stresses above those listed under “Absolute Maximum ratings” may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: $V_{EE} = 0V$.

2: $V_{CC} = 0V$.

3: $V_{EE} = 0V, V_{IN} \leq V_{CC}$.

4: $V_{CC} = 0V, V_{IN} \geq V_{EE}$.

5: Mil Std. 883 Human Body Model, all pins.

DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = 3.0V$ to $5.5V$, $V_{EE} = 0V$ or $V_{EE} = -5.5V$ to $-3.0V$, $V_{CC} = 0V$;
 $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated. (Note 1)

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|-----------------------------------|---------------|------------------|------------------|------------------|---------|---|
| Power Supply Current | I_{EE} | — | 20 | 24 | mA | — |
| Output High Voltage (Note 2) | V_{OH} | $V_{CC} - 1.085$ | $V_{CC} - 1.005$ | $V_{CC} - 0.88$ | V | $T_A = -40^{\circ}C$ |
| | | $V_{CC} - 1.025$ | $V_{CC} - 0.955$ | $V_{CC} - 0.88$ | | $T_A = 0^{\circ}C$ to $+85^{\circ}C$ |
| Output Low Voltage (Note 2) | V_{OL} | $V_{CC} - 1.830$ | $V_{CC} - 1.695$ | $V_{CC} - 1.555$ | V | $T_A = -40^{\circ}C$ |
| | | $V_{CC} - 1.810$ | $V_{CC} - 1.705$ | $V_{CC} - 1.620$ | | $T_A = 0^{\circ}C$ to $+85^{\circ}C$ |
| Input High Voltage (Single-Ended) | V_{IH} | $V_{CC} - 1.165$ | — | $V_{CC} - 0.880$ | V | — |
| Input Low Voltage (Single-Ended) | V_{IL} | $V_{CC} - 1.810$ | — | $V_{CC} - 1.475$ | V | — |
| Output Reference Voltage | V_{BB} | $V_{CC} - 1.38$ | — | $V_{CC} - 1.26$ | V | — |
| Common Mode Range (Note 3) | V_{IHCMR} | $V_{EE} + 1.3$ | — | $V_{CC} - 0.4$ | V | $T_A = -40^{\circ}C$, $V_{PP} < 500$ mV |
| | | $V_{EE} + 1.2$ | — | $V_{CC} - 0.4$ | | $T_A = 0^{\circ}C$ to $85^{\circ}C$, $V_{PP} < 500$ mV |
| | | $V_{EE} + 1.5$ | — | $V_{CC} - 0.4$ | | $T_A = -40^{\circ}C$, $V_{PP} \geq 500$ mV |
| | | $V_{EE} + 1.4$ | — | $V_{CC} - 0.4$ | | $T_A = 0^{\circ}C$ to $85^{\circ}C$, $V_{PP} \geq 500$ mV |
| Input Sensitivity (Note 4) | V_{PP} (DC) | 50 | — | — | mV | — |
| Input High Current | I_{IH} | — | — | 150 | μA | — |
| Input Low Current | I_{IL} | 0.5 | — | — | μA | D, SEL, COM_SEL |
| | | -300 | — | — | μA | /D |

- Note 1:** Devices are designed to meet the DC specifications shown in the above table after thermal equilibration has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.
- 2:** Outputs are terminated through a 50Ω resistor to $V_{CC} - 2.0V$.
- 3:** The CMR range is referenced to the most positive side of the differential input voltage. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between 150 mV and 1V.
- 4:** Differential input voltage required to obtain a full ECL swing on the outputs.

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AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = +3.0V$ to $+5.5V$, $V_{EE} = 0V$ or $V_{EE} = -5.5V$ to $-3.02V$, $V_{CC} = 0V$; $T_A = -40^\circ C$ to $+85^\circ C$, $R_L = 50\Omega$ to $V_{CC} - 2V$; unless otherwise stated.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|--------------------|------------|------|------|-------|--------------------------------|
| Propagation Delay D to Q (Differential) | t_{PLH}, t_{PHL} | 340 | — | 540 | ps | $T_A = -40^\circ C$ |
| | | 350 | — | 550 | | $T_A = 0^\circ C$ |
| | | 360 | — | 560 | | $T_A = +25^\circ C$ |
| | | 380 | — | 580 | | $T_A = +85^\circ C$ |
| Propagation Delay D to Q (Single-Ended) | | 290 | — | 590 | | $T_A = -40^\circ C$ |
| | | 300 | — | 600 | | $T_A = 0^\circ C$ |
| | | 310 | — | 610 | | $T_A = +25^\circ C$ |
| | | 330 | — | 630 | | $T_A = +85^\circ C$ |
| Propagation Delay SEL, COM_SEL to Q | | 430 | — | 730 | | $T_A = -40^\circ C$ |
| | | 440 | — | 740 | | $T_A = 0^\circ C, +25^\circ C$ |
| | | 450 | — | 750 | | $T_A = +85^\circ C$ |
| Within Device Skew (Note 1) | | t_{SKEW} | — | 40 | | 80 |
| Duty Cycle Skew (Note 2) | — | | — | 100 | — | |
| Input Swing (Note 3) | $V_{PP}(AC)$ | 150 | — | 1000 | mV | — |
| Output Rise/Fall Time Q (20% to 80%) | t_r/t_f | 200 | — | 540 | ps | — |

Note 1: Within-device skew defined as identical transitions on similar paths through a device.

Note 2: Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.

Note 3: Input swing for which AC parameters are ensured.

TEMPERATURE SPECIFICATIONS

| Parameters | Symbol | Min. | Typ. | Max. | Units | Conditions |
|--|---------------|------|------|------|-------|--------------------|
| Temperature Ranges | | | | | | |
| Operating Temperature Range | T_A | -40 | — | +85 | °C | — |
| Storage Temperature | T_S | -65 | — | +150 | °C | — |
| Lead Temperature | T_{LEAD} | — | — | +260 | °C | Soldering, 20 sec. |
| Package Thermal Resistance (SOIC) | | | | | | |
| Junction-to-Ambient | θ_{JA} | — | 90 | — | °C/W | Still Air |
| | | — | 60 | — | | 500 lfpm |
| Junction-to-Case | θ_{JC} | — | 35 | — | °C/W | — |

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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

TABLE 2-1: PIN FUNCTION TABLE

| Pin Name | Description |
|-------------|--------------------------|
| D0A - D1A | Input Data A. |
| D0B - D1B | Input Data B. |
| SEL0 - SEL1 | Individual Select Input. |
| COM_SEL | Common Select Input. |
| Q0 - Q1 | True Outputs. |
| /Q0 - /Q1 | Inverted Outputs. |

2.1 Truth Table

TABLE 2-2: TRUTH TABLE

| SEL | DATA |
|-----|------|
| H | A |
| L | B |

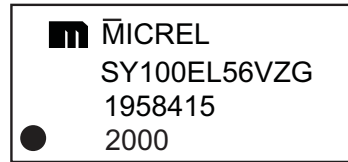
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

20-Lead SOIC*



Example



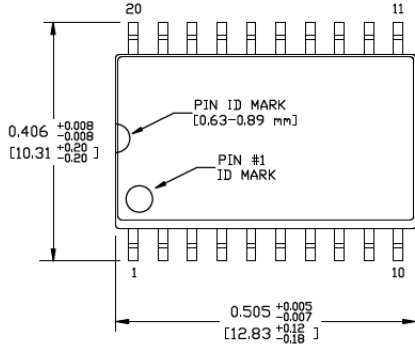
| | | |
|----------------|--|--|
| Legend: | XX...X | Product code or customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |
| | •, ▲, ▼ | Pin one index is identified by a dot, delta up, or delta down (triangle mark). |
| Note: | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. | |
| | Underbar (¯) and/or Overbar (¯) symbol may not be to scale. | |

SY100EL56V

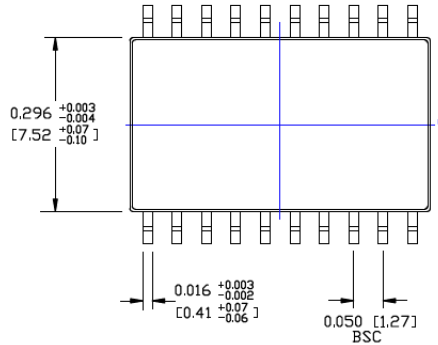
TITLE

20 LEAD SOICW PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

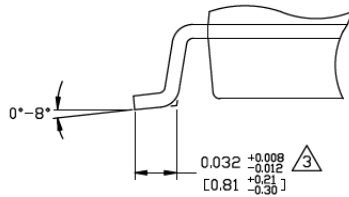
| DRAWING # | SOICW-20LD-PL-1 | UNIT | INCH [MM] |
|-----------|-----------------|------|-----------|
|-----------|-----------------|------|-----------|



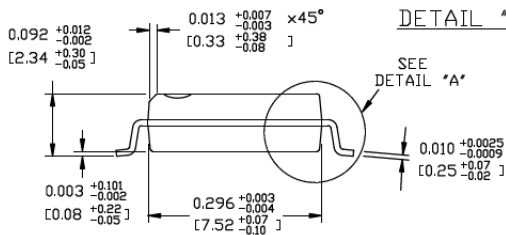
TOP VIEW
NOTE: 1, 2



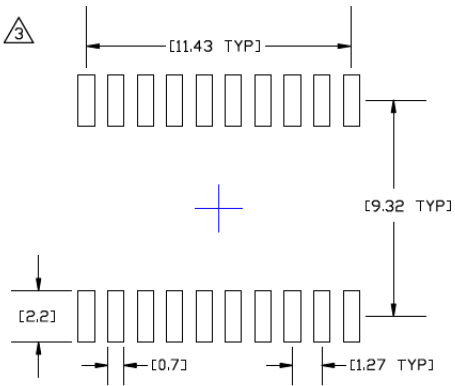
BOTTOM VIEW
NOTE: 1, 2



DETAIL "A"



END VIEW
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN

NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

APPENDIX A: REVISION HISTORY

Revision A (August 2019)

- Converted Micrel document SY100EL56V to Microchip data sheet DS20006242A.
- Minor text changes throughout.

SY100EL56V

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| <u>PART NO.</u> | <u>-XX</u> | <u>X</u> | <u>X</u> | <u>-XX</u> | Examples: |
|------------------------------|----------------------|-----------------------------------|-------------------------------|--------------------|---|
| Device | Supply Voltage Range | Package | Temperature Range | Special Processing | |
| Device: | SY100EL56: | Dual Differential 2:1 Multiplexer | | | a) SY100EL56VZG: SY100EL56, 3.3V/5V, 20-Lead SOIC, -40°C to +85°C, 38/Tube |
| Supply Voltage Range: | V | = | 3.3V/5V | | b) SY100EL56VZG-TR: SY100EL56, 3.3V/5V, 20-Lead, SOIC, -40°C to +85°C, 1,000/Reel |
| Package: | Z | = | 20-Lead SOIC (Pb-Free NiPdAu) | | |
| Temperature Range: | G | = | -40°C to +85°C | | |
| Special Processing: | <blank> | = | 38/Tube | | |
| | TR | = | 1,000/Reel | | Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option. |

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