# **Self-Protected FET** with Temperature and **Current Limit**

## 40 V, 6.5 A, Single N-Channel, DPAK

Self-protected FETs are a series of power MOSFETs which utilize ON Semiconductor HDPlus™ technology. The self-protected MOSFET incorporates protection features such as integrated thermal and current limits. The self-protected MOSFETs include an integrated Drain-to-Gate Clamp that provides overvoltage protection from transients and avalanche. The device is protected from Electrostatic Discharge (ESD) by utilizing an integrated Gate-to-Source Clamp.

#### **Features**

- Short Circuit Protection
- In Rush Current Limit
- Thermal Shutdown with Automatic Restart
- Avalanche Rated
- Overvoltage Protection
- ESD Protection (4 kV HBM)
- Controlled Slew Rate for Low Noise Switching
- AEC Q101 Qualified
- This is a Pb-Free Device

#### **Applications**

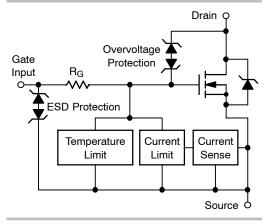
- Solenoid Driver
- Relay Driver
- Small Motors
- Lighting
- · Relay Replacement
- Load Switching



### ON Semiconductor®

#### http://onsemi.com

V <sub>DSS</sub> (Clamped)	R <sub>DS(on)</sub> Typ	I <sub>D</sub> Typ (Limited)
40 V	110 mΩ @ 10 V	6.5 A



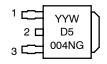


# **CASE 369C** STYLE 2

G

1

### **MARKING** DIAGRAM



D5004N = Device Code 1 = Gate = Drain = Year WW = Work Week = Source = Pb-Free Device

#### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NID5004NT4G	DPAK (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

### MOSFET MAXIMUM RATINGS ( $T_J = 25^{\circ}C$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage Internally Clamped	V <sub>DSS</sub>	44	Vdc
Gate-to-Source Voltage	V <sub>GS</sub>	±14	Vdc
Drain Current Continuous	I <sub>D</sub>	Internally Limited	
Total Power Dissipation  @ T <sub>A</sub> = 25°C (Note 1)  @ T <sub>A</sub> = 25°C (Note 2)	P <sub>D</sub>	1.3 2.5	W
Thermal Resistance Junction-to-Case Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	R <sub>θJC</sub> R <sub>θJA</sub> R <sub>θJA</sub>	3.0 95 50	°C/W
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD}$ = 30 Vdc, $V_{GS}$ = 5.0 Vdc, $I_{L}$ = 1.8 Apk, $L$ = 160 mH, $R_{G}$ = 25 $\Omega$ ) (Note 3)	E <sub>AS</sub>	273	mJ
Operating and Storage Temperature Range (Note 4)	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. Surface mounted onto minimum pad size (100 sq/mm) FR4 PCB, 1 oz cu.
- Mounted onto 1" square pad size (700 sq/mm) FR4 PCB, 1 oz cu.
   Not subject to Production Test
- 4. Normal pre-fault operating range. See thermal limit range conditions.

### MOSFET ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic			Min	Тур	Max	Unit
OFF CHARACTERISTICS				III	1	1
Drain-to-Source Clamped Breakdown Voltage $(V_{GS} = 0 \text{ V}, I_D = 2 \text{ mA})$			36	40	44	V
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 32 V, V <sub>GS</sub> = 0 V)			-	27	100	μΑ
Gate Input Current (V <sub>GS</sub> = 5.0 V, V <sub>DS</sub> = 0 V)		I <sub>GSS</sub>	-	45	200	μА
ON CHARACTERISTICS						
Gate Threshold Voltage ( $V_{DS} = V_{GS}, I_D = 150 \mu A$ ) Threshold Temperature Coeffic	ent	V <sub>GS(th)</sub>	1.0	1.85 5.0	2.2	V -mV/°C
Static Drain-to-Source On-Re (V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.0 A, T <sub>J</sub> @ 2		R <sub>DS(on)</sub>	-	110	130	mΩ
Static Drain-to-Source On-Resistance (Note 5) $(V_{GS} = 5.0 \text{ V}, I_D = 2.0 \text{ A}, T_J @ 25^{\circ}\text{C})$ $(V_{GS} = 5.0 \text{ V}, I_D = 2.0 \text{ A}, T_J @ 150^{\circ}\text{C})$			- -	130 240	150 270	mΩ
Source–Drain Forward On Volta $(I_S = 7.0 \text{ A}, V_{GS} = 0 \text{ V})$	age	V <sub>SD</sub>	-	0.9	1.1	V
SWITCHING CHARACTERIST	ICS (Note 6)		•			
Turn-on Delay Time	$R_{L} = 6.6 \; \Omega, \; V_{in} = 0 \; to \; 10 \; V, \\ V_{DD} = 13.8 \; V, \; I_{D} = 2.0 \; A, \; 10\% \; V_{in} \; to \; 10\% \; I_{D}$	td <sub>(on)</sub>	-	97	115	ns
Turn-on Rise Time	$R_L = 6.6 \ \Omega, \ V_{in} = 0 \ to \ 10 \ V, \ V_{DD} = 13.8 \ V, \ I_D = 2.0 \ A, \ 10\% \ I_D \ to \ 90\% \ I_D$	t <sub>rise</sub>	-	282	300	ns
Turn-off Delay Time	$\begin{aligned} R_L &= 6.6 \ \Omega, \ V_{in} = 0 \ to \ 10 \ V, \\ V_{DD} &= 13.8 \ V, \ I_D = 2.0 \ A, \ 90\% \ V_{in} \ to \ 90\% \ I_D \end{aligned}$	td <sub>(off)</sub>	-	930	1020	ns
Turn-off Fall Time	$R_L = 6.6 \ \Omega, \ V_{in} = 0 \ to \ 10 \ V, \ V_{DD} = 13.8 \ V, \ I_D = 2.0 \ A, \ 90\% \ I_D \ to \ 10\% \ I_D$		_	690	750	ns
Slew Rate ON	ON $ \begin{aligned} R_L &= 6.6 \ \Omega, \ V_{in} = 0 \ \text{to} \ 10 \ \text{V}, \\ V_{DD} &= 13.8 \ \text{V}, \ I_D = 2.0 \ \text{A}, \ 70\% \ \text{to} \ 50\% \ \text{V}_{DD} \end{aligned} $		_	64	-	V/μs
Slew Rate OFF	Slew Rate OFF $ \begin{array}{c} {\sf R_L = 6.6~\Omega,V_{in} = 0~to~10~V,} \\ {\sf V_{DD} = 13.8~V,I_D = 2.0~A,50\%~to~70\%~V_{DD}} \end{array} $		_	28	-	V/μs
SELF PROTECTION CHARACT	<b>TERISTICS</b> ( $T_J = 25^{\circ}C$ unless otherwise noted) (Note	∋ 7)				
Current Limit	$\begin{split} V_{DS} &= 10 \text{ V}, \text{ V}_{GS} = 5.0 \text{ V}, \text{ T}_{J} = 25^{\circ}\text{C} \text{ (Note 8)} \\ V_{DS} &= 10 \text{ V}, \text{ V}_{GS} = 5.0 \text{ V}, \text{ T}_{J} = 100^{\circ}\text{C} \text{ (Note 6, 8)} \\ V_{DS} &= 10 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ T}_{J} = 25^{\circ}\text{C} \text{ (Note 6, 8)} \end{split}$	I <sub>LIM</sub>	4.0 4.0 -	6.5 5.5 7.9	11 11 -	А
Temperature Limit (Turn-off)	V <sub>GS</sub> = 5.0 V (Note 6)	T <sub>LIM(off)</sub>	150	180	200	°C
Thermal Hysteresis	V <sub>GS</sub> = 5.0 V	$\Delta T_{LIM(on)}$	-	10	-	°C
Temperature Limit (Turn-off)	V <sub>GS</sub> = 10 V (Note 6)	T <sub>LIM(off)</sub>	150	180	200	°C
Thermal Hysteresis	V <sub>GS</sub> = 10 V	$\Delta T_{LIM(on)}$	-	20	-	°C
$ \begin{array}{lll} \text{Input Current during} & \text{$V_{DS}=0$ V, $V_{GS}=5.0$ V, $T_{J}=T_{J}>T_{(fault)}$ (Note 6) } \\ \text{Thermal Fault} & \text{$V_{DS}=0$ V, $V_{GS}=10$ V, $T_{J}=T_{J}>T_{(fault)}$ (Note 6) } \\ \end{array} $		I <sub>g(fault)</sub>	5.5 12	5.2 11	-	mA
ESD ELECTRICAL CHARACTE	ERISTICS (T <sub>J</sub> = 25°C unless otherwise noted)					
Electrostatic Discharge Capability Human Body Model (HBM) Machine Model (MM) (Note 6)		ESD	4000 400	_ _	_ _	V

- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
   Not subject to Production Test
   Fault conditions are viewed as beyond the normal operating range of the part.
- 8. Current limit measured at 380  $\mu s$  after gate pulse.

#### **TYPICAL PERFORMANCE CURVES**

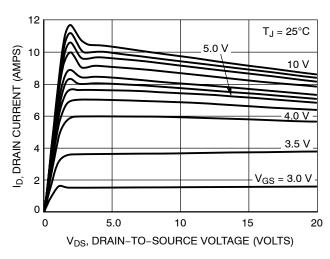


Figure 1. On-Region Characteristics

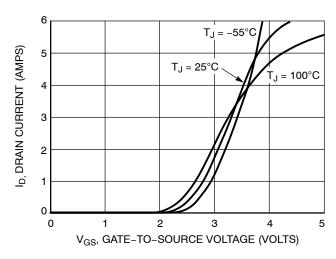


Figure 2. Transfer Characteristics

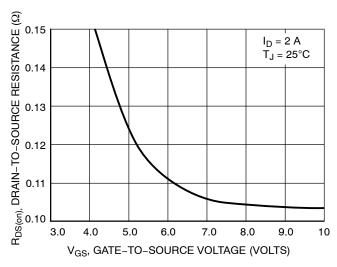


Figure 3. On-Resistance vs. Gate-to-Source Voltage

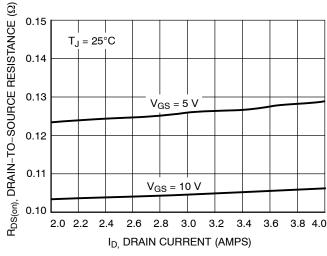


Figure 4. On-Resistance vs. Drain Current

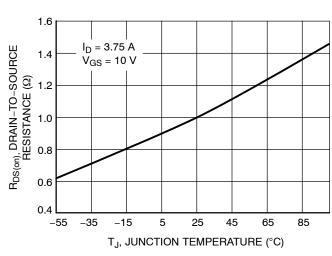


Figure 5. On–Resistance Variation with Temperature

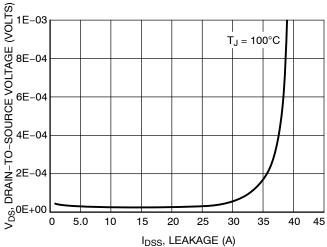
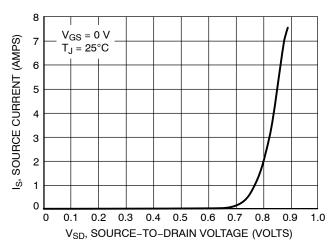


Figure 6. Drain-to-Source Leakage Current vs. Voltage

#### **zl** TYPICAL PERFORMANCE CURVES



12000 10000 8000 8000 4000 2000 6 7 8 9 10 V<sub>GS</sub>, GATE-TO-SOURCE VOLTAGE (VOLTS)

Figure 7. Diode Forward Voltage vs. Current

Figure 8. Input Current vs. Gate Voltage

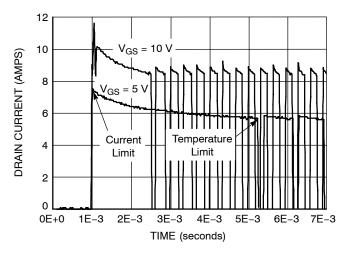


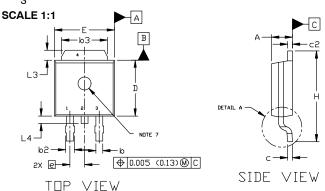
Figure 9. Short Circuit Response\*

<sup>\*(</sup>Actual thermal cycling response in short circuit dependent on device power level, thermal mounting, and ambient temperature conditions)





**DATE 31 MAY 2023** 



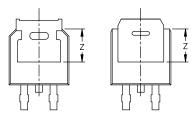


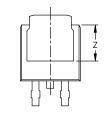
- DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994. CONTROLLING DIMENSION: INCHES
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS 63,
- L3. AND Z. L3, AND Z.

  DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH,
  PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR
  GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
  DIMENSIONS D AND E ARE DETERMINED AT THE
  OUTERMOST EXTREMES OF THE PLASTIC BODY.
  DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
  DETININAL MOLD ESCALUPE.

- OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS		
MIM	MIN.	MAX.	MIN.	MAX.	
Α	0.086	0.094	2.18	2.38	
A1	0.000	0.005	0.00	0.13	
b	0.025	0.035	0.63	0.89	
b2	0.028	0.045	0.72	1.14	
b3	0.180	0.215	4.57	5.46	
C	0.018	0.024	0.46	0.61	
c2	0.018	0.024	0.46	0.61	
D	0.235	0.245	5.97	6.22	
E	0.250	0.265	6.35	6.73	
e	0.090	BSC	2.29 BSC		
Н	0.370	0.410	9.40	10.41	
L	0.055	0.070	1.40	1.78	
L1	0.114	REF	2.90	REF	
L2	0.020 BSC		0.51	BSC	
L3	0.035	0.050	0.89	1.27	
L4		0.040		1.01	
Z	0.155		3.93		

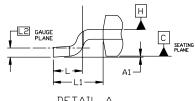




BOTTOM VIEW

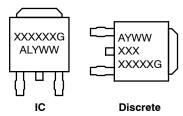
BOTTOM VIEW ALTERNATE CONSTRUCTIONS

5.80 [0.228] 6.20 [0.244] 2.58 3.00 [0.102] [0.118] 1.60 [0.063] 6.17 [0.243]



DETAIL A ROTATED 90° CW

**GENERIC MARKING DIAGRAM\*** 



XXXXXX	= Device Code
Α	= Assembly Location
L	= Wafer Lot
Υ	= Year
WW	= Work Week
G	= Pb-Free Package

\*This information is generic. Please refer to

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DUWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

3 FMITTER

4. COLLECTOR

s

3 GATE

RECOMMENDED MOUNTING FOOTPRINT\*

STYLE 1: STYLE 2: PIN 1. BASE PIN 1. GATE 2. COLLECTOR 2. DRAIL 3. EMITTER 3. SOUF 4. COLLECTOR 4. DRAIL	N 2. CATHODE RCE 3. ANODE	3. GATE	STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE
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STYLE 7: PIN 1. GATE 2. COLLECTOR STYLE 6: STYLE 8: STYLE 9: STYLE 10: PIN 1. MT1 2. MT2 PIN 1. N/C 2. CATHODE 3. ANODE PIN 1. ANODE 2. CATHODE

4. CATHODE

device data sheet for actual part marking. PIN 1. CATHODE 2. ANODE 3. CATHODE Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may 3 RESISTOR ADJUST not follow the Generic Marking. 4. ANODE

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DESCRIPTION:	DPAK (SINGLE GAUGE)		PAGE 1 OF 1	

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