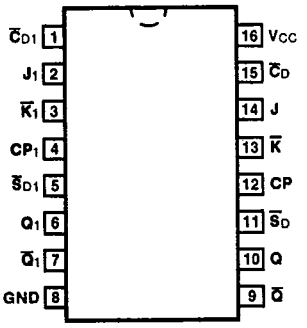
T-46-07-07

9024

DUAL J$\overline{K}$ (OR D) FLIP-FLOP

CONNECTION DIAGRAM
PINOUT A

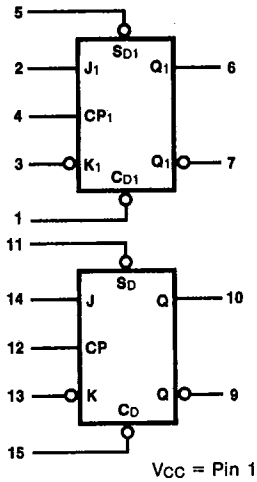


DESCRIPTION — The 9024 consists of two high speed, clocked J$\overline{K}$ flip-flops. The Clocking operation is independent of rise and fall times of the clock waveform. The J$\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and $\overline{K}$ pins together.

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +75°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Ceramic DIP (D)	A	9024DC	9024DM	6B
Flatpak (F)	A	9024FC	9024FM	4L

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	9XXX (U.L.) HIGH/LOW
J, $\overline{K}$ Inputs	1.5/1.0
Clock, $\overline{S}_D$ Inputs	3.0/2.0
$\overline{C}_D$ Input	6.0/3.0
Outputs	30/8.8 (7.8)

SYNCHRONOUS ENTRY J-$\overline{K}$ MODE OPERATION

INPUTS @ t_n		OUTPUTS @ t_{n+1}	
J	$\overline{K}$	Q	$\overline{Q}$
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

SYNCHRONOUS ENTRY D MODE OPERATION

INPUTS @ t_n	OUTPUTS @ t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
t_n, t_{n+1} = time before and after rising edge of CP.

ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

INPUTS		OUTPUTS	
$\overline{S}_D$ 5(11)	$\overline{C}_D$ 1(15)	Q 6(10)	$\overline{Q}$ 7(9)
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

DC CHARACTERISTICS OVER COMMERCIAL TEMPERATURE RANGE: V_{CC} = +5.0 V ±5%

SYMBOL	PARAMETER	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	1.9		1.8		1.6		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage		0.85		0.85		0.85	V	Guaranteed Input LOW Threshold
V_{OL}	Output LOW Voltage		0.45		0.45		0.45	V	V_{CC} = 4.75 V, I_{OL} = 14.1 mA
									V_{CC} = 5.25 V, I_{OL} = 16 mA
I_{IH}	Input HIGH Current J, $\overline{K}$				60		60	µA	V_{CC} = 5.25 V, V_{IN} = 4.5 V Gnd on Other Inputs
	Clock Input, $\overline{S}_D$				120		120		
	$\overline{C}_D$				240		240		
I_{IL}	Input LOW Current J, $\overline{K}$		-1.6		-1.6		-1.6	mA	V_{CC} = 5.25 V, V_{IN} = .45 V 4.5 V on Other Inputs
	Clock Input, $\overline{S}_D$		-3.2		-3.2		-3.2		
	$\overline{C}_D$*		-4.8		-4.8		-4.8		
	J, $\overline{K}$		-1.41		-1.41		-1.41	mA	V_{CC} = 4.75 V, V_{IN} = .45 V 4.5 V on Other Inputs
	Clock Input, $\overline{S}_D$		-2.82		-2.82		-2.82		
	$\overline{C}_D$*		-4.23		-4.23		-4.23		
I_{OS}	Output Short Circuit Current	-30	-100	-30	-100	-30	-100	mA	V_{CC} = 5.25 V, V_{OUT} = 0 V
I_{CC}	Power Supply Current				14			mA	Per Flip-Flop in Worst Logic State

*Denotes maximum current under normal operation. These currents may increase up to 4 I_{IL} if J, K = HIGH and $\overline{S}_D$ = LOW.

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9XXX Series

T-46-07-07

DC CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE: V_{CC} = +5.0 ±10%

SYMBOL	PARAMETER	-55°C		25°C		125°C		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
V_{IH}	Input HIGH Voltage	2.0		1.7		1.4		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage		0.8		0.9		0.8	V	Guaranteed Input LOW Threshold
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 12.4 mA V_{CC} = 5.5 V, I_{OL} = 16 mA
I_{IH}	Input HIGH Current J, $\overline{K}$ Clock Input, $\overline{S}_D$ $\overline{C}_D$				60 120 240		60 120 240	μA	V_{CC} = 5.5 V, V_{IN} = 4.5 V Gnd on Other Inputs
I_{IL}	Input LOW Current J, $\overline{K}$ Clock Input, $\overline{S}_D$ $\overline{C}_D$ (Note 4)		-1.6 -3.2 -4.8		-1.6 -3.2 -4.8		-1.6 -3.2 -4.8	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V 4.5 V on Other Inputs
	J, $\overline{K}$ Clock Input, $\overline{S}_D$ $\overline{C}_D$*		-1.24 -2.48 -3.72		-1.24 -2.48 -3.72		-1.24 -2.48 -3.72	mA	V_{CC} = 4.5 V, V_{IN} = 0.4 V 4.5 V on Other Inputs
I_{OS}	Output Short Circuit Current	-30	-100	-30	-100	-30	-100	mA	V_{CC} = 5.5 V, V_{OUT} = 0 V
I_{CC}	Power Supply Current				14			mA	Per Flip-Flop in Worst Logic State

*Denotes maximum current under normal operation. These currents may increase up to 4 I_{IL} if J, K = HIGH and $\overline{S}_D$ = LOW.

SWITCHING CHARACTERISTICS: T_A = 25°C, V_{CC} = +5.0 V, C_L = 15 pF

SYMBOL	PARAMETER	9XXX		UNITS	TEST CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CP to Q or $\overline{Q}$		20 33	ns	Figs. 3-1, 3-8
t_h (H) t_h (L)	Hold Time HIGH or LOW J, $\overline{K}$ to CP	0		ns	Figs. 3-1, 3-6
t_s (H) t_s (L)	Setup Time HIGH or LOW J, $\overline{K}$ to CP	20	1.0	ns	
t_{PLH}	Propagation Delay $\overline{S}_D$ to Q, $\overline{C}_D$ to $\overline{Q}$		12	ns	Figs. 3-1, 3-16
t_{PHL}	Propagation Delay $\overline{S}_D$ to $\overline{Q}$, $\overline{C}_D$ to Q		25	ns	
f_{max}	Maximum Toggle Frequency	25		MHz	Figs. 3-1, 3-8