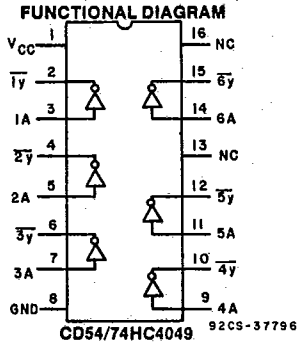
T-52-07-00

CD54/74HC4049
CD54/74HC4050

File No. **1543**

High-Speed CMOS Logic

FUNCTIONAL DIAGRAM



CD54/74HC4049 92CS-37796

Hex Buffers, Inverting and Non-Inverting

Type Features

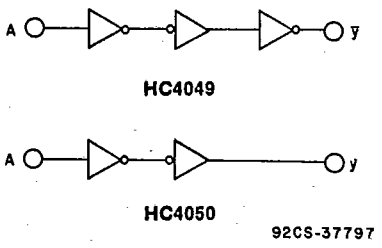
- *Typical propagation delay = 6 ns @ V_{CC} = 5 V, C_L = 15pF, T_A = 25°C*
- *High-to-low voltage level converter for up to V_I = 16 V*

The RCA-CD54/74HC4049 and CD54/74HC4050 are fabricated with high-speed silicon gate technology. They have a modified input protection structure that enables these parts to be used as logic level translators which will convert high-level logic to a low-level logic while operating off the low-level logic supply. For example, 0-V to 15-V input logic levels can be down-converted to 0-V to 5-V logic levels. The modified input protection structure protects the input from both positive and negative electrostatic discharge. These parts can also be used as simple buffers or inverters without level translation. The CD54/74HC4049 and CD54/74HC4050 are enhanced versions of equivalent CMOS types.

The CD54HC4049 and CD54/74HC4050 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix) and in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

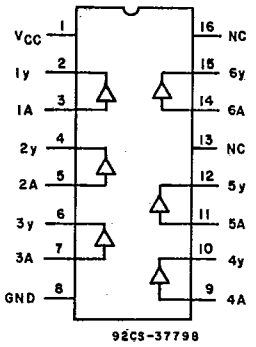
Family Features

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%,V_{CC}, N_{IH} = 30% V_{CC}; @ V_{CC} = 5 V



LOGIC DIAGRAMS

FUNCTIONAL DIAGRAM

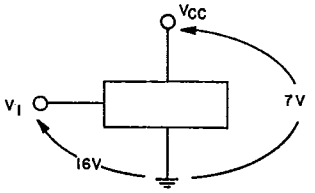


CD54/74HC4050

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}) ..... -0.5 to +7 V
DC INPUT VOLTAGE, (V_I)
(Voltages referenced to ground) ..... -0.5 to +16 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V) ..... -20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 V < V_o < V_{CC} + 0.5$ V) ..... ±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125° C
PACKAGE TYPE E, M ..... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

Voltage Relationships:
(Maximum Positive Limits)



92CS-37799RI

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
DC Output Voltage, V_O	0	V_{CC}	V
DC Input Voltage (V_I)	0	15	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r, t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		CD54/74HC4049, CD54/74HC4050											UNITS
		TEST CONDITIONS			74HC/54HC SERIES			74HC SERIES		54HC SERIES			
					+25°C			-40/ +85°C		-55/ +125°C			
		V_I V	I_O mA	V_{CC} V	Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
High-Level Input Voltage	V_{IH}			2	1.5	—	—	1.5	—	1.5	—		V
				4.5	3.15	—	—	3.15	—	3.15	—		
				6	4.2	—	—	4.2	—	4.2	—		
Low-Level Input Voltage	V_{IL}			2	—	—	0.5	—	0.5	—	0.5		V
				4.5	—	—	1.35	—	1.35	—	1.35		
				6	—	—	1.8	—	1.8	—	1.8		
High-Level Output Voltage CMOS Loads	V_{OH}	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—		V
				4.5	4.4	—	—	4.4	—	4.4	—		
				6	5.9	—	—	5.9	—	5.9	—		
TTL Loads (Standard Output)		V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—		V
			-5.2	6	5.48	—	—	5.34	—	5.2	—		
Low-Level Output Voltage CMOS Loads	V_{OL}	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1		V
				4.5	—	—	0.1	—	0.1	—	0.1		
				6	—	—	0.1	—	0.1	—	0.1		
TTL Loads (Standard Output)		V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4		V
			5.2	6	—	—	0.26	—	0.33	—	0.4		
Input Leakage Current	I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1		μA
		15		6	—	—	±0.5	—	±5	—	±5		
Quiescent Device Current	I_{CC}	15 or Gnd	0	6	—	—	2	—	20	—	40		μA

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r,t_f=6 ns)

CHARACTERISTIC		SYMBOL	54HC AND 74HC	
			TYPICAL	UNITS
Propagation Delay, Data Input to Output (C_L = 15 pF)	HC4049 HC4050	t_{PLH}, t_{PHL}	6	ns
Power Dissipation Capacitance*		C_{PD}	35	pF

*C_{PD} is used to determine the dynamic power consumption, per inverter
$P_D = V_{CC}^2 f_i(C_{PD} + C_L)$ where: f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r,t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C		-40° C to +85° C		-55° C to +125° C		UNITS
			HC		74HC		54HC		
			Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay nA to n$\overline{Y}$ HC4049 nA to nY HC4050	t_{PLH}, t_{PHL}	2	—	85	—	105	—	130	ns
		4.5	—	17	—	21	—	26	
		6	—	14	—	18	—	22	
Transition Time	t_{TLH}, t_{THL}	2	—	75	—	95	—	110	ns
		4.5	—	15	—	19	—	22	
		6	—	13	—	16	—	19	
Input Capacitance	C_I	—	—	10	—	10	—	10	pF

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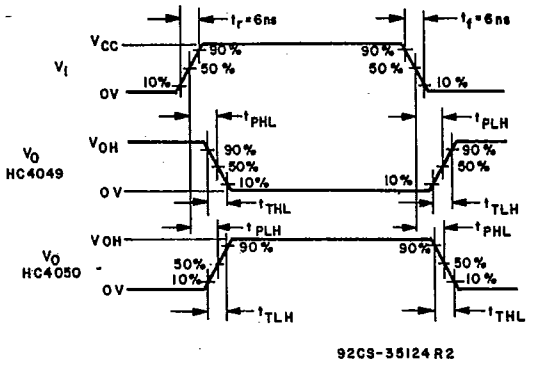

Fig. 1 - Transition times and propagation delay times, combination logic.