ISL78600

Multi-Cell Li-Ion Battery Manager

The ISL78600 Li-ion battery manager IC supervises up to 12 series-connected cells. The part provides accurate monitoring, cell balancing, and extensive system diagnostics functions. Three cell balancing modes are incorporated: Manual Balance mode, Timed Balance mode, and Auto Balance mode. The Auto Balance mode terminates balancing functions when a charge transfer value specified by the host microcontroller has been met.

The ISL78600 communicates to a host microcontroller through an SPI interface and to other ISL78600 devices using a robust, proprietary, 2-wire daisy chain system.

The ISL78600 is offered in a 64 Ld TQFP package and is specified for operation at a temperature range of -40°C to +105°C.

Applications

- Hybrid Electric Vehicle (HEV), Plug-in Hybrid Electric Vehicle (PHEV), and Electric Vehicle (EV) battery packs
- Electric motorcycle battery packs
- Backup battery and energy storage systems requiring high accuracy management and monitoring
- Portable and semiportable equipment

Related Literature

For a full list of related documents, visit our website

- ISL78600 product page

Features

- Up to 12-cell voltage monitors with support for Li-ion CoO_2, Li-ion Mn_2O_4, and Li-ion FePO4 chemistries
- Board level cell voltage measurement accuracy ±1.5mV
- 13-bit cell voltage measurement
- Pack voltage measurement accuracy ±100mV
- 14-bit pack voltage and temperature measurements
- Cell voltage scan rate of 19.5µs per cell (234µs to scan 12 cells)
- Internal and external temperature monitoring
- Up to four external temperature inputs
- Robust daisy chain communications system
- Integrated system diagnostics for all key internal functions
- Hardwired and communications based fault notification
- Integrated watchdog shuts down device if communication is lost
- 2Mbps SPI
- AEC-Q100 qualified

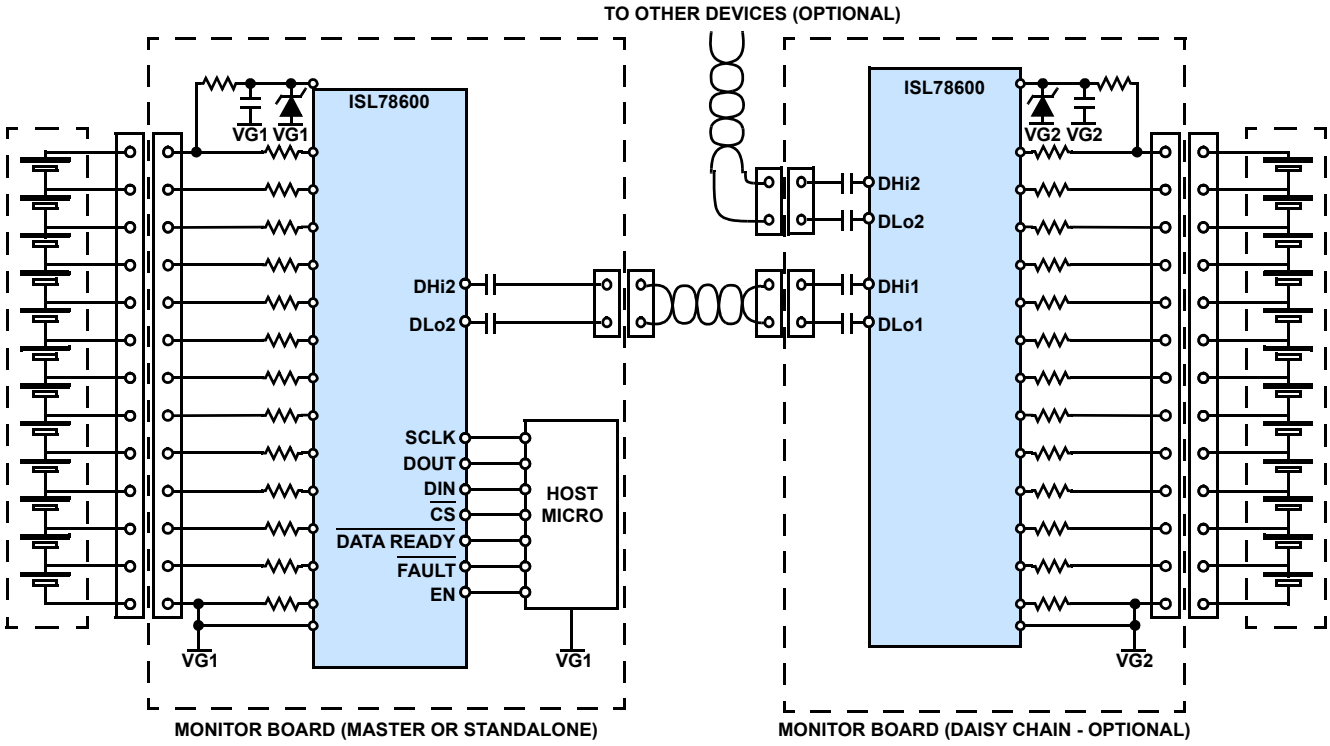


Figure 1. Typical Application

Contents

1. Overview

1.1 Block Diagram

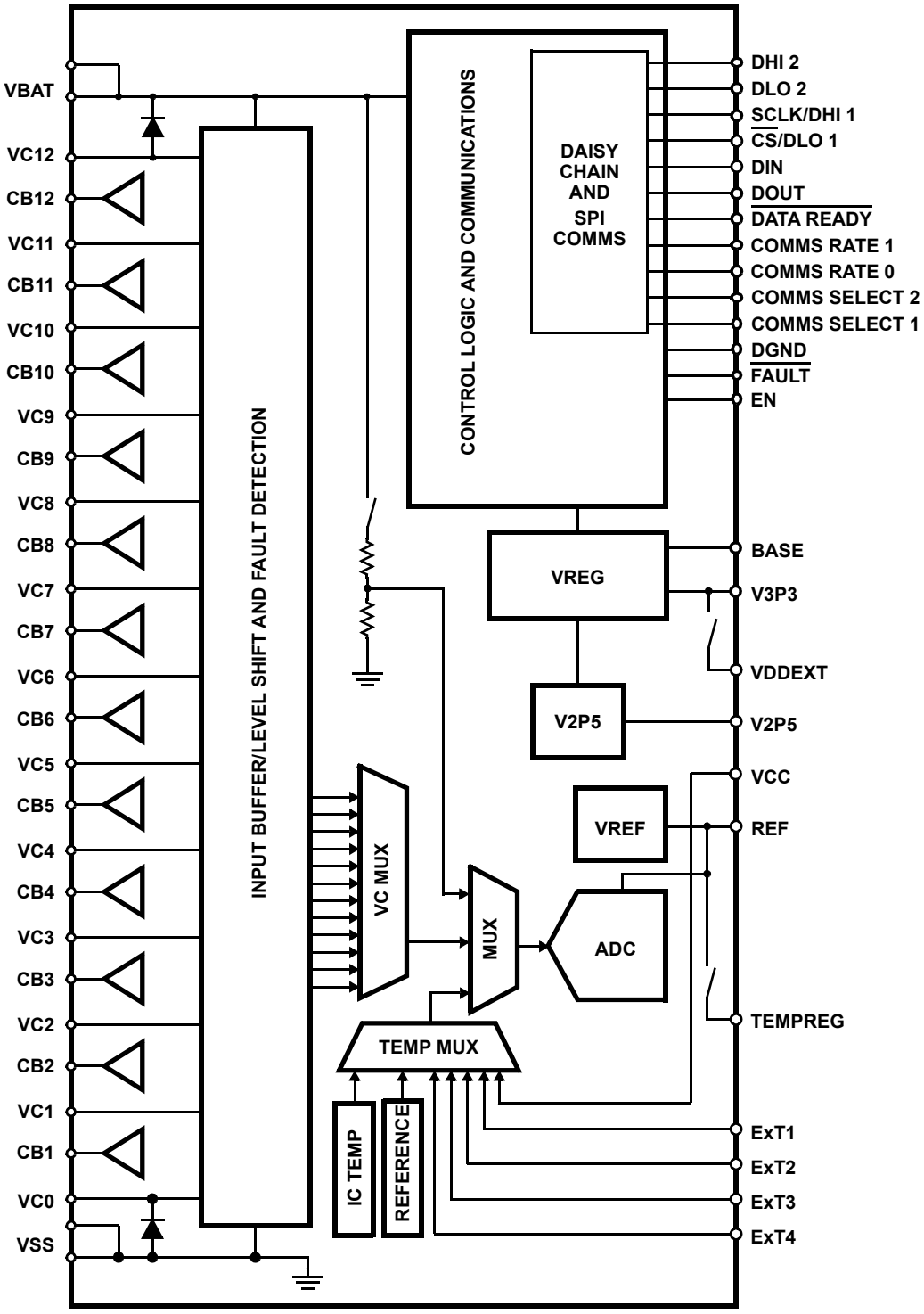


Figure 2. Block Diagram

1.2 Ordering Information

Part Number (Note 2, Note 3)	Part Marking	Trim Voltage, V_{NOM} (V)	Temp. Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL78600ANZ	ISL78600ANZ	3.3	-40 to +105	-	64 Ld TQFP	Q64.10x10D
ISL78600ANZ-T	ISL78600ANZ	3.3	-40 to +105	1k	64 Ld TQFP	Q64.10x10D
ISL78600EVKIT1Z	Evaluation Kit					

Notes:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL78600 product information page. For more information about handling and processing moisture sensitive devices, see TB363.

Table 1. Product Family

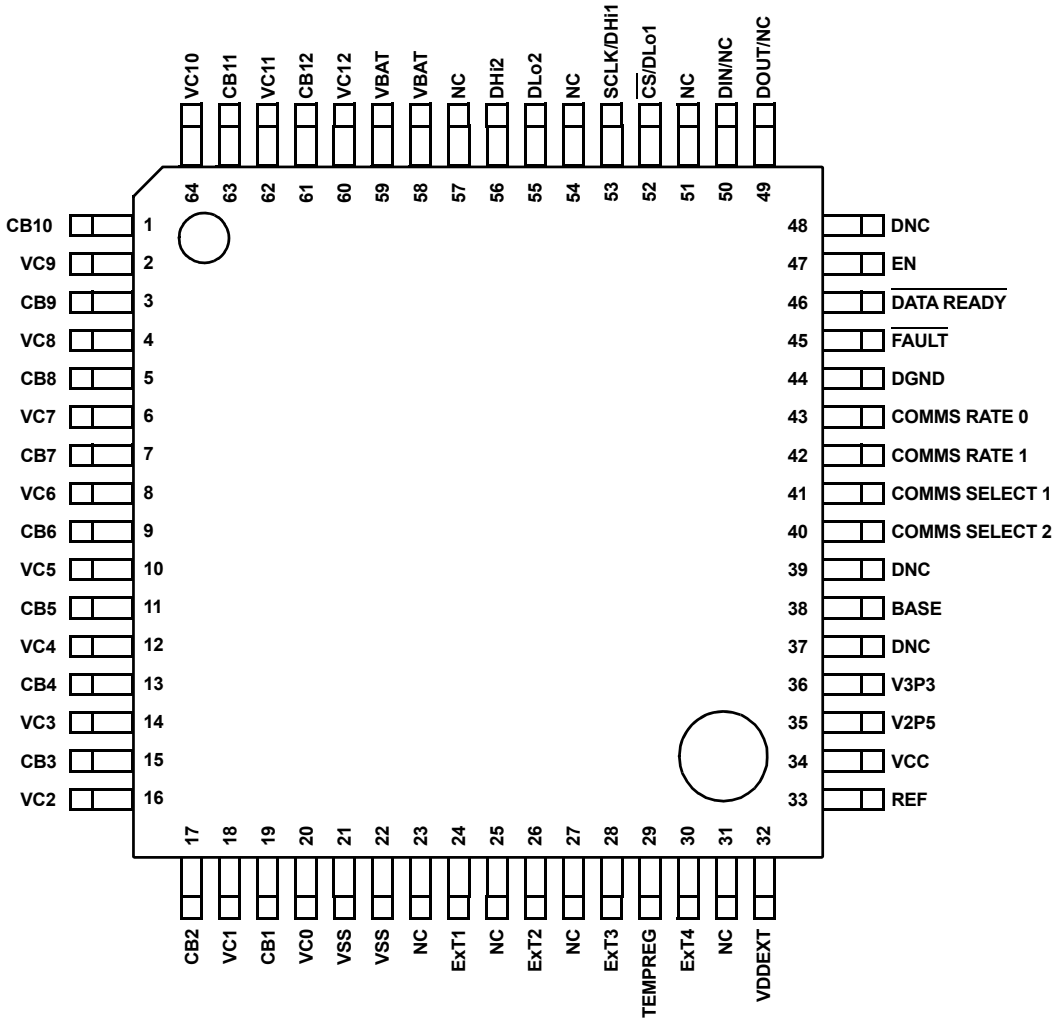
Part Number	Maximum Initial Cell Voltage Monitor Error (Note 4)
ISL78600	2.0mV
ISL78610	10.0mV

Note:

4. Conditions: Temperature = -20°C to +60°C, V_{CELL} = 2.6V to 4.0V, limits applied to a ±3 sigma distribution.

1.3 Pin Configuration

(64 Ld 10x10 TQFP)
Top View



1.4 Pin Descriptions

Pin Name	Pin Number	Description
VC0, VC1, VC2, VC3, VC4, VC5, VC6, VC7, VC8, VC9, VC10, VC11, VC12	20, 18, 16, 14, 12, 10, 8, 6, 4, 2, 64, 62, 60	Battery cell voltage inputs. VCn connects to the positive terminal of CELLn and the negative terminal of CELLn+1. (VC12 connects only to the positive terminal of CELL12 and VC0 only connects with the negative terminal of CELL1.)
CB1, CB2, CB3, CB4, CB5, CB6, CB7, CB8, CB9, CB10, CB11, CB12	19, 17, 15, 13, 11, 9, 7, 5, 3, 1, 63, 61	Cell Balancing FET control outputs. Each output controls an external FET, which provides a current path around the cell for balancing.
VBAT	58, 59	Main IC supply pins. Connect to the most positive terminal in the battery string.
VSS	21, 22	Ground. These pins connect to the most negative terminal in the battery string.
ExT1, ExT2, ExT3, ExT4	24, 26, 28, 30	External temperature monitor or general purpose inputs. The temperature inputs are intended for use with external resistor networks using NTC type thermistor sense elements but can also be used as general purpose analog inputs at the user's discretion. 0V to 2.5V input range.
TEMPREG	29	Temperature monitor voltage regulator output. This switched 2.5V output supplies a reference voltage to external NTC thermistor circuits to provide ratiometric ADC inputs for temperature measurement.

Pin Name	Pin Number	Description
VDDEXT	32	External V3P3 supply input/output. Connected to the V3P3 pin through a switch, this pin can be used to power external circuits from the V3P3 supply. The switch is open when the ISL78600 is placed in Sleep mode.
REF	33	2.5V voltage reference decoupling pin. Connect a 2.0µF to 2.5µF X7R capacitor to VSS. Do not connect any additional external load to this pin.
VCC	34	Analog supply voltage input. Connect to V3P3 through a 33Ω resistor. Connect a 1µF capacitor to ground.
V2P5	35	Internal 2.5V digital supply decoupling pin. Connect a 1µF capacitor to DGND.
V3P3	36	3.3V digital supply voltage input. Connect the emitter of the external NPN regulator transistor to this pin. Connect a 1µF capacitor to DGND.
BASE	38	Regulator control pin. Connect the external NPN transistor's base. Do not let this pin float.
DNC	37, 39, 48	Do not connect. Leave pins floating.
COMMS SELECT 1	41	Communications Port 1 mode select pin. Connect to V3P3 through a 1kΩ resistor for daisy chain communications on Port 1 or to DGND for SPI operation on Port 1.
COMMS SELECT 2	40	Communications Port 2 mode select pin. Connect to V3P3 through a 1kΩ resistor to enable Port 2 or to DGND to disable this port.
COMMS RATE 0, COMMS RATE 1	43, 42	Daisy chain communications data rate setting. Connect to DGND ('0') or to V3P3 ('1') through a 1kΩ resistor to select between various communication data rates.
DGND	44	Digital ground.
FAULT	45	Logic fault output. Asserted low if a fault condition exists.
DATA READY	46	SPI data ready. Asserted low when the device is ready to transmit data to the host microcontroller.
EN	47	Enable input. Tie to V3P3 to enable the part, then the device is ready after a delay of t_{PUD} ("Power-Up Specifications" on page 13). Tie to DGND to disable (all IC functions are turned off).
DOUT/NC	49	Serial data output (SPI) or NC (daisy chain). 0V to 3.3V push-pull output.
DIN/NC	50	Serial data input (SPI) or NC (daisy chain). 0V to 3.3V input.
$\overline{CS}$/DLo1	52	Chip-Select, active low 3.3V input (SPI) or daisy chain Port 1 Low connection.
SCLK/DHi1	53	Serial-clock input (SPI) or daisy chain Port 1 High connection.
DHi2	56	Daisy chain Port 2 High connection.
DLo2	55	Daisy chain Port 2 Low connection.
NC	23, 25, 27, 31, 51, 54, 57	No internal connection.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Voltage Relative to VSS, unless otherwise specified			
VBAT	-0.5	63	V
DHi1, DLo1, DHi2, DLo2,	-0.5	VBAT + 0.5	V
VCn (for n= 0 to 12)	-0.5	VBAT + 0.5	V
CBn (for n= 1 to 12)	-0.5	VBAT + 0.5	V
VC12	-0.5	63	V
VC11	-0.5	63	V
VC10	-0.5	63	V
VC9	-0.5	54	V
VC8	-0.5	45	V
VC7	-0.5	45	V
VC6	-0.5	36	V
VC5	-0.5	36	V
VC4	-0.5	27	V
VC3	-0.5	27	V
VC2	-0.5	18	V
VC1	-0.5	18	V
VC0	-0.5	9	V
CBn (for n= 1 to 9)	V(VCn-1) - 0.5	V(VCn-1) + 9	V
CBn (for n= 10 to 12)	V(VCn) - 9	V(VCn) + 0.5	V
BASE, DIN, SCLK, $\overline{CS}$, DOUT, $\overline{DATA\ READY}$, COMMS SELECT n, TEMPREG, REF, V3P3, VCC, $\overline{FAULT}$, COMMS RATE n, EN, VDDEXT	- 0.2	5.5	V
ExTn	- 0.2	4.1	V
V2P5	- 0.2	2.9	V
Note: DOUT, $\overline{DATA\ READY}$, and $\overline{FAULT}$ are digital outputs and should not be driven from external sources. V2P5, REF, TEMPREG and BASE are analog outputs and should not be driven from external sources.			

ESD Rating	Value	Unit
Human Body Model (Tested per AECQ100-002)	2	kV
Capacitive Discharge Model (Tested per AECQ100-011)	2	kV
Latch-Up (Tested per AEC-Q100-004; Class 2, Level A)	100	mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
64 Ld TQFP Package (Notes 5, 6)	42	9

Notes:

5. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379.
6. For θ_{JC}, the “case temp” location is taken at the package top center.

Parameter	Minimum	Maximum	Unit
Maximum Continuous Package Power Dissipation		400	mW
Storage Temperature	-55	+125	°C
Maximum Operating Junction Temperature		+125	°C
Pb-Free Reflow Profile	See TB493.		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Voltage Relative to VSS, Unless Otherwise Specified			
T_A, Ambient Temperature Range	-40	+105	°C
VBAT	6	60	V
VBAT (for Daisy Chain operation)	10	60	V
VCn - VC(n-1) (for n = 1 to 12)	-0.1	5.0	V
VC0	-0.1	+0.1	V
CBn - VC(n-1) (for n = 1 to 9)	-0.5	9.0	V
CBn - VC(n-1) (for n = 10 to 12)	-9.0	0.5	V
VC5, VC6	-0.5	36	V
DIN, SCLK, $\overline{CS}$, COMMS SELECT 1, COMMS SELECT 2, V3P3, VCC, COMMS RATE 0, COMMS RATE 1, EN	0	3.6	V
ExT1, ExT2, ExT3, ExT4 Input Voltage	0	2.5	V

2.4 Electrical Specifications

V_{BAT} = 6 to 60V, T_A = -20°C to +60°C, unless otherwise specified. Biasing setup as in Figure 45 on page 34 or equivalent.

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Measurement Specifications						
Cell Voltage Input Measurement Range	V_{CELL}	VC(n) - VC(n-1), for design reference.	- 0.3		5	V
Cell Monitor Voltage Resolution	$V_{CELLRES}$	[VC(n) - VC(n-1)] LSB step size (13-bit signed number), 5V full scale value		0.61		mV

V_{BAT} = 6 to 60V, T_A = -20°C to +60°C, unless otherwise specified. Biasing setup as in Figure 45 on page 34 or equivalent. **(Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
ISL78600 Initial Cell Monitor Voltage Error (Note 9) V_{NOM} = Nominal calibration voltage Note: Cell measurement accuracy figures assume a fixed 1kΩ resistor is placed in series with each VCn pin (n = 0 to 12). See ""Performance Characteristics" on page 20	ΔV_{CELL}	$V_{CELL} = V_{NOM}$ - 0.3V < $V_{CELL} < V_{NOM}$ + 0.3V	-2.5		2.5	mV
		$V_{CELL} = V_{NOM}$ - 0.7V < $V_{CELL} < V_{NOM}$ + 0.7V	-3.5		3.5	mV
		-40°C to +85°C (Note 8)	-7.5		7.5	mV
		-40°C to +105°C (Note 8)	-8.5		8.5	mV
		V_{CELL} = 4.95	-8.0		8.0	mV
		-40°C to +85°C (Note 8)	-11.0		11.0	mV
		-40°C to +105°C (Note 8)	-11.0		11.0	mV
		V_{CELL} = 0.5	-12.0		12.0	mV
		-40°C to +85°C (Note 8)	-18.0		18.0	mV
		-40°C to +105°C (Note 8)	-20.0		20.0	mV
Cell Input Current Note: Cell accuracy figures assume a fixed 1kΩ resistor is placed in series with each VCn pin (n = 0 to 12)	I_{VCELL}	VC0 Input				
		VC0 ≥ 0.5 and VC0 ≤ 4.0V	-1.5	-1	-0.5	µA
		VC0 > 4.0V	-1.75		-0.50	µA
		-40°C to +105°C (Note 8)	-2.0	-1	-0.5	µA
		VC1, VC2, VC3 Inputs				
		VCn - VC(n-1) ≥ 0.5 and VCn - VC(n-1) ≤ 4.0V	-2.7	-2	-1.3	µA
		VCn - VC(n-1) > 4.0V	-2.85		-1.00	µA
		-40°C to +105°C (Note 8)	-3.0	-2	-1.0	µA
		VC4 Input				
		VCn - VC(n-1) ≥ 0.5 and VCn - VC(n-1) ≤ 4.0V	-0.6	0	0.6	µA
		VCn - VC(n-1) > 4.0V	-0.7		0.7	µA
		-40°C to +105°C (Note 8)	- 0.8	0	0.8	µA
		VC5, VC6, VC7, VC8, VC9, VC10, VC11 inputs				
		VCn - VC(n-1) < 2.6V	0.5	2	2.7	µA
		VCn - VC(n-1) ≥ 2.6V and VCn - VC(n-1) ≤ 4.0V	1.5	2	2.7	µA
		VCn - VC(n-1) > 4.0V	1.50	2	2.85	µA
		-40°C to +105°C (Note 8)	0.5	2	3.0	µA
		VC12 Input				
		VC12 - VC11 ≥ 0.5 and VC12 - C11 ≤ 4.0V	0.6	1	1.7	µA
		VC12 - VC11 > 4.0V	0.60		1.75	µA
		-40°C to +105°C (Note 8)	0.6	1	2.0	µA
V_{BAT} Monitor Voltage Resolution	$VBAT_{RES}$	ADC resolution referred to input (V_{BAT}) level. 14-bit unsigned number. Full scale value = 79.67V.		4.863		mV
Initial V_{BAT} monitor Voltage Error (Note 9)	ΔV_{BAT}	Measured at V_{BAT} = 36V to 43.2V	-100		100	mV
		Measured at V_{BAT} = 31.2V to 48V	-125		125	mV
		Measured at V_{BAT} = 6V to 59.4V	-320		322	mV
		Measured at V_{BAT} = 6V to 59.4V -40°C to +105°C (Note 8)	-490		490	mV
External Temperature Monitoring Regulator	V_{TEMP}	Voltage on TEMPREG output. (0 to 2mA load)	2.475	2.500	2.525	V

V_{BAT} = 6 to 60V, T_A = -20°C to +60°C, unless otherwise specified. Biasing setup as in Figure 45 on page 34 or equivalent. **(Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
External Temperature Output Impedance	R_{TEMP}	Output Impedance at TEMPREG pin. (Note 8)	0	0.1	0.2	Ω
External Temperature Input Range	V_{EXT}	Effective ExTn input voltage range. For design reference. This is the input voltage range that does not trigger an open input condition.	0		2344	mV
External Temperature Input Pull-Up	$R_{EXTTEMP}$	Pull-up resistor to $V_{TEMPREG}$ applied to each input during measurement		10		MΩ
External Temperature Input Offset	V_{EXTOFF}	V_{BAT} = 39.6V	-7.0		7.0	mV
		V_{BAT} = 39.6V, -40°C to +105°C (Note 8)	-10		10	mV
External Temperature Input INL	V_{EXTINL}	(Note 8)		±0.61		mV
External Temperature Input Gain Error	V_{EXTG}	Error at 2.5V input	-7.5		11	mV
		-40°C to +105°C (Note 8)	-8		18.5	mV
Internal Temperature Monitor Error	V_{INTMON}			±10		°C
Internal Temperature Monitor Resolution	T_{INTRES}	Output resolution (LSB/°C), 14-bit number		31.9		LSB/°C
Internal Temperature Monitor Output	T_{INT25}	Output count at +25°C		9180		Decimal
Power-Up Specifications						
Power-Up Condition Threshold	V_{POR}	V_{BAT} voltage (rising)	4.8	5.1	5.6	V
Power-Up Condition Hysteresis	V_{PORhys}			460		mV
Initial Power-Up Delay	t_{POR}	Time after VPOR condition V_{REF} from 0V to 0.95 x V_{REF}(nominal) (EN tied to V3P3) Device can now communicate			27.125	ms
Enable Pin Power-Up Delay	t_{PUD}	Delay after EN = 1 to V_{REF} from 0V to 0.95 x V_{REF}(nominal) (V_{BAT} = 39.6V) - Device can now communicate			27.125	ms

V_{BAT} = 6 to 60V, T_A = -20°C to +60°C, unless otherwise specified. Biasing setup as in Figure 45 on page 34 or equivalent. **(Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Supply Current Specifications						
V_{BAT} Supply Current	I_{VBAT}	Non-daisy chain configuration. Device enabled. No communications, ADC, measurement, balancing, or open-wire detection activity.				
		6V		70	90	µA
		39.6V		73	95	µA
		60V		73	96	µA
		-40°C to +105°C (Note 8)			105	µA
	$I_{VBATMASTER}$	Daisy chain configuration – master device. Enabled. No communications, ADC, measurement, balancing, or open-wire detection activity.				
		6V	400	550	660	µA
		39.6V	500	650	900	µA
		60V	550	710	1000	µA
		-40°C to +105°C (Note 8)			1150	µA
		Peak current when daisy chain transmitting		18		mA
	$I_{VBATMID}$	Daisy chain configuration – Middle stack device. Enabled. No communications, ADC, measurement, balancing, or open-wire detection activity.				
		6V	700	1020	1210	µA
		39.6V	900	1210	1560	µA
		60V	1000	1340	1700	µA
		-40°C to +105°C (Note 8)			1850	µA
		Peak current when daisy chain transmitting		18		mA
	$I_{VBATTOP}$	Daisy chain configuration – top device. Enabled. No communications, ADC, measurement, balancing, or open-wire detection activity.				
		6V	400	550	660	µA
		39.6V	500	650	900	µA
		60V	550	710	1000	µA
		-40°C to +105°C (Note 8)			1150	µA
		Peak current when daisy chain transmitting		18		mA
	$I_{VBATSLEEP1}$ (Note 8)	Sleep mode (EN = 1, daisy chain configuration)				
		6V	13	28	44	µA
		39.6V	18	33	48	µA
		60V	20	35	50	µA
		-40°C to +105°C			120	µA
	$I_{VBATSLEEP2}$ (Note 8)	Sleep mode (EN = 1, stand-alone, non-daisy chain)	13.2	19	34.1	µA
		-40°C to +105°C	13.5		109	µA
	$I_{VBATSHDN}$ (Note 8)	Shutdown. device “off” (EN = 0) (Daisy chain and non-daisy chain configurations)				
		6V	6	13	28	µA
		39.6V	7	15	29	µA
		60V	7	16	30	µA
		-40°C to +105°C			101	µA

V_{BAT} = 6 to 60V, T_A = -20°C to +60°C, unless otherwise specified. Biasing setup as in Figure 45 on page 34 or equivalent. **(Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
V_{BAT} Supply Current Tracking, Sleep Mode	$I_{VBAT\Delta SLEEP}$ (Note 8)	EN = 1, daisy chain sleep mode configuration. V_{BAT} current difference between any two devices operating at the same temperature and supply voltage.	0		18	µA
		-40°C to +105°C	0		56	µA
V_{BAT} Incremental Supply Current, Balancing	$I_{VBATBAL}$	All balancing circuits on. Incremental current: Add to non-balancing V_{BAT} current. V_{BAT} = 39.6V	250	300	350	µA
		-40°C to +105°C (Note 8)	200	300	400	µA
V3P3 Regulator Voltage (Normal)	V_{3P3N}	EN = 1, Load current range 0 to 5mA. V_{BAT} = 39.6V	3.25	3.35	3.45	V
		-40°C to +105°C (Note 8)	3.2		3.5	V
V3P3 Regulator Voltage (Sleep)	V_{3P3S}	EN = 1, Load current range. No load. (SLEEP). V_{BAT} = 39.6V		2.8		V
V3P3 Regulator Control Current	I_{BASE}	Current sourced from BASE output. V_{BAT} = 6V	1			mA
		-40°C to +105°C (Note 8)	1			mA
V3P3 Supply Current	I_{V3P3}	Device enabled No measurement activity, Normal mode	0.8	1	1.2	mA
		-40°C to +105°C (Note 8)	0.8		1.3	mA
V_{REF} Reference Voltage	V_{REF}	EN = 1, no load, normal mode		2.5		V
VDDEXT Switch Resistance	R_{VDDEXT}	Switch “ON” resistance, V_{BAT} = 39.6V		12		Ω
		-40°C to +105°C (Note 8)	5		22	Ω
V_{CC} Supply Current	I_{VCC}	Device enabled (EN = 1). Stand-alone or daisy configuration. No ADC or daisy chain communications active.	2.00	3.25	4.50	mA
		-40°C to +105°C (Note 8)	2.0		5.0	mA
	$I_{VCCACTIVE1}$	Device enabled (EN = 1). Stand-alone or daisy configuration. average current during 16ms scan continuous operation. V_{BAT} = 39.6V		6.0		mA
	$I_{VCCSLEEP}$	Device enabled (EN = 1). Sleep mode. V_{BAT} = 39.6V		0.5		µA
	$I_{VCCSHDN}$	Device disabled (EN = 0). Shutdown mode.	0	0.5	3.5	µA
		-40°C to +105°C (Note 8)			9.0	µA
Over-Temperature Protection Specifications						
Internal Temperature Limit Threshold	T_{INTSD}	Balance stops and auto scan stops. Temperature rising or falling.		150		°C
External Temperature Limit Threshold	T_{XT}	Corresponding to 0V (minimum) and $V_{TEMPREG}$ (maximum) External temperature input voltages higher than 15/16 $V_{TEMPREG}$ are registered as open input faults.	0		16383	Decimal
Cell Over and Undervoltage Test Specifications						
Undervoltage Threshold	V_{UV}	Programmable. Corresponding to 0V (minimum) and 5V (maximum)	0		8191	Decimal
Overvoltage Threshold	V_{OV}	Programmable. Corresponding to 0V (minimum) and 5V (maximum)	0		8191	Decimal

V_{BAT} = 6 to 60V, T_A = -20°C to +60°C, unless otherwise specified. Biasing setup as in Figure 45 on page 34 or equivalent. **(Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Voltage Reference/Oscillator Check Specifications						
V3P3 Power-Good Window	V_{3PH}	3.3V power-good window high threshold. V_{BAT} = 39.6V	3.79	3.89	3.99	V
		-40°C to +105°C (Note 8)	3.70		4.05	V
	V_{3PL}	3.3V power-good window low threshold. V_{BAT} = 39.6V	2.54	2.64	2.71	V
		-40°C to +105°C (Note 8)	2.5		2.8	V
V2P5 Power-Good Window	V_{2PH}	2.5V power-good window high threshold. V_{BAT} = 39.6V	2.65	2.70	2.90	V
		-40°C to +105°C (Note 8)	2.53		2.90	V
	V_{2PL} (Note 8)	2.5V power-good window low threshold. V_{BAT} = 39.6V	1.85	2.03	2.24	V
		-40°C to +105°C	1.76		2.28	V
V_{CC} Power-Good Window	V_{VCCH}	VCC power-good window high threshold. V_{BAT} = 39.6V	3.60	3.74	3.90	V
		-40°C to +105°C (Note 8)	3.6		4.0	V
	V_{VCCL}	VCC power-good window low threshold. V_{BAT} = 39.6V	2.6	2.7	2.8	V
		-40°C to +105°C (Note 8)	2.55		2.85	V
V_{REF} Power-Good Window	V_{RPH}	V_{REF} power-good window high threshold. V_{BAT} = 39.6V	2.525	2.700	2.900	V
		-40°C to +105°C (Note 8)	2.525		2.900	V
	V_{RPL}	V_{REF} power-good window low threshold. V_{BAT} = 39.6V	2.150	2.300	2.465	V
		-40°C to +105°C (Note 8)	2.0		2.4	V
V_{REF} Secondary Reference Accuracy Test	V_{RACC}	V_{REF} value calculated using stored coefficients. V_{BAT} = 39.6V ("Voltage Reference Check Calculation" on page 110)	2.488	2.500	2.512	V
Voltage Reference Check Timeout	t_{VREF}	Time to check voltage reference value from power-on, enable, or wakeup		20		ms
Oscillator Check Timeout	t_{OSC}	Time to check main oscillator frequency from power-on, enable, or wakeup		20		ms
Oscillator Check Filter Time	t_{OSCF}	Minimum duration of fault required for detection		100		ms
Cell Open-Wire Detection (See "Scan Wires Command" on page 54 and "Open-Wire Test" on page 102.)						
Open-Wire Current	I_{OW}	ISCN bit = 0; V_{BAT} = 39.6V	0.125	0.150	0.185	mA
		ISCN bit = 1; V_{BAT} = 39.6V	0.85	1.00	1.15	mA
Open-Wire Detection Time	t_{OW}	Open-wire current source "on" time		4.6		ms
Open VC0 Detection Threshold	V_{VC0}	CELL1 negative terminal (with respect to VSS) V_{BAT} = 39.6V (Note 8)	1.2	1.5	1.8	V
Open VC1 Detection Threshold	V_{VC1}	CELL1 positive terminal (with respect to VSS) V_{BAT} = 39.6V (Note 8)	0.6	0.7	0.8	V
Primary Detection Threshold, VC2 to VC12	V_{VC2_12P}	V(VC(n - 1)) - V(VCn), n = 2 to 12 V_{BAT} = 39.6V (Note 8)	--1.5	-1.2	-0.9	V
Secondary Detection Threshold, VC2 to VC12	V_{VC2_12S}	Through ADC. VC2 to VC12 only V_{BAT} = 39.6V (Note 8)	-100	-39	10	mV
Open V_{BAT} Fault Detection Threshold	V_{VBO}	VC12 - V_{BAT}		200		mV

V_{BAT} = 6 to 60V, T_A = -20°C to +60°C, unless otherwise specified. Biasing setup as in Figure 45 on page 34 or equivalent. **(Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Open VSS Fault Detection Threshold	V_{VSSO}	VSS - VC0		250		mV
Cell Balance Output Specifications						
Cell Balance Pin Output Impedance	R_{CBL}	CBn output off impedance between CB(n) to VC(n-1): cells 1 to 9 and between CB(n) to VC(n): cells 10 to 12	2	4	5	MΩ
Cell Balance Output Current	I_{CBH1}	CBn output on. (CB1-CB9); V_{BAT} = 39.6V; device sinking current	-28	-25	-21	µA
	I_{CBH2}	CBn output on. (CB10-CB12); V_{BAT} = 39.6V; device sourcing current	21	25	28	µA
Cell Balance Output Leakage in Shutdown	I_{CBSD}	EN = GND. V_{BAT} = 39.6V	-500	10	700	nA
External Cell Balance FET Gate Voltage	VGS	CBn Output on; External 320kΩ between VCn and CBn (n = 10 to 12) and between CBn and VCn-1 (n = 1 to 9)	7.04	8.00	8.96	V
Internal Cell Balance Output Clamp	VCBCL	I_{CB} = 100µA	8.94			V
Logic Inputs: SCLK, $\overline{CS}$, DIN						
Low-Level Input Voltage	V_{IL}				0.8	V
High-Level Input Voltage	V_{IH}		1.75			V
Input Hysteresis	V_{HYS}	(Note 8)	100			mV
Input Current	I_{IN}	0V < V_{IN} < V3P3	-1		+1	µA
Input Capacitance (Note 8)	C_{IN}				10	pF
Logic Inputs: EN, COMMS SELECT1, COMMS SELECT2, COMMS RATE 0, COMMS RATE 1						
Low-Level Input Voltage	V_{IL}				0.3* V3P3	V
High-Level Input Voltage	V_{IH}		0.7* V3P3			V
Input Hysteresis	V_{HYS}	(Note 8)	0.05* V3P3			V
Input Current	I_{IN}	0V < V_{IN} < V3P3	-1		+1	µA
Input Capacitance (Note 8)	C_{IN}				10	pF
Logic Outputs: DOUT, $\overline{Fault}$, $\overline{Data\ Ready}$						
Low-Level Output Voltage	V_{OL1}	At 3mA sink current	0		0.4	V
	V_{OL2}	At 6mA sink current	0		0.6	V
High-Level Output Voltage	V_{OH1}	At 3mA source current	V3P3 –0.4		V3P3	V
	V_{OH2}	At 6mA source current	V3P3 –0.6		V3P3	V
SPI Interface Timing (See Figure 3 and Figure 4)						
SCLK Clock Frequency	f_{SCLK}				2	MHz
Pulse Width of Input Spikes Suppressed	t_{IN1}		50		200	ns
Enable Lead Time	t_{LEAD}	Chip select low to ready to receive clock data	200			ns
Clock High Time	t_{HIGH}	(Note 8)	200			ns
Clock Low Time	t_{LOW}	(Note 8)	200			ns

V_{BAT} = 6 to 60V, T_A = -20°C to +60°C, unless otherwise specified. Biasing setup as in Figure 45 on page 34 or equivalent. **(Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Enable Lag Time	t_{LAG}	Last data read clock edge to chip select high (Note 8)	250			ns
CHIP SELECT High Time	$t_{CS:WAIT}$	Minimum high time for $\overline{CS}$ between bytes	200			ns
Slave Access Time	t_A	Chip Select low to DOUT active. (Note 8)			200	ns
Data Valid Time	t_V	Clock low to DOUT valid			350	ns
Data Output Hold Time (Note 8)	t_{HO}	Data hold time after falling edge of SCLK	0			ns
DOUT Disable Time	t_{DIS}	DOUT disabled following rising edge of $\overline{CS}$ (Note 8)			240	ns
Data Setup Time	t_{SU}	Data input valid prior to rising edge of SCLK	100			ns
Data Input Hold Time	t_{HI}	Data input to remain valid following rising edge of SCLK	80			ns
$\overline{DATA\ READY}$ Stop Delay Time	$t_{DR:SP}$	Chip select high to $\overline{DATA\ READY}$ high		750		ns
$\overline{DATA\ READY}$ High Time	$t_{DR:WAIT}$	Time between bytes		1.0		µs
SPI Communications Timeout	$t_{SPI:TO}$	Time the $\overline{CS}$ remains high before SPI communications time out - requiring the start of a new command		100		µs
DOUT Rise Time	t_R	Up to 50pF load			30	ns
DOUT Fall Time	t_F	Up to 50pF load			30	ns
Daisy Chain Communications Interface: DHi1, DLo1, DHi2, DLo2						
Daisy Chain Clock Frequency		Comms Rate (0, 1) = 11	450	500	550	kHz
		Comms Rate (0, 1) = 10	225	250	275	kHz
		Comms Rate (0, 1) = 01	112.5	125	137.5	kHz
		Comms Rate (0, 1) = 00	56.25	62.5	68.75	kHz
Common-Mode Reference Voltage				$V_{BAT}/2$		V

Notes:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
8. These MIN and/or MAX values are based on characterization data and are not 100% tested.
9. Stresses may be induced in the ISL78600 during soldering or other high temperature events that affect measurement accuracy. Initial accuracy does not include effects due to this. See Figure 6 on page 21 for cell reading accuracy obtained after soldering to Renesas evaluation boards. When soldering the ISL78600 to a customized circuit board with a layout or construction significantly differing from the Renesas evaluation board, design verification tests should be applied to determine drift due to soldering and over lifetime.

2.5 Timing Diagrams

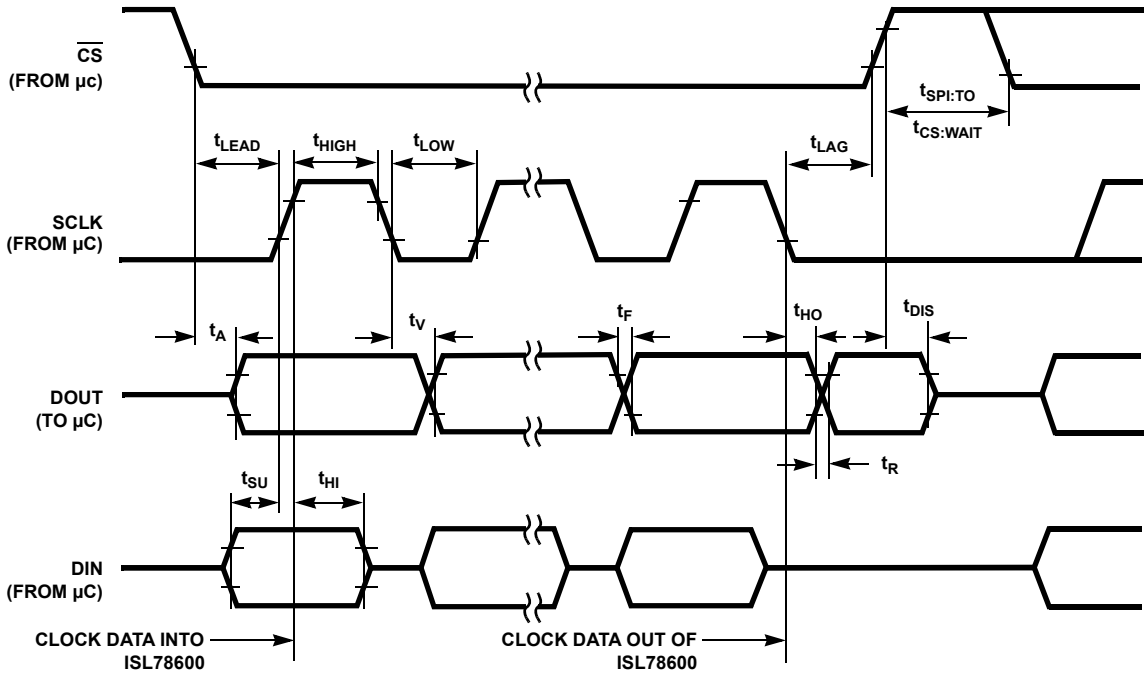


Figure 3. SPI Full Duplex (4-Wire) Interface Timing

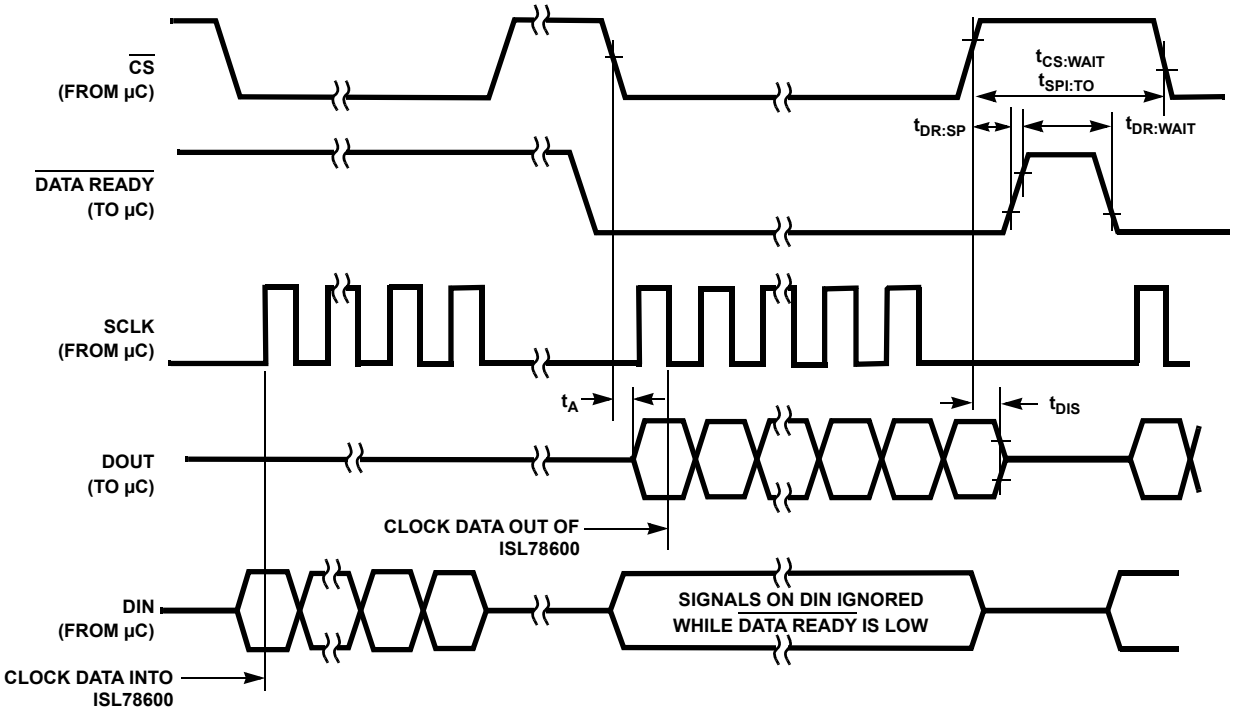


Figure 4. SPI Half Duplex (3-Wire) Interface Timing

2.6 Performance Characteristics

Table 2. Board Level Cell Voltage Reading Error (Cell Chemistry Ranges)

Parameter	Symbol	Test Conditions	Min (Note 10)	Typ	Max (Note 10)	Unit
ISL78600 Cell Monitor Voltage Error (Absolute)	ΔV_{CELLA}	VCELL = 3.25V at 25°C (± 3 sigma) (± 6 sigma)	 -0.9 -2.8	 1.01 1.01	 2.9 4.8	 mV
		VCELL = 1.65V to 2.85V (±3 sigma) -20°C to +60°C -40°C to +85°C -40°C to +105°C	 -1.8 -2.8 -4.6	 0.79 0.45 0.06	 3.4 3.7 4.7	 mV
		VCELL = 1.65V to 2.85V (±6 sigma) -20°C to +60°C -40°C to +85°C -40°C to +105°C	 -4.4 -6.1 -9.1	 0.79 0.45 0.06	 5.9 7.0 9.2	 mV
		VCELL = 2.5V to 3.65V (±3 sigma) -20°C to +60°C -40°C to +85°C -40°C to +105°C	 -1.4 -1.4 -2.9	 0.96 0.94 0.78	 2.9 3.3 3.0	 mV
		VCELL = 2.5V to 3.65V (±6 sigma) -20°C to +60°C -40°C to +85°C -40°C to +105°C	 -2.8 -3.8 -5.8	 0.96 0.94 0.78	 4.3 5.6 5.9	 mV
		VCELL = 2.5V to 4.3V (±3 sigma) -20°C to +60°C -40°C to +85°C -40°C to +105°C	 -1.7 -1.8 -3.3	 0.96 1.09 1.03	 3.3 4.0 3.4	 mV
		VCELL = 2.5V to 4.3V (±6 sigma) -20°C to +60°C -40°C to +85°C -40°C to +105°C	 -4.2 -4.6 -6.7	 0.96 1.09 1.03	 5.8 6.8 6.8	 mV
ISL78600 Initial V_{BAT} Reading Error (Absolute)	ΔV_{BAT}	Temperature = -20°C to +60°C V_{BAT} = 30V to 48V Limits applied to a ±3 sigma distribution Limits applied to a ±5 sigma distribution	 -51 -99	 27	 103 126	 mV
		Temperature = -20°C to +60°C V_{BAT} = 19.8V to 49V Limits applied to a ±3 sigma distribution Limits applied to a ±5 sigma distribution	 -78 -159	 36	 153 195	 mV
		Temperature = -40°C to +105°C V_{BAT} = 30V to 48V Limits applied to a ±3 sigma distribution Limits applied to a ±5 sigma distribution	 -71 -166	 12	 119 178	 mV
		Temperature = -40°C to +105°C V_{BAT} = 19.8V to 49V Limits applied to a ±3 sigma distribution Limits applied to a ±5 sigma distribution	 -92 -210	 18.5	 156 229	 mV
Voltage Reference Long Term Drift				-0.31		mV/ log(kHrs)

10. These distribution values are based on characterization of devices mounted on evaluation boards and are not 100% tested. Test performed approximately 30 days post assembly, individually stored in static free bags at room temperature until testing.

2.7 Typical Performance Curves

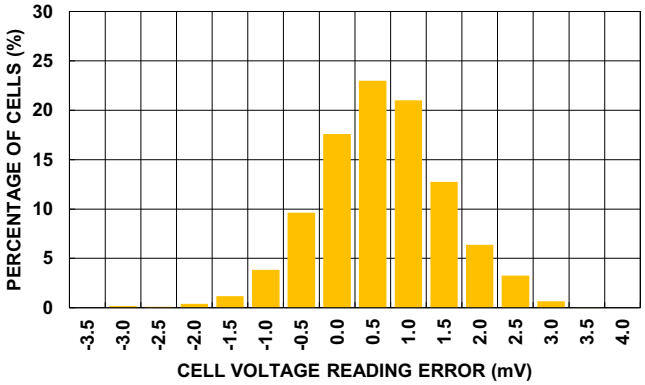


Figure 5. Cell Voltage Accuracy Histogram 1.65V to 4.3V, -20°C to +60°C

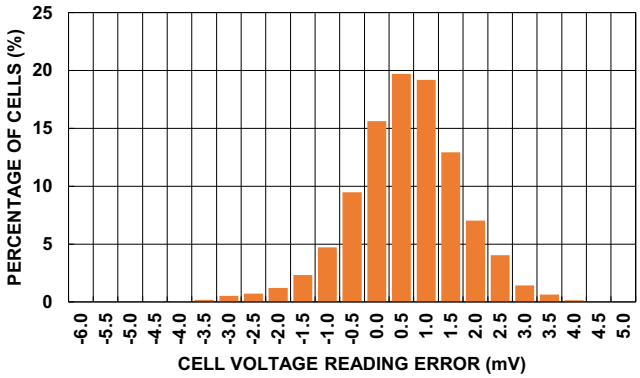


Figure 6. Cell Voltage Accuracy Histogram 1.65V to 4.3V, and -40°C to +85°C

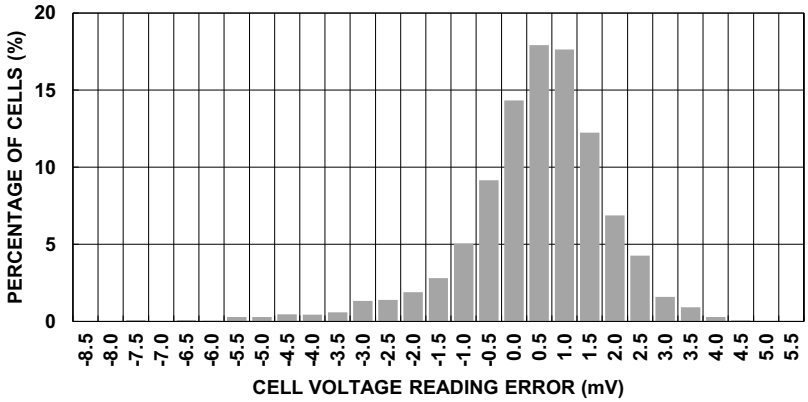


Figure 7. Cell Voltage Accuracy Histogram 1.65V to 4.3V, and -40°C to +105°C

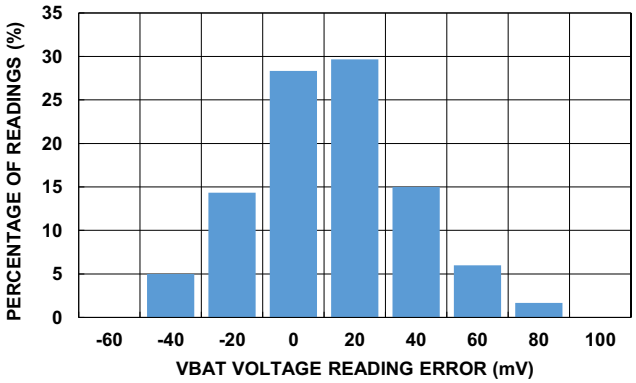


Figure 8. V_{BAT} Accuracy Histogram 30V to 48V; -40°C to +85°C

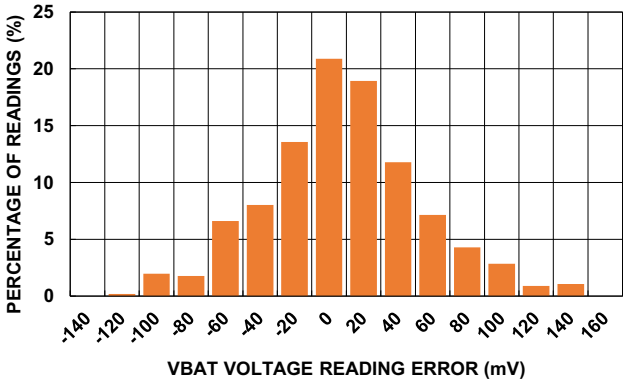


Figure 9. V_{BAT} Accuracy Histogram 19.8V to 49V; -40°C to +105°C

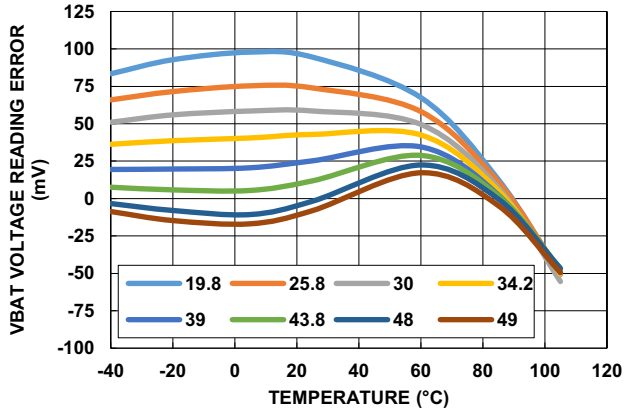


Figure 10. V_{BAT} Voltage Reading Error -40°C to +105°C

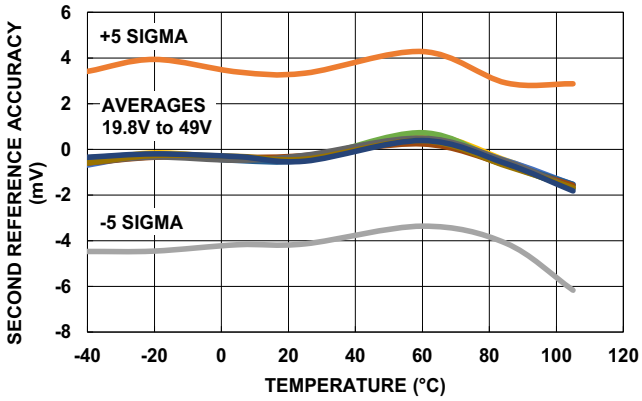


Figure 11. Second Reference Error vs Temperature V_{BAT} = 19.8V to 49V

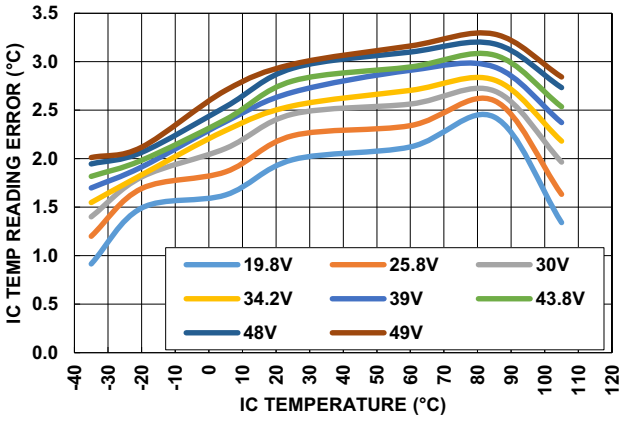


Figure 12. Internal Temperature Reading Accuracy vs Temperature

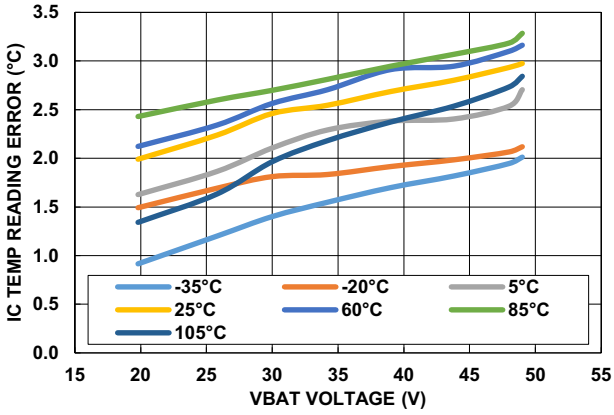


Figure 13. Internal Temperature Reading Accuracy vs Voltage

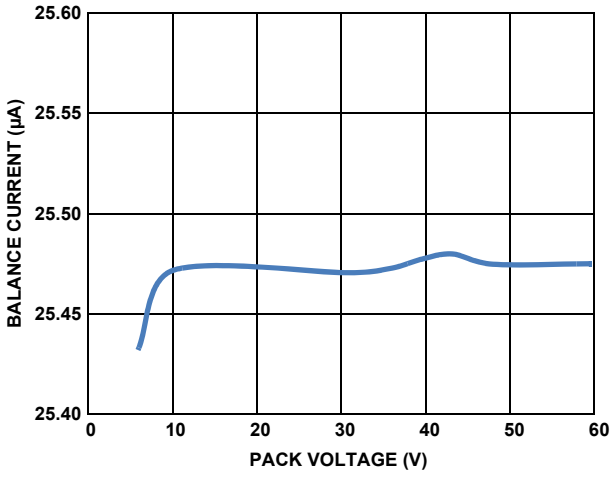


Figure 14. Balance Current vs. Pack Voltage

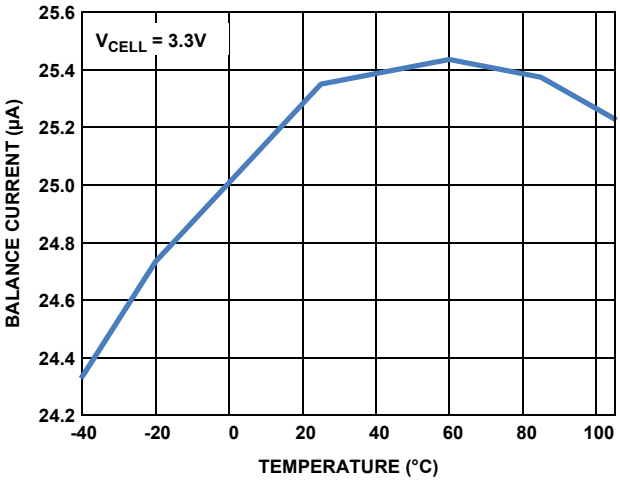


Figure 15. Balance Current vs. Temperature

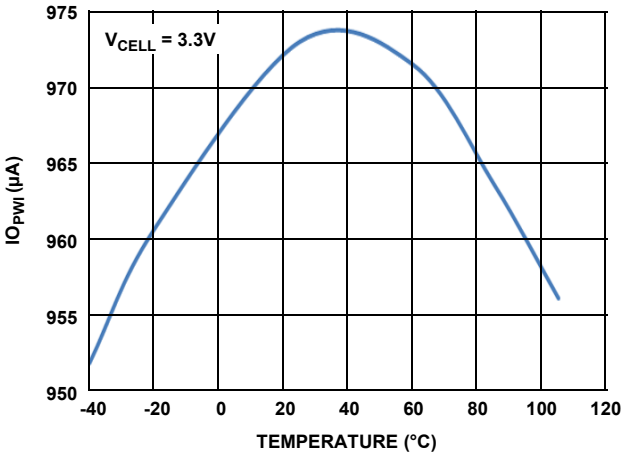


Figure 16. Open-Wire Test Current vs. Temperature (1mA Setting)

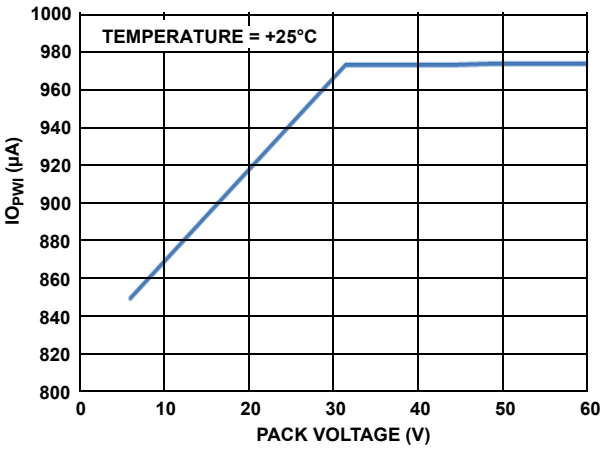


Figure 17. Open-Wire Test Current vs Pack Voltage (1mA Setting)

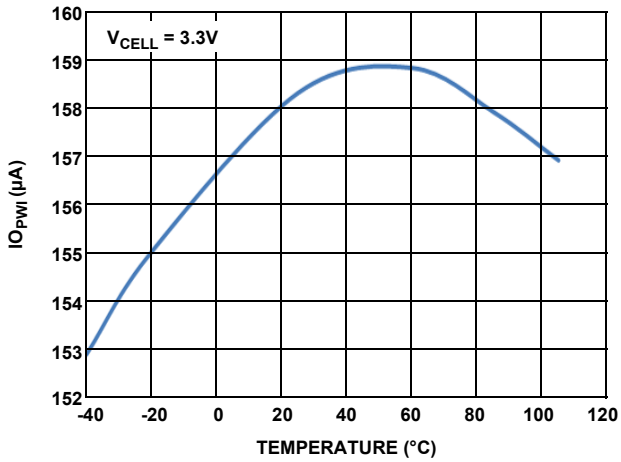


Figure 18. Open-Wire Test Current vs. Temperature (150µA Setting)

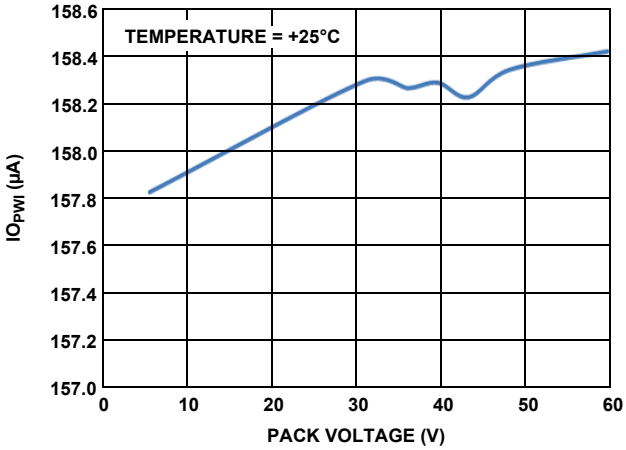


Figure 19. Open-Wire Test Current vs Pack Voltage (150µA Setting)

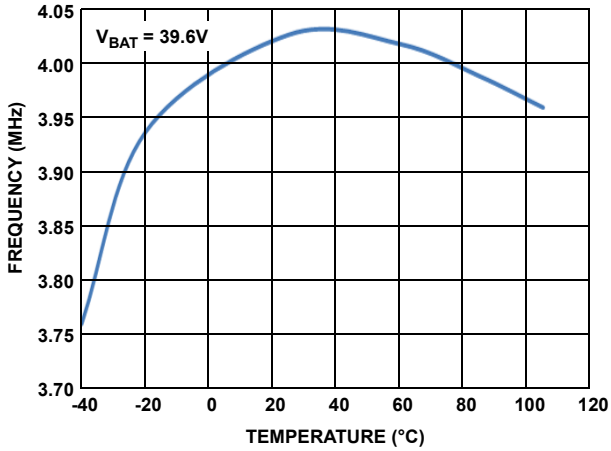


Figure 20. 4MHz Oscillator Frequency vs. Temperature

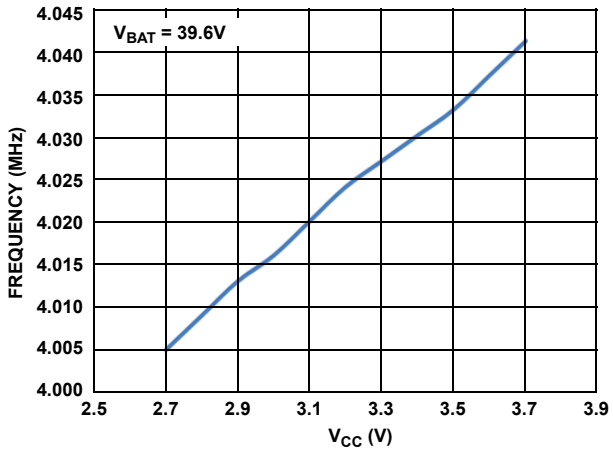


Figure 21. 4MHz Oscillator Frequency vs. V_{CC}

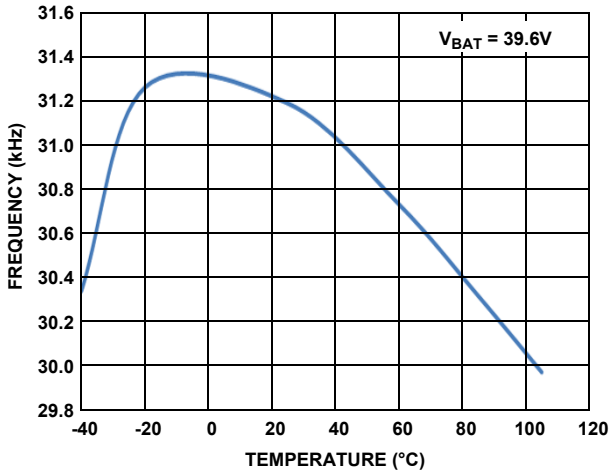


Figure 22. 32kHz Oscillator Frequency vs. Temperature

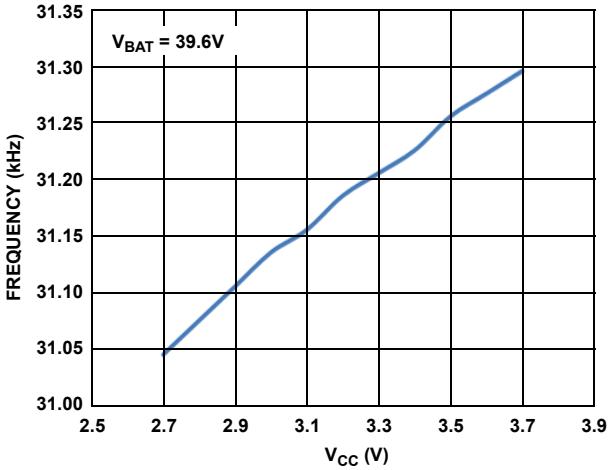


Figure 23. 32kHz Oscillator Frequency vs. V_{CC}

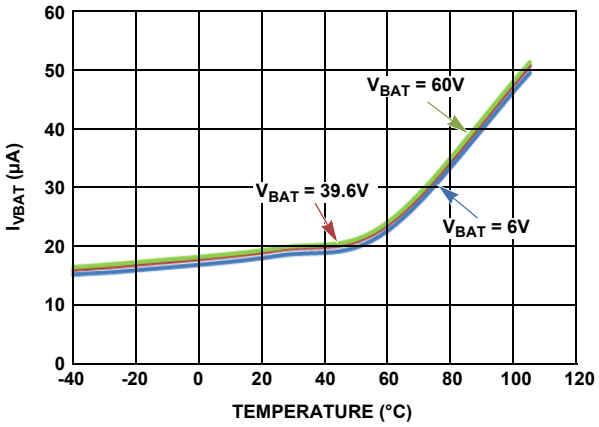


Figure 24. VBAT Sleep Current vs. Temperature (Standalone Mode) 6V, 39.6V, 60V

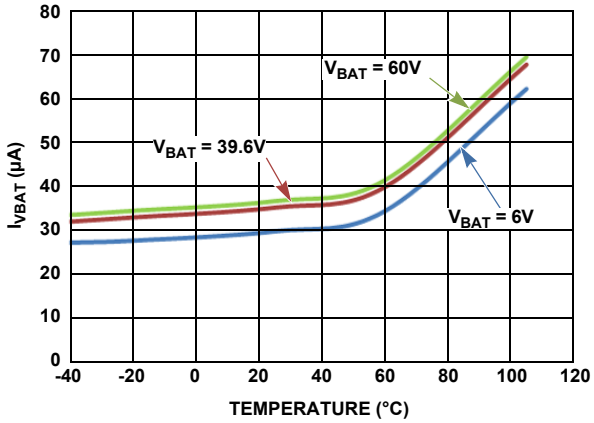


Figure 25. VBAT Sleep Current vs. Temperature (Daisy Chain Master) 6V, 39.6V, 60V

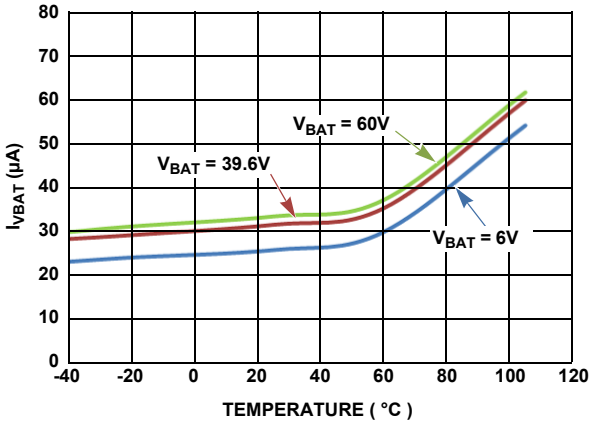


Figure 26. VBAT Sleep Current vs. Temperature (Daisy Chain Middle) 6V, 39.6V, 60V

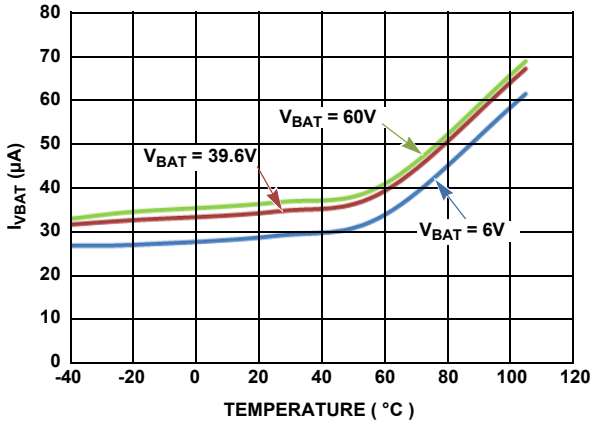


Figure 27. VBAT Sleep Current vs. Temperature (Daisy Chain Top) 6V, 39.6V, 60V

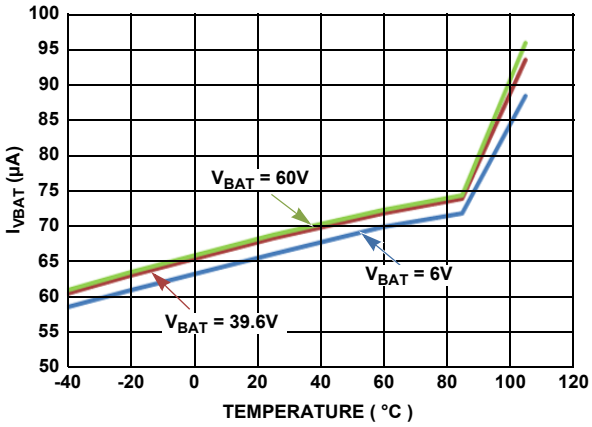


Figure 28. VBAT Supply Current vs. Temperature (Standalone Mode) 6V, 39.6V, 60V

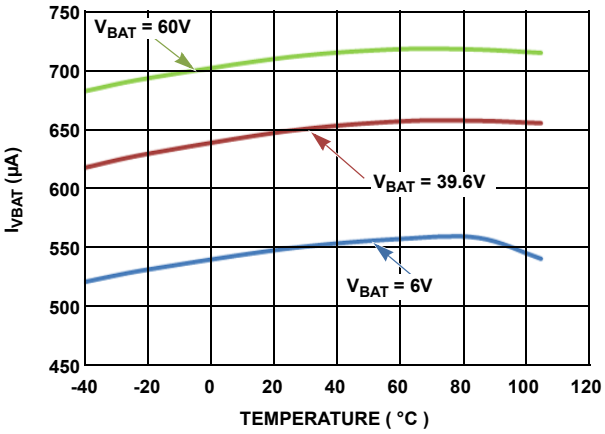


Figure 29. VBAT Supply Current vs. Temperature (Daisy Chain Master) 6V, 39.6V, 60V

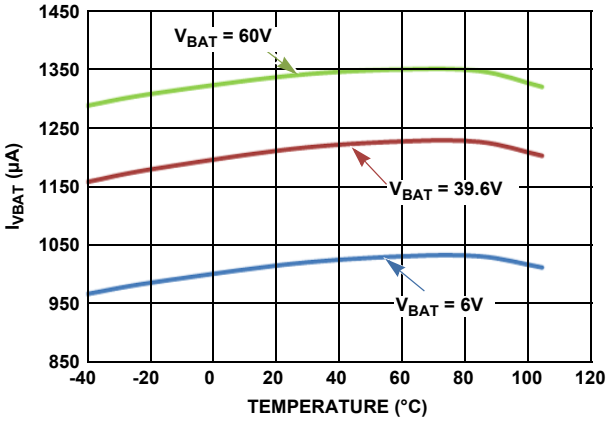


Figure 30. VBAT Supply Current vs. Temperature (Daisy Chain Middle) 6V, 39.6V, 60V

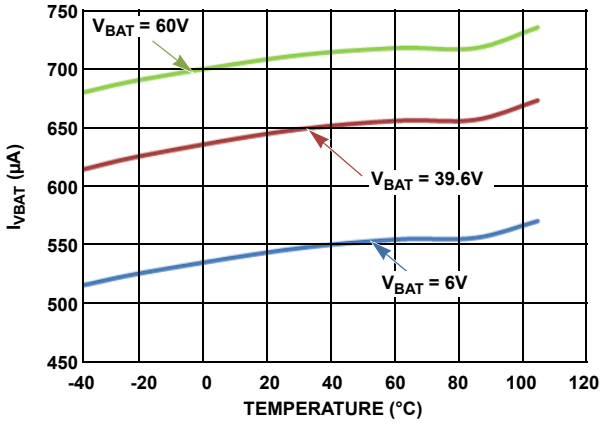


Figure 31. VBAT Supply Current vs. Temperature (Daisy Chain Top) 6V, 39.6V, 60V

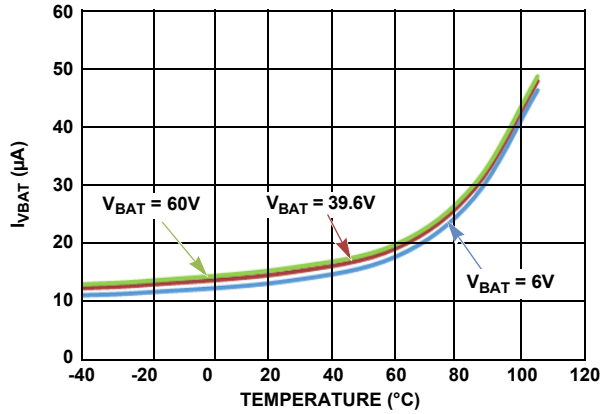


Figure 32. VBAT Shutdown Current vs. Temperature (EN = 0) 6V, 39.6V, 60V

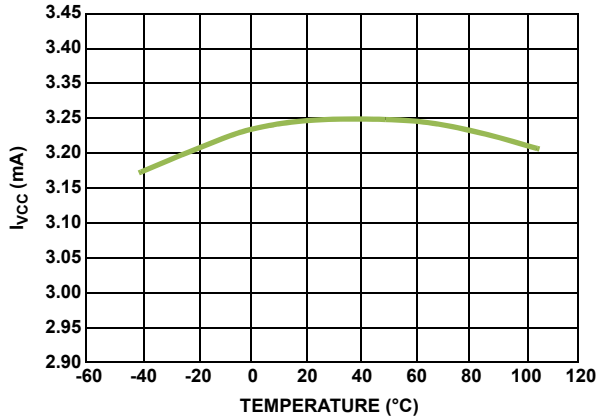


Figure 33. V_{CC} Supply Current vs. Temperature 6V, 39.6V, 60V

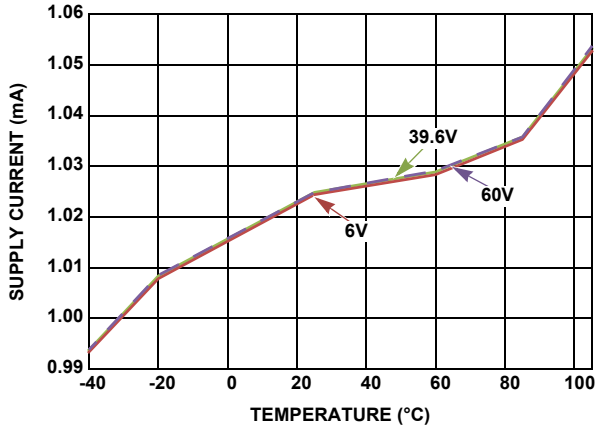


Figure 34. V_{3P3} Supply Current vs. Temperature 6V, 39.6V, 60V

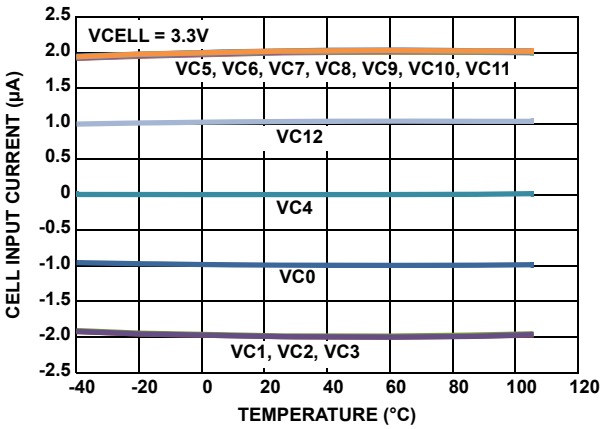


Figure 35. Cell Input Current vs. Temperature

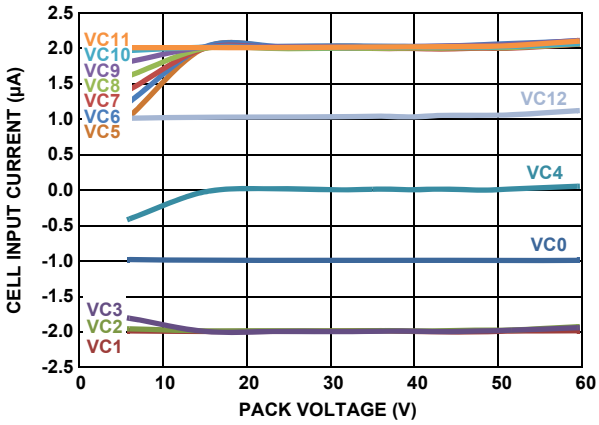


Figure 36. Cell Input Current vs. Pack Voltage (+25°C)

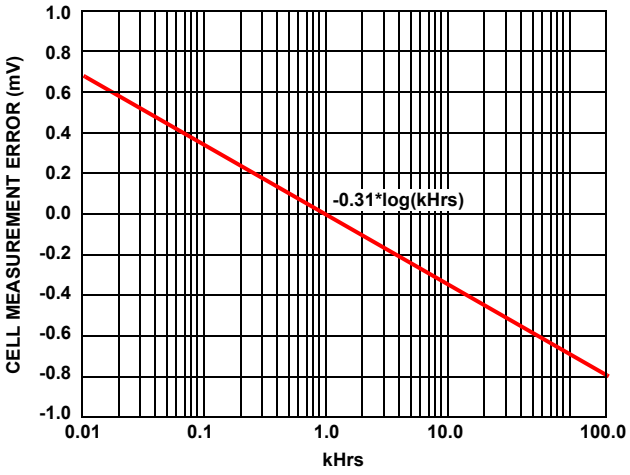


Figure 37. Long Term Drift

3. Device Description and Operation

The ISL78600 is a Li-ion battery manager IC that supervises up to 12 series-connected cells. Up to 14 ISL78600 devices can be connected in series to support systems with up to 168 cells. The ISL78600 provides accurate monitoring, cell balance control, and diagnostic functions. The ISL78600 includes a voltage reference, 14-bit A/D converter, and registers for control and data.

When multiple ISL78600 devices are connected to a series of cells, their power supply domains are normally non-overlapping. The lower (VSS) supply of each ISL78600 nominally connects to the same potential as the upper (V_{BAT}) supply of the ISL78600 device below.

3.1 Cell Voltage Monitoring

Within each device, the cell voltage monitoring system has two basic elements: a level shift to eliminate the cell common-mode voltage, and an analog-to-digital conversion of the cell voltage.

Each ISL78600 is calibrated at a specific cell input voltage value, V_{NOM}. Cell voltage measurement error data is given in "Measurement Specifications" on page 11 for various voltage and temperature ranges with voltage ranges defined with respect to V_{NOM}. Plots showing the typical error distribution over the full input range are included in "Typical Performance Curves" on page 21.

To collect cell voltage and temperature measurements, the ISL78600 provides two multiple parameter measurement "scanning" modes in addition to single parameter direct measurement capability. The scanning modes provide pseudo-simultaneous measurement of all cell voltages in the stack.

The ISL78600 does not measure current. The system performs this separately using other measurement systems.

The only filtering applied to the ADC measurements is that resulting from external protection circuits and the limited bandwidth of the measurement path. No additional filtering is performed within the part. This arrangement is typically needed to maintain timing integrity between the cell voltage and pack current measurements. However, the ISL78600 does apply filtering to the fault detection systems.

3.2 Cell Balancing

Cell balancing is an important function in a battery pack consisting of a stack of multiple Li-ion cells. As the cells charge and discharge, differences in each cell's ability to take on and give up charge, typically leads to cells with different states of charge. The problem with a stack of cells having different states of charge is that Li-ion cells have a maximum voltage, above which it should not be charged, and a minimum voltage, below which it should not be discharged. The extreme case, where one cell in the stack is at the maximum voltage and one cell is at the minimum voltage, results in a nonfunctional battery stack, because the battery stack cannot be charged or discharged.

The ISL78600 provides multiple cell balance modes: Manual Balance mode, Timed Balance mode, and Auto Balance mode. These are described in more detail in "Alarm Response" on page 106.

The ISL78600 incorporates extensive fault diagnostics functions, which include cell overvoltage and undervoltage, regulator and oscillator operation, open cell input detection, and communication faults. The current status of most faults is accessible using the ISL78600 registers. Some communication faults are reported by special responses to system commands and some as "unprompted" responses from the device detecting the fault to the host microcontroller through the daisy chain.

3.3 Power Modes

To conserve power, the ISL78600 has three main power modes: Normal mode, Sleep mode, and "off" (Shutdown mode).

3.3.1 Sleep Mode

The device enters Sleep mode in response to a *Sleep* command or after a watchdog timeout (see "Watchdog Function" on page 105.) Only the communications input circuits, low speed oscillator and internal registers are active in Sleep mode, allowing the part to perform timed scan and balancing activity and to wake up in response to communications.

3.3.2 Shutdown Mode (Hardware Reset)

The device is in Shutdown mode when the Enable pin is low. In this mode, the internal bias for most of the IC is powered down except digital core, sleep mode regulators, and digital input buffers. When exiting, the device powers up and does not reload the factory programmed configuration data from the EEPROM.

The host can perform a hardware reset by toggling the EN pin low, then high. This resets the hardware but does not reload the registers. After waiting for a t_{UV} settling time, see "Power-Up Specifications" on page 13 the host must perform a new IDENTIFY sequence (see "Identify Command" on page 69). Also, since the hardware reset does not recall the EEPROM values, it is recommended that a Reset command "Reset Command" on page 60 be sent to each device to ensure that EEPROM values have been properly recalled. The following is the recommended sequence following a hardware reset.

1. Switch EN on.
2. Wait the required delay (t_{UV} "Power-Up Specifications" on page 13) after re-enabling the parts.
3. Identify devices
4. Send Reset command to each device starting from the top device.
   (This operation recalls the EEPROM values and performs an EEPROM checksum calculation.)
5. Identify devices again (Identify is required after a software reset)
6. The host checks the EEPROM MISR Data Register and MISR Calculated Checksum register on all devices. These two register values should match (see "Memory Checksum" on page 102).
7. Re-load all non-default setup parameters (like OV/UV limits) to all devices.
8. The host sends a Calc Register Checksum command to each device (see "Calc Register Checksum" on page 61).
9. The host sends a Check Register checksum to verify that there is no error (see "Check Register Checksum" on page 61). If there is a mismatch, the device sends a fault response back to the host (see "Memory Checksum" on page 102).

3.3.3 Normal Mode

Normal mode consists of an active state and a standby state. In the standby state, all systems are powered and the device is ready to perform an operation in response to commands from the host microcontroller. In the Active state, the device is performing an operation, such as ADC conversion, open-wire detection, etc.

4. System Hardware Connection

4.1 Battery and Cell Balance Connection

The first consideration in designing a battery system around the ISL78600 is the connection of the cells to the IC.

The battery connection elements are split between the cell monitor connections (VCn) and the cell balance connections (CBn).

4.1.1 Battery Connection

All inputs to the ISL78600 VCn pins are protected against battery voltage transients by external RC filters. The basic input filter structure, with capacitors to the local ground, provides protection against transients and EMI for the cell inputs. They carry the loop currents produced by EMI and should be placed as close to the battery connector as possible. The ground terminals of the capacitors must be connected directly to a solid ground plane. Do not use vias to connect these capacitors to the input signal path or to ground. Any vias should be placed in line to the signal inputs so that the inductance of these forms a low pass filter with the grounded capacitors.

The resistors on the input filter provide a current limit function during hot plug events. The ISL78600 is calibrated for use with 1kΩ series protection resistors at the VCn inputs. The V_{BAT} connection uses a lower value input resistor to accommodate the supply current of the ISL78600. As much as possible, the time constant produced by the filtering applied to VBAT should be matched to that applied to the VCn monitoring inputs (see Figure 38).

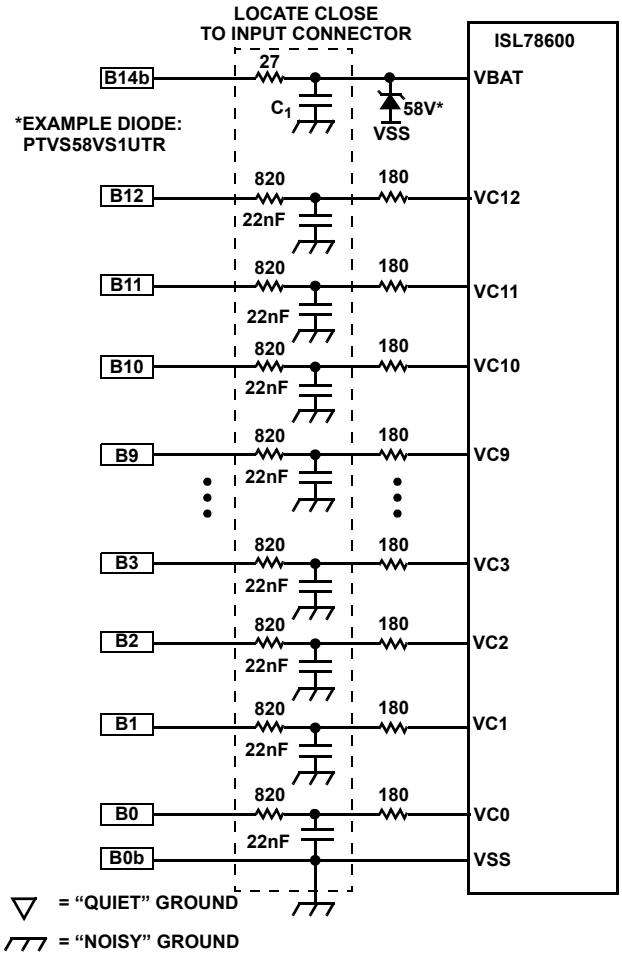


Figure 38. Typical Input Filter

The filtered battery voltage connects to the internal cell voltage monitoring system. The monitoring system is made up of three basic elements: a level shifter to eliminate the cell common-mode voltage, a multiplexer to select a specific input, and an analog-to-digital conversion of the cell voltage.

Each ISL78600 is calibrated at a specific cell input voltage value, V_{NOM} with an expected input series resistance of 1kΩ. Cell voltage measurement error data is given in "Measurement Specifications" on page 11 for various voltage and temperature ranges with voltage ranges defined with respect to V_{NOM}. Plots showing the typical error distribution over the full input range are included in "Typical Performance Curves" on page 21.

Another important consideration is the connection of cells in a stacked (non-overlapping) configuration. Mainly, this involves how to connect the supply and ground pins at the junction of two devices. The diagram in Figure 39 shows the recommended minimum connection to the pack. It is preferred that there be four connection wires at the intersection of two devices, but this does pose a cost constraint. To minimize the connections, the power and monitor pins are connected separately, as shown in Figure 39. It is not recommended that all four wires connect together with a single wire to the pack. There are two reasons for this. First, the power supply current for the devices might affect the accuracy of the cell voltage readings. Second, if the single wire breaks, it is very difficult for the system to tell specifically what happened through normal diagnostic methods.

An alternative circuit in Figure 40 shows the connection of one (or two) wires with additional Schottky diodes to provide supply current paths to allow the device to detect a connection fault and to minimize the effects on cell voltage measurements when there is an open connection to the battery.

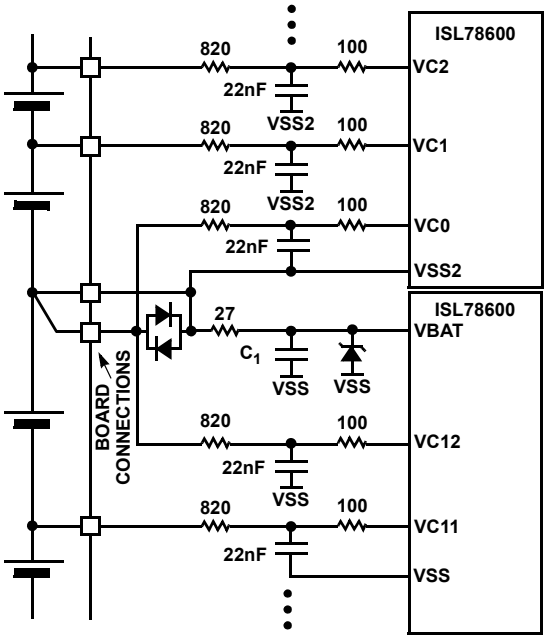


Figure 39. Battery Connection Between Stacked Devices (Option 1)

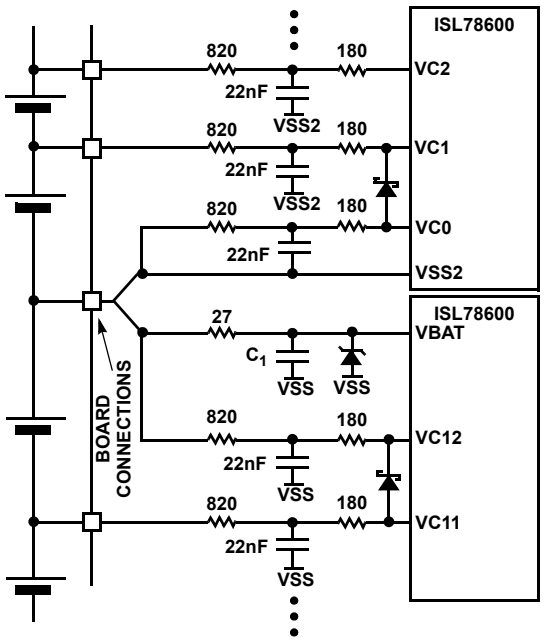


Figure 40. Battery Connection Between Stacked Devices (Option 2)

4.1.2 Cell Balance Connection

The ISL78600 uses external MOSFETs for cell balancing. The gate drive for these is derived from on-chip current sources on the ISL78600, which are 25µA nominally. The current sources are turned on and off as needed to control the external MOSFET devices. The current sources are turned off when the device is in Shutdown mode or Sleep mode. The ISL78600 uses a mix of N-channel and P-channel MOSFETs for the external balancing function. The top three cell locations, Cells 10, 11, and 12 are configured to use P-channel MOSFETs while the remaining cell locations, Cells 1 through 9 use N-channel MOSFETs. The mix of N-channel and P-channel devices are used for the external FETs in order to remove the need for a charge pump, while providing a balance FET gate voltage that is sufficient to drive the FET on, regardless of the cell voltages.

Figures 41 and 42 show the circuit detail for the recommended balancing and cell voltage monitoring system. In this configuration, the cell voltage is monitored after the cell balance resistor. This allows the system to monitor the operation of the external balance circuits and is part of the fault detection system. However, this connection prevents monitoring the cell voltage while cell balance is enabled for that cell.

Figure 41 shows the connection for VC12 to VC9. This connection for the upper 3 cells uses P-channel FETs, while VC9 and below use N-channel FETs. Similarly, Figure 42 shows the connection for VC1 to VC3, using an N-channel FETs, with the connections for VC3 through VC9 being similar. See Figure 52 on page 42 for a more complete example.

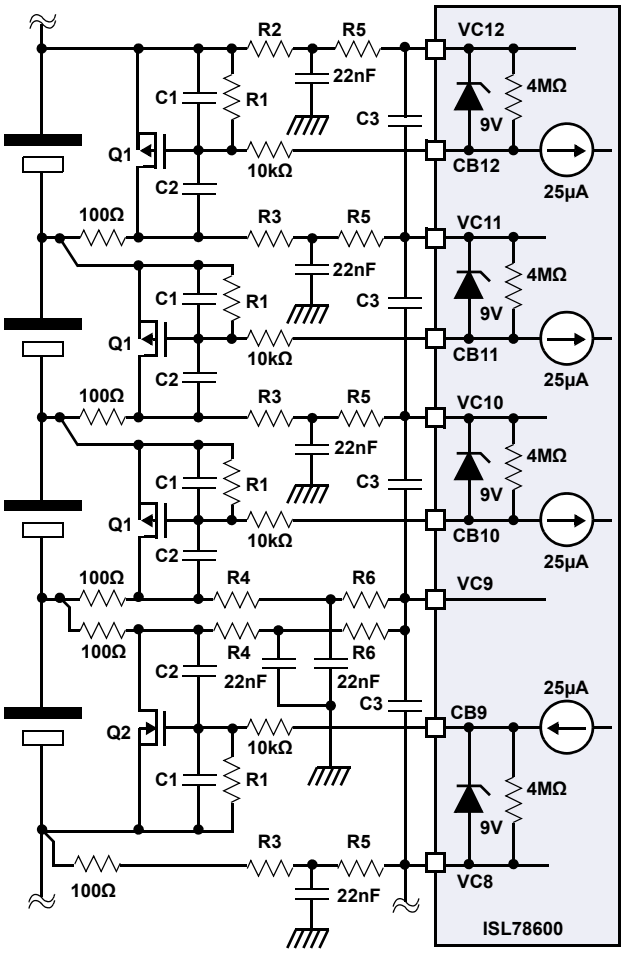


Figure 41. Cell Monitor and Balance Circuit Arrangement (VC8 to VC12)

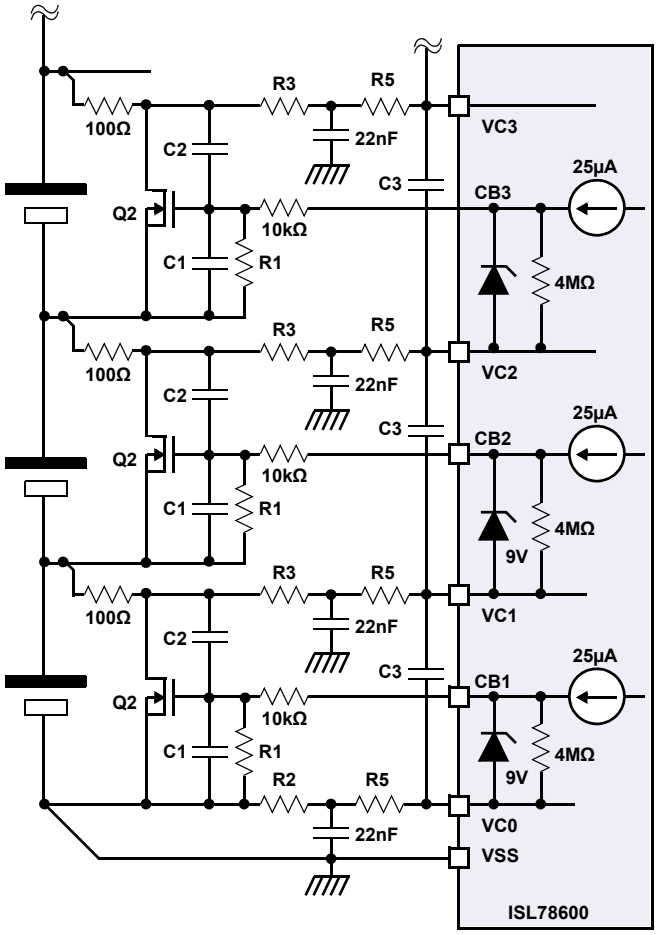


Figure 42. Cell Monitor and Balance Circuit Arrangement (VC0 to VC3)

Table 3. ISL78600 Input Filter Component Options

Q1 (P-channel) with examples		Q2 (N-channel) with examples		C1	C2	C3	R1	R2	R3	R4	R5	R6
30V	A&O Semi AO3401	30V	A&O Semi AO3402	10nF	1nF	Not populated	100k	820	720	1.54k	180	360
30V	A&O Semi AO3401	30V	A&O Semi AO3402	10nF	1nF	100nF	100k	100	0	0	910	1900
60V	Fairchild FDN5618	60V	Diodes DMN6140L-7	10nF	Not needed	Not populated	330k	820	720	1.54k	180	360
60V	Fairchild FDN5618	60V	Diodes DMN6140L-7	10nF	Not needed	100nF	330k	100	0	0	910	1900

Note: Q1 and Q2 should have low $r_{DS(ON)}$ specifications (<100mΩ) to function properly in this fault diagnostic configuration.

Figures 43 and 44 show an alternative balancing and cell voltage monitoring arrangement. The diagram in Figure 43 shows the connection for VC9 through VC12, using P-channel FETs for the upper three inputs. Figure 44 shows the connection for VC1 through VC3 using N-channel FETs. With this alternative circuit it is possible to monitor the cell voltages during cell balancing (even though the voltage drops a little when measuring a cell that is being balanced). However, this circuit connection does not allow the system to check for all potential external component failures. See Figure 55 on page 45 for a more complete example.

The gate of the N-channel MOSFET (cell locations 1 through 9) and P-channel MOSFETs (Cells 10 through 12) are normally protected against excessive voltages during cell voltage transients by the action of the parasitic Cgs and Cgd capacitances. These momentarily turn on the FET in the event of a large transient, thus limiting the Vgs values to reasonable levels. A 10nF capacitor is included between the MOSFET gate and source terminals to protect against EMI effects. This capacitor provides a low impedance path to ground at high frequencies and prevents the MOSFET turning on in response to high frequency interference.

The 10k and 330k resistors are chosen to prevent the 9V clamp at the output from the ISL78600 from activating.

Reduced cell counts for fewer than 12 cells are accommodated by removing connections to the cells in the middle of the stack first. The top and bottom cell locations are always occupied. See "Operating with Reduced Cell Counts" on page 40 for suggested cell configurations when using fewer than 12 cells.

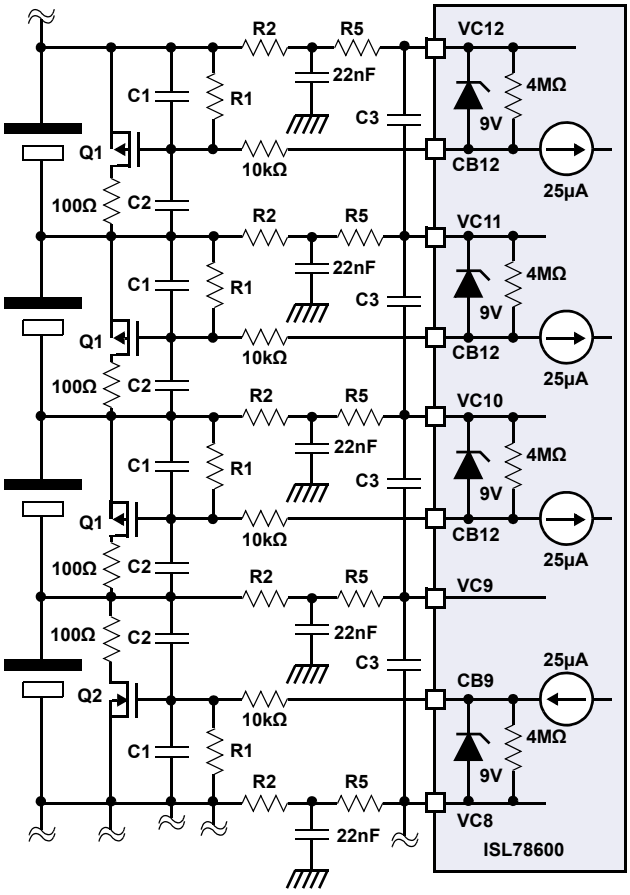


Figure 43. Alternate Cell Monitor and Balance Circuit Arrangement (VC8 to VC12)

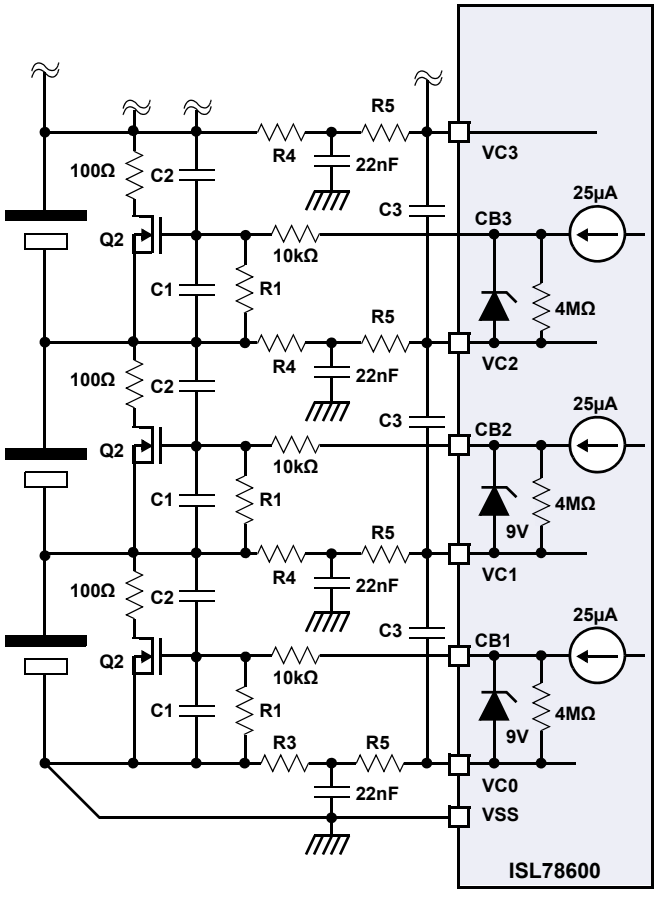


Figure 44. Alternate Cell Monitor and Balance Circuit Arrangement (VC1 to VC3)

Table 4. ISL78600 Alternate Input Filter Component Options

Q1 (P-channel) with examples		Q2 (N-channel) with examples		C1	C2	C3	R1	R2	R3	R4	R5	R6
30V	Diodes DMP32D4S-13	30V	Diodes DMN63D8L-7	10nF	1nF	Not populated	100k	820	720	1.54k	180	360
30V	Diodes DMP32D4S-13	30V	Diodes DMN63D8L-7	10nF	1nF	100nF	100k	100	0	0	910	1900
60V	Fairchild NDS0605	60V	Fairchild NDS7002	10nF	Not needed	Not populated	330k	820	720	1.54k	180	360
60V	Fairchild NDS0605	60V	Fairchild NDS7002	10nF	Not needed	100nF	330k	100	0	0	910	1900

Note: Q1 and Q2 $r_{DS(ON)}$ specification is not critical, since fault diagnostics are not performed in this configuration.

4.1.3 Cell Voltage Measurements during Balancing

The standard cell balancing circuit (Figures 41, 42, and 52) is configured so the cell measurement is taken from the drain connection of the balancing MOSFET. When balancing is enabled for a cell, the resulting cell measurement is then the voltage across the balancing MOSFET (VGS voltage). This system provides a diagnostic function for the cell balancing circuit. The input voltage of the cell adjacent to the MOSFET drain connection is also affected by this mechanism: the input voltage for this cell increases by the same amount that the voltage of the balance cell decreases.

For example, if Cells 2 and 3 are both at 3.6V and balancing is enabled for Cell 2, the voltage across the balancing MOSFET may be only 50mV. In this case, the input voltage on the VC2 pin would be VC1 + 50mV and Cell 3 would be VC2 + 7.15V. Thus, the VC3 value is outside the measurement range of the cell input. The VC3 would then read full scale voltage, which is 4.9994V. This full scale voltage reading occurs if the sum of the voltages on the two adjacent cells is greater than the total of 5V plus the balancing on voltage of the balanced cell. Table 5 shows the cell affected when each cell is balanced.

The cell voltage measurement is affected by impedances in the cell connectors and any associated wiring. The balance current passes through the connections at the top and bottom of the balanced cell. This effect further reduces the voltage measured on the balanced cell and increases the voltage measured on cells above and below the balanced cell. For example, if Cell 4 is balanced with 100mA, and the total impedance of the connector and wiring for each cell connection is 0.1Ω, then Cell 4 would read low by an additional 20mV (10mV due to each pin) while Cells 3 and 5 would both read high by 10mV.

Table 5. Cell Readings During Balancing

Cell Balanced	Cell with Low Reading	Cell with High Reading
1	1	2
2	2	3
3	3	4
4	4	5
5	5	6
6	6	7
7	7	8
8	8	9
9	9 (Note 11)	10 (Note 11)
10	10 (Note 11)	9 (Note 11)
11	11	10
12	12	11

Note:

11. Cells 9 and 10 produce a different result from the other cells. Cell 9 uses an N-channel MOSFET while Cell 10 uses a P-channel MOSFET. The circuit arrangement used with these devices produces approximately half the normal cell voltage when balancing is enabled. The adjacent cell then sees an increase of half the voltage of the balanced cell.

4.2 Power Supplies and Reference

4.2.1 Voltage Regulators

The two VBAT pins, along with V3P3, VCC, and VDDEXT are used to supply power to the ISL78600. Power for the high voltage circuits and Sleep mode internal regulators is provided through the VBAT pins. V3P3 supplies the logic circuits and VCC is similarly used to supply the low voltage analog circuits. The V3P3 and VCC pins must not be connected to external circuits other than those associated with the ISL78600 main voltage regulator. The VDDEXT pin is provided for use with external circuits.

The ISL78600 main low voltage regulator uses an external NPN pass transistor to supply 3.3V power for the V3P3 and VCC pins. This regulator is enabled whenever the ISL78600 is in Normal mode and can also be used to power external circuits through the VDDEXT pin. An internal switch connects the VDDEXT pin to the V3P3 pin. Both the main regulator and the switch are off when the part is placed in Sleep mode or Shutdown mode (EN pin Low.) The pass transistor's base is connected to the ISL78600 BASE pin. A suitable configuration for the external components associated with the V3P3, VCC, and VDDEXT pins is shown in Figure 45.

The external pass transistor is required. **Do not allow the BASE pin to float.**

4.2.2 Voltage Reference

A bypass capacitor is required between REF (Pin 33) and the analog ground VSS. The total value of this capacitor should be in the range of 2.0µF to 2.5µF. Use X7R type dielectric capacitors for this function. The ISL78600 continuously performs a power-good check on the REF pin voltage starting at 20ms after a power-up, enable, or wakeup condition. If the REF capacitor is too large, then the reference voltage may not reach its target voltage range before the power-good check starts and can result in a *REF* Fault. If the capacitor is too small, it may lead to inaccurate voltage readings.

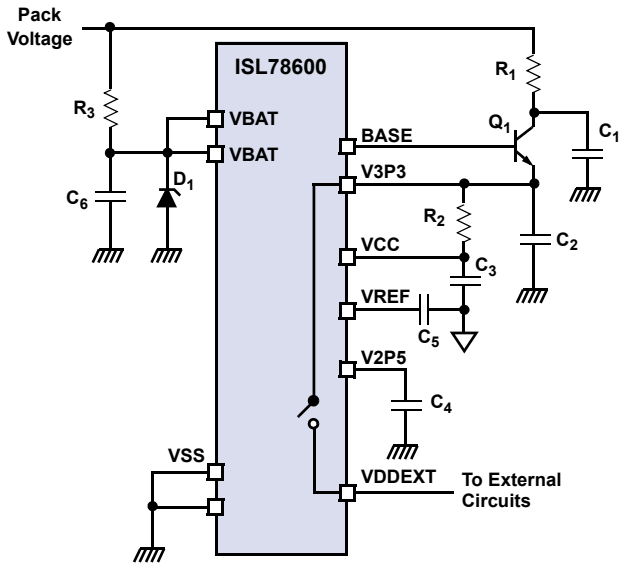


Figure 45. ISL78600 Regulator and External Supply Arrangement

Table 6. Component Selection for Circuit in Figure 45

Component	Value
R_1	sized to pass the maximum supply current at the minimum specified battery pack voltage.
R_2	33Ω
R_3	27Ω
C_1	Selected to produce a time constant with R_1 of a few milliseconds. C_1 and R_1 provide transient protection for the collector of Q_1. Component values and voltage ratings should be obtained through simulation of measurement of the worst case transient expected on VBAT.

Table 6. Component Selection for Circuit in Figure 45 (Continued)

Component	Value
C_2, C_3, C_4	1µF
C_5	2.2µF
C_6	220nF/100V
D_1	PTVS54VS1UTR
Q_1	Selected for power dissipation at the maximum specified battery voltage and load current. The load current includes the V_{3P3} and V_{CC} currents for the ISL78600 and the maximum current drawn by external circuits supplied through VDDEXT. The voltage rating should be determined by the worst case transient expected on VBAT.

4.3 Communications Circuits

The ISL78600 operates as a stand-alone monitor for up to 12 series-connected cells or in a daisy chain configuration for multiple series connected ISL78600 monitoring devices. For stand-alone (non-daisy chain) systems, only a synchronous SPI is needed for communications between a host microcontroller and the ISL78600.

Both the SPI port and daisy chain ports are needed for communication in systems where there is more than one ISL78600.

A daisy chain consists of a bottom device, a top device, and up to 12 middle devices. The ISL78600 device located at the bottom of the stack is called the master and communicates to the host microcontroller using SPI communications and to other ISL78600 devices using the daisy chain port. Each middle device provides two daisy chain ports: one is connected to the ISL78600 above in the stack and the other to the ISL78600 below. Communications between the SPI and daisy chain interfaces are buffered by the master device to accommodate timing differences between the two systems.

The daisy chain ports are fully differential, DC balanced, bidirectional, and AC coupled to provide maximum immunity to EMI and other system transients while requiring only two wires for each port.

The addressed device, top device, and bottom device act as master devices for controlling command and response communications. All other devices are repeaters, passing data up or down the chain.

The communications setup is controlled by the COMMS SELECT 1 and COMMS SELECT 2 pins on each device. These pins specify whether the ISL78600 is a stand-alone device, the daisy chain master, the daisy chain top, or a middle position in the daisy chain. See Figures 46, 47, and Table 7. This configuration also specifies the use of SPI or daisy chain on the communication ports.

Table 7. Communications Mode Control

COMMS SELECT1	COMMS SELECT2	Port 1 COMM	Port 2 COMM	Communications Configuration
0	0	SPI (Full Duplex)	Disabled	Stand-Alone
0	1	SPI (Half Duplex)	Enabled	Daisy Chain, Master Device Setting
1	0	Daisy Chain	Disabled	Daisy Chain, Top Device Setting
1	1	Daisy Chain	Enabled	Daisy Chain, Middle Device Setting

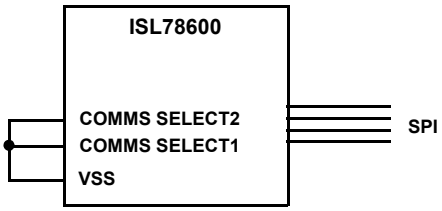


Figure 46. Non-Daisy Chain Communications and Selection

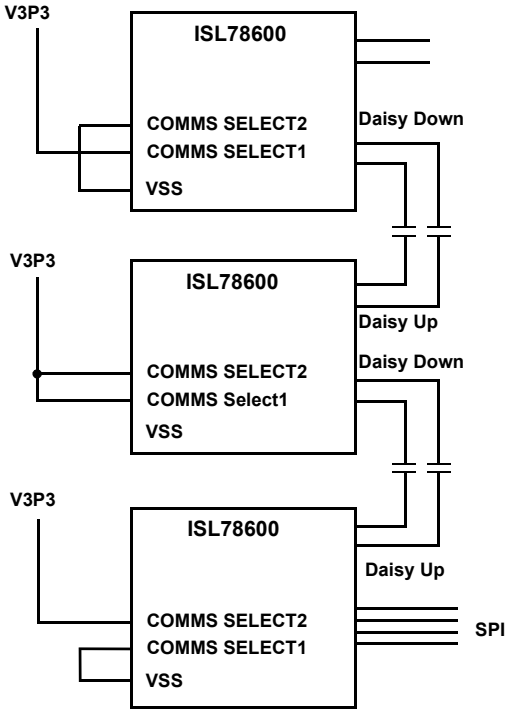


Figure 47. Daisy Chain Communications and Selection

Four daisy chain data rates are available and are configurable by pin selection using the COMMS RATE 0 and COMMS RATE 1 pins (see Table 8 on page 36).

Table 8. Daisy Chain Communication Rate Selection

COMMS Rate 0	COMMS Rate 1	Data Rate (kHz)
0	0	62
0	1	125
1	0	250
1	1	500

The state of the COMMS SELECT 1, COMMS SELECT 2, COMMS RATE 0, and COMMS RATE 1 pins can be checked by reading the CSEL[2:1] and CRAT[1:0] bits in the Comms Setup register (see Table 9). The SIZE[3:0] bits show the number of devices in the daisy chain and the ADDR[3:0] bits indicate the location of a device within the daisy chain. See “Read and Write Commands” on page 52 for more information how to read this register.

Table 9. Comms Setup Register (ADDRESS 6’h18)

11	10	9	8	7	6	5	4	3	2	1	0
CRAT1	CRAT0	CSEL2	CSEL1	SIZE3	SIZE2	SIZE1	SIZE0	ADDR3	ADDR2	ADDR1	ADDR0
Shows the status of the COMMS RATE 1 and COMMS RATE 0 pins		Shows the status of the COMMS SEL 2 and COMMS SEL 1 pins		Shows the daisy chain stack size (i.e. the total number of stacked devices)				Shows the devices position within the daisy chain stack			

4.4 Daisy Chain Circuits

The ISL78600 daisy chain communications system external circuit arrangement is symmetrical to provide the bidirectional communications function. The performance of the system under transient voltage and EMI conditions is enhanced by the use of a capacitive load. A schematic of the daisy chain circuit for board-to-board connection is shown in Figure 48.

The basic circuit elements are the series resistor and capacitor elements, R_1 and C_1, which provide the transient current limit and AC coupling functions, and the line termination components C_2, which provide the capacitive load. Capacitors C_1 and C_2 should be located as closely as possible to the board connector.

The AC coupling capacitors C_1 need to be rated for the maximum voltage, including transients, that are applied to the interface. Specific component values are needed for correct operation with each daisy chain data rate and are given in Table 10.

The daisy chain operates with standard unshielded twisted pair wiring. The component values given in Table 10 accommodate cable capacitance values from 0pF to 50pF when operating at the 500kHz data rate. Higher cable capacitance values can be accommodated by either reducing the value of C_2 or operating at lower data rates.

The values of components in Figure 48 are given in Table 10 for various daisy chain operating data rates.

The circuit and component values of Figure 48 and Table 10 accommodate cables with differential capacitance values in the ranges given. This allows a range of cable lengths to be accommodated through careful selection of cable properties.

The circuit of Figure 48 provides full isolation when used with off board wiring. The daisy chain external circuit can be simplified in cases where the daisy chain system is contained within a single board. Figure 49 on page 38 and Table 11 on page 38 show the circuit arrangement and component values for single board use. In this case, the AC coupling capacitors C_1 need only be rated for the maximum transient voltage expected from device to device.

The value for C_2 in Table 10 is ideally 220pF. This creates a 3:1 ratio in the transmit vs received signal. However, additional capacitance on the board due to device pin, board layout, and connector capacitance forces the use of a lower value capacitor. In practical terms, using the “ideal” capacitor and ignoring real additional capacitance on the board reduces the signal level at the receiver. It is recommended that the board layout minimize distance on daisy chain traces and isolate them as much as possible from each other and from ground planes. Expect at least 50pF to 90pF of additional board capacitance, depending on layout and connectors.

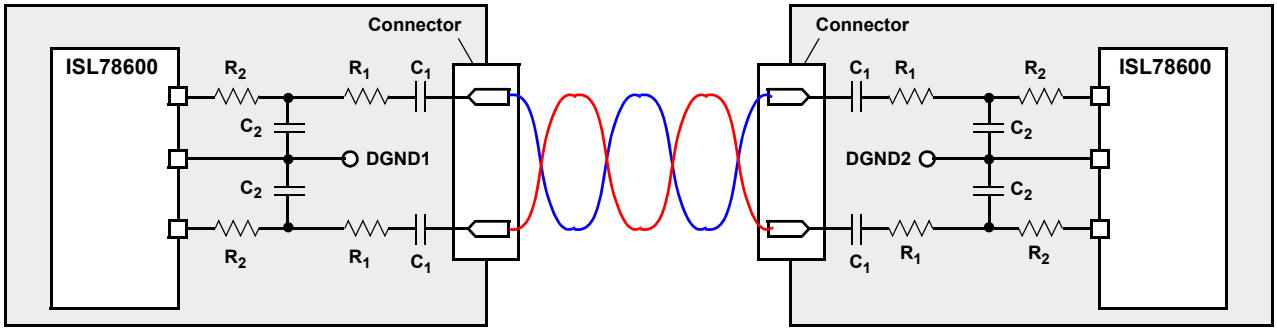


Figure 48. ISL78600 Daisy Chain Off-Board Circuit Implementation

Table 10. Component Values in Figure 48 (Off Board Circuit) for Various Data Rates

Component	Quantity (Each)	Daisy Chain Clock Rates				Comments
		500kHz	250kHz	125kHz	62.5kHz	
C_1	4	220pF	470pF	1nF	2.2nF	NPO dielectric type capacitors are recommended. Please consult Renesas if Y type or “open mode” devices are required for your application.
C_2	4	150pF (Note 12)	400pF	960pF	2nF	Use same dielectric type as C_1
R_1	4	470Ω	470Ω	470Ω	470Ω	
R_2	4	100Ω	100Ω	100Ω	100Ω	
Cable Capacitance Range	N/A	0 to 50pF	0 to 100pF	0 to 200pF	0 to 400pF	

Note:
12. See text for a discussion on the value for C_2.

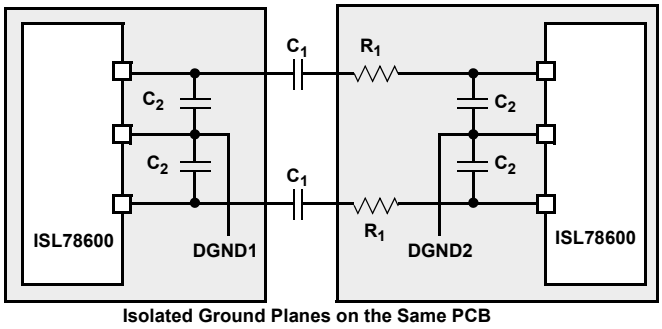


Figure 49. ISL78600 Daisy Chain On-Board Circuit Implementation

Table 11. Component Values in Figure 49 (On Board Circuit) for Various Data Rates

Component	Quantity (Each)	Tolerance	Daisy Chain Data Rate			
			500kHz	250kHz	125kHz	62.5kHz
C_1	2	5%	100pF	220pF	470pF	1nF
C_2	4	5%	150pF	400pF	960pF	2nF
R_1	2		1kΩ	1kΩ	1kΩ	1kΩ

4.5 External Inputs

The ISL78600 provides four external inputs for use either as general purpose analog inputs or for NTC type thermistors.

The arrangement of the external inputs is shown in Figure 50 on page 39 using the ExT4 input as an example. It is important that the components are connected in the sequence. For example, C_1 must be connected so the trace from this capacitor’s positive terminal connects to R_2 before connecting to R_1. This guarantees the correct operation of the various fault detection functions.

Each of the external inputs has an internal pull-up resistor, which is connected by a switch to the VCC pin whenever the TEMPREG output is active. This arrangement results in an open input being pulled up to the V_{CC} voltage.

Inputs above 15/16 of full scale are registered as open inputs and cause the relevant bit in the Over-Temperature Fault register, along with the OT bit in the Fault Status register to be set, on condition of the respective

temperature test enable bit in the Fault Setup register. The user must then read the register value associated with the faulty input to determine if the fault was due to an open input (value above 15/16 full scale) or an over-temperature condition (value below the external temperature limit setting).

The function of each of the components in Figure 50 is listed in Table 12 with the diagnostic result of an open or short fault in each component.

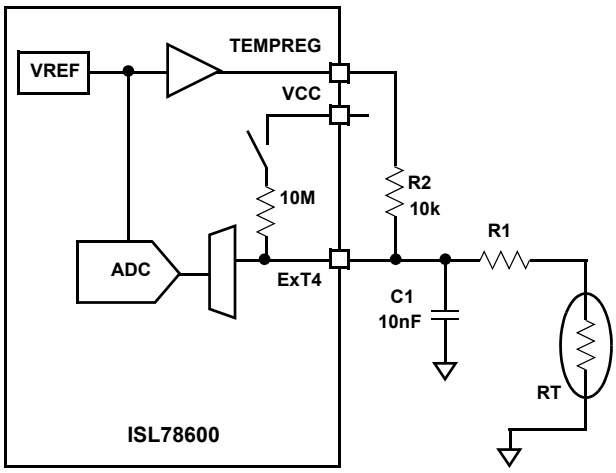


Figure 50. Connection of NTC Thermistor to ExT4

Table 12. Component Functions and Diagnostic Results for Circuit of Figure 50

COMPONENT	FUNCTION	DIAGNOSTIC RESULT
R_1	Optional. Might be needed if thermistor is off board. Provides protection from wiring shorts to external high voltage and input filtering.	Open: Open-wire detection Short: No diagnostic result
R_2	Measurement high-side resistor	Open: Low input level (over-temperature indication) Short: High input level (open-wire indication).
Thermistor		Open: High input level (open-wire indication). Short: Low input level (over-temperature indication)
C_1	Noise Filter. Connects to measurement ground VSS.	Open: No diagnostic result. Short: Low input level (over-temperature indication)

4.6 Typical Application Circuits

Typical application circuits are shown in Figures 51 through 57. Table 13 on page 48 contains recommended component values. All external (off-board) inputs to the ISL78600 are protected against battery voltage transients by RC filters. They also provide a current limit function during hot plug events. The ISL78600 is calibrated for use with 1kΩ series protection resistors at the cell inputs. V_{BAT} uses a lower value resistor to accommodate the V_{BAT} supply current of the ISL78600. A value of 27Ω is used for this component. As much as possible, the time constant produced by the filtering applied to V_{BAT} should be matched to that applied to the Cell 12 monitoring input. Component values given in Table 13 produce the required matching characteristics.

Figure 51 on page 41 shows the standard arrangement for connecting the ISL78600 to a stack of 12 cells. The cell input filter is designed to maximize EMI suppression. These components should be placed close to the connector with a well controlled ground to minimize noise for the measurement inputs. The balance circuits shown in Figure 51 provide normal cell monitoring when the balance circuit is turned off, and a near zero cell voltage reading when the balance circuit is turned on. This is part of the diagnostic function of the ISL78600.

Figure 52 on page 42 shows connections for the daisy chain system, setup pins, power supply, and external voltage inputs for daisy chain devices other than the master (stack bottom) device.

Figure 53 on page 43 shows the daisy chain system, setup pins, microcontroller interface, power supply, and external voltage inputs for the daisy chain master device. Figure 53 is also applicable to stand-alone (non-daisy chain) devices although in this case the daisy chain components connected to DHi2 and DLo2 would be omitted.

Figure 54 on page 44 shows an alternate arrangement for the battery connections in which the cell input circuits are connected directly to the battery terminal and not through the balance resistor. In this condition the balance diagnostic function capability is removed.

4.7 Operating with Reduced Cell Counts

When using the ISL78600 with fewer than 12 cells, ensure that each used cell has a normal input circuit connection to the top and bottom monitoring inputs for that cell. The simplest way to use the ISL78600 with any number of cells is to always use the full input circuit arrangement for all inputs, and short together the unused inputs at the battery terminal. In this way each cell input sees a normal source impedance independent of whether or not it is monitoring a cell.

The cell balancing components associated with unconnected cell inputs are not required and can be removed. Unused cell balance outputs should be tied to the adjacent cell voltage monitoring pin.

The input circuit component count can be reduced in cases where fewer than 10 cells are being monitored. It is important that cell inputs that are being used are not connected to other (unused) cell inputs as this would affect measurement accuracy. Figures 55, 56, and 57 show examples of systems with 10 cells, 8 cells, and 6 cells, respectively.

The component notations and values used in Figures 55, 56, and 57 are the same as those used in Figures 51. But in Figure 57, the resistor associated with the input filter on VC9 is noted as R_5, rather than R5U. This value change is needed to maintain the correct input network impedance in the absence of the Cell 9 balance circuits.

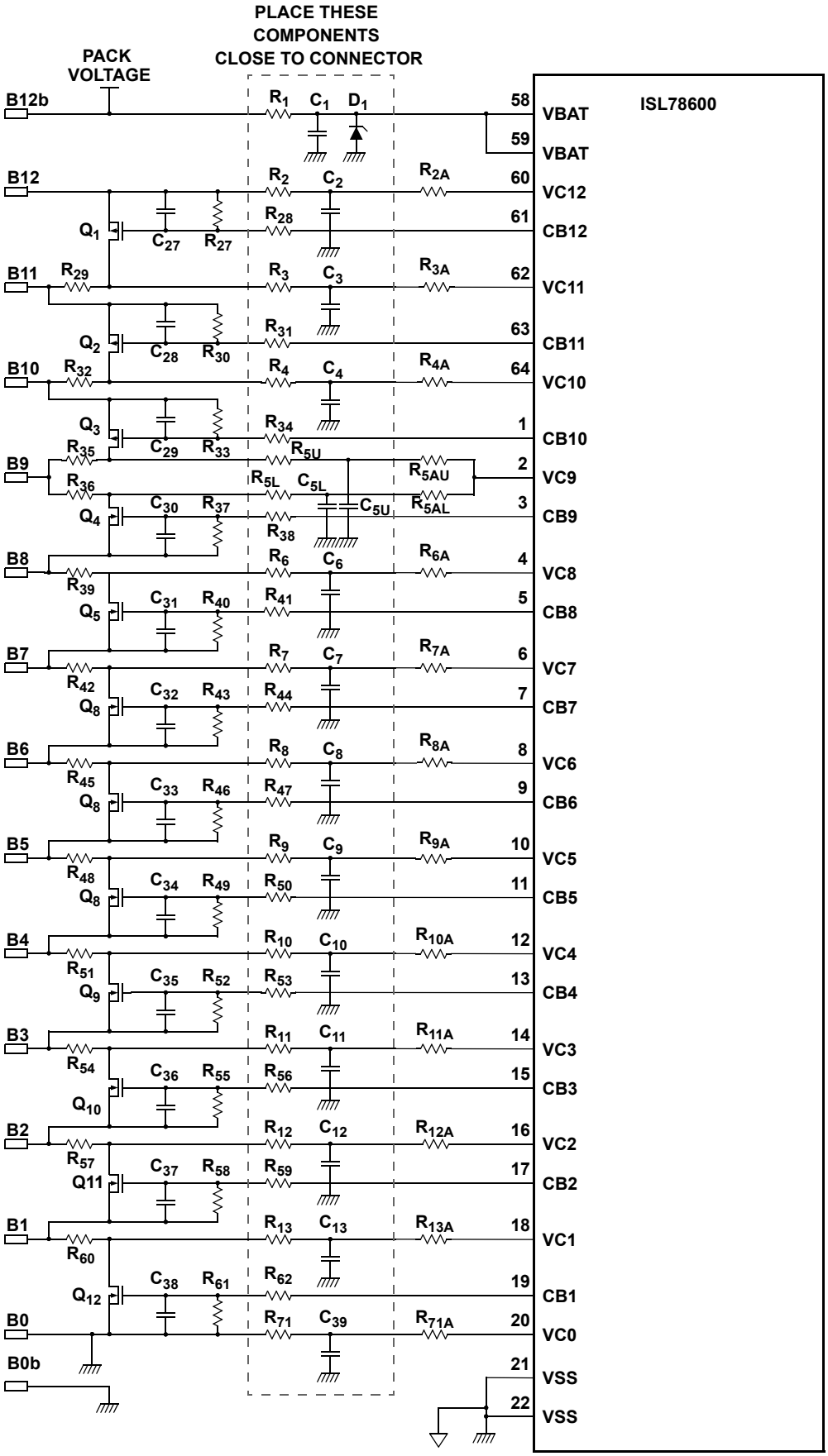


Figure 51. Typical Battery Connection Circuit

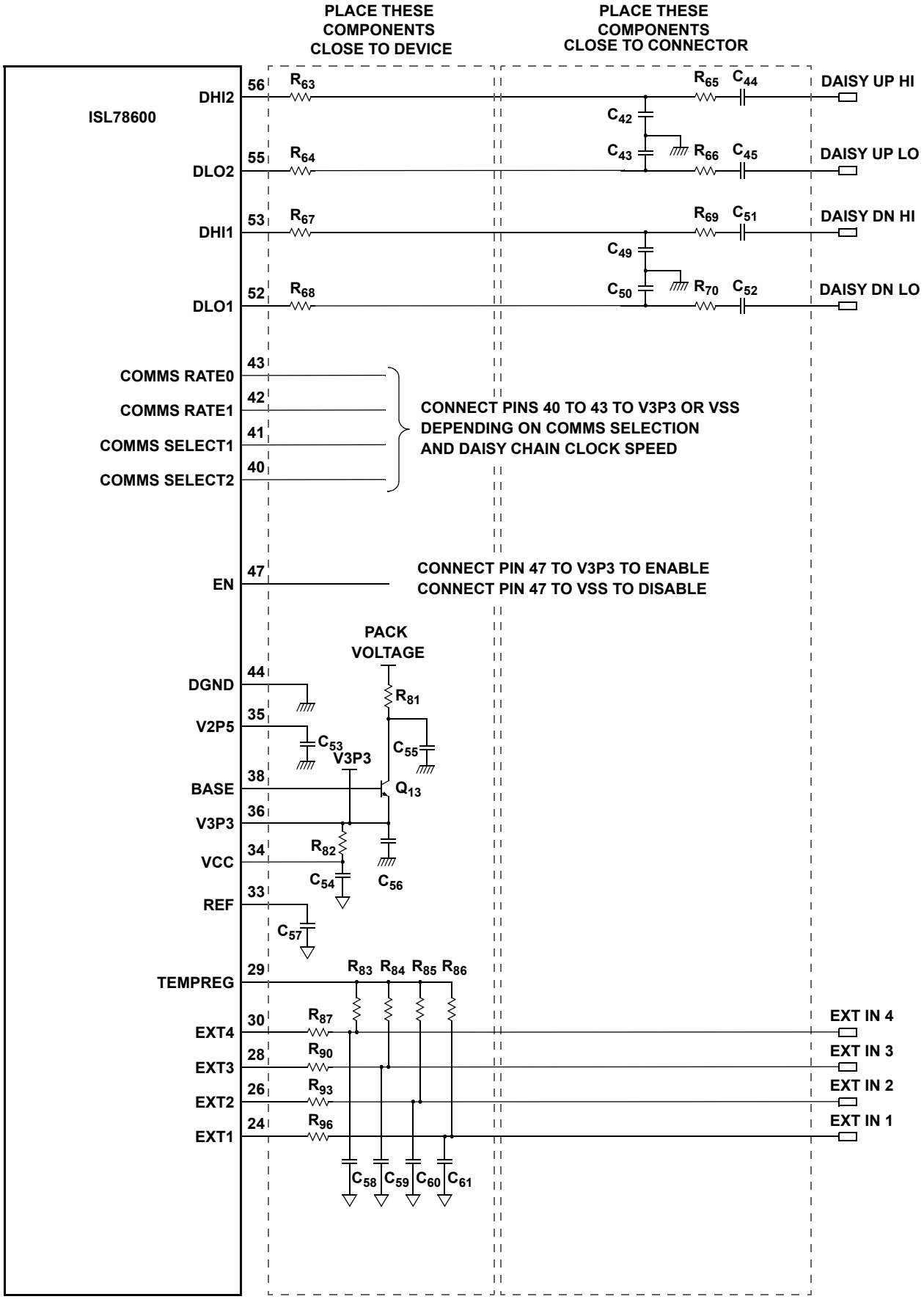


Figure 52. Typical Non-Battery Connection Circuits For Middle and Top Daisy Chain Devices

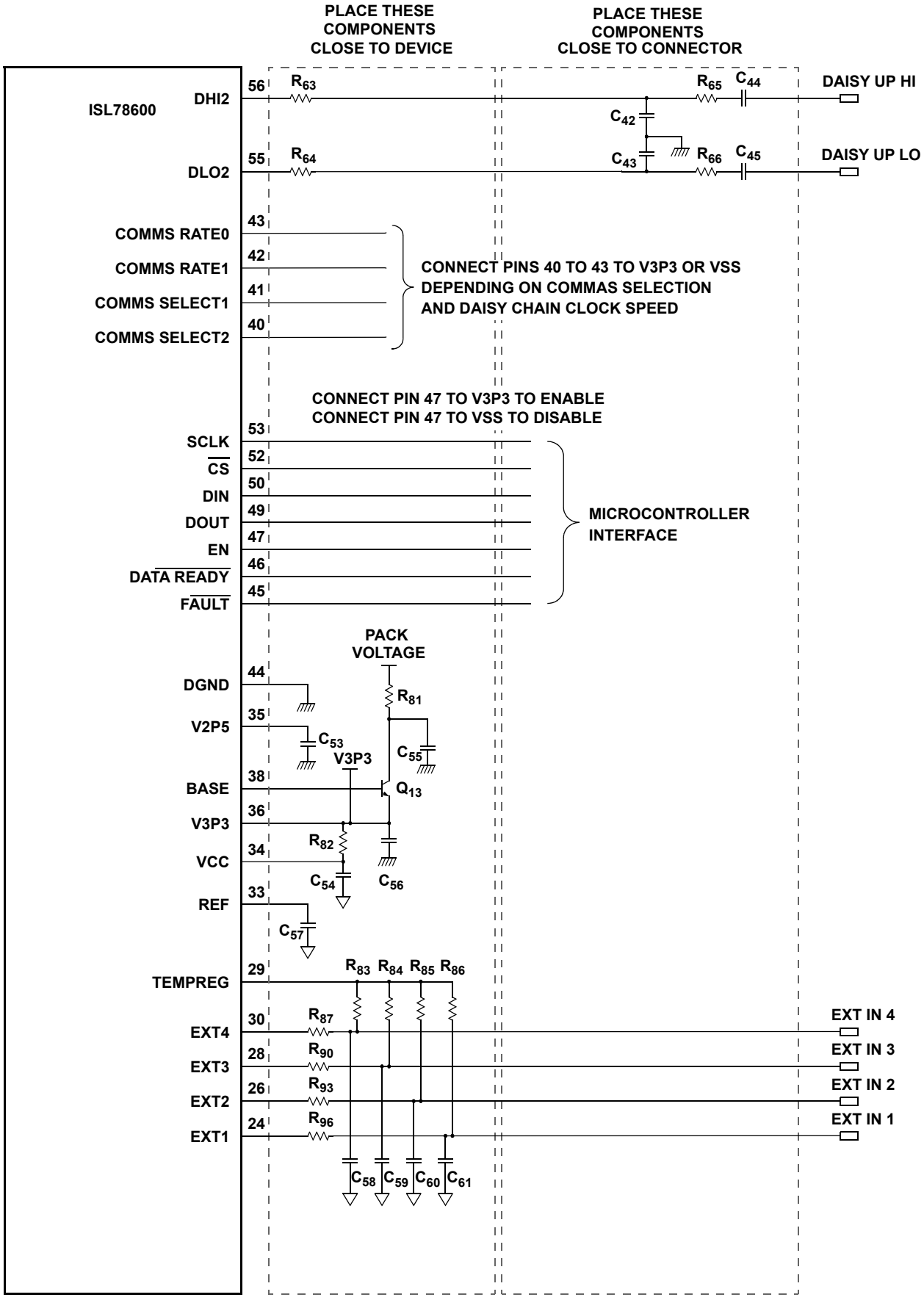


Figure 53. Typical Non-Battery Connection Circuits For Master Daisy Chain Device

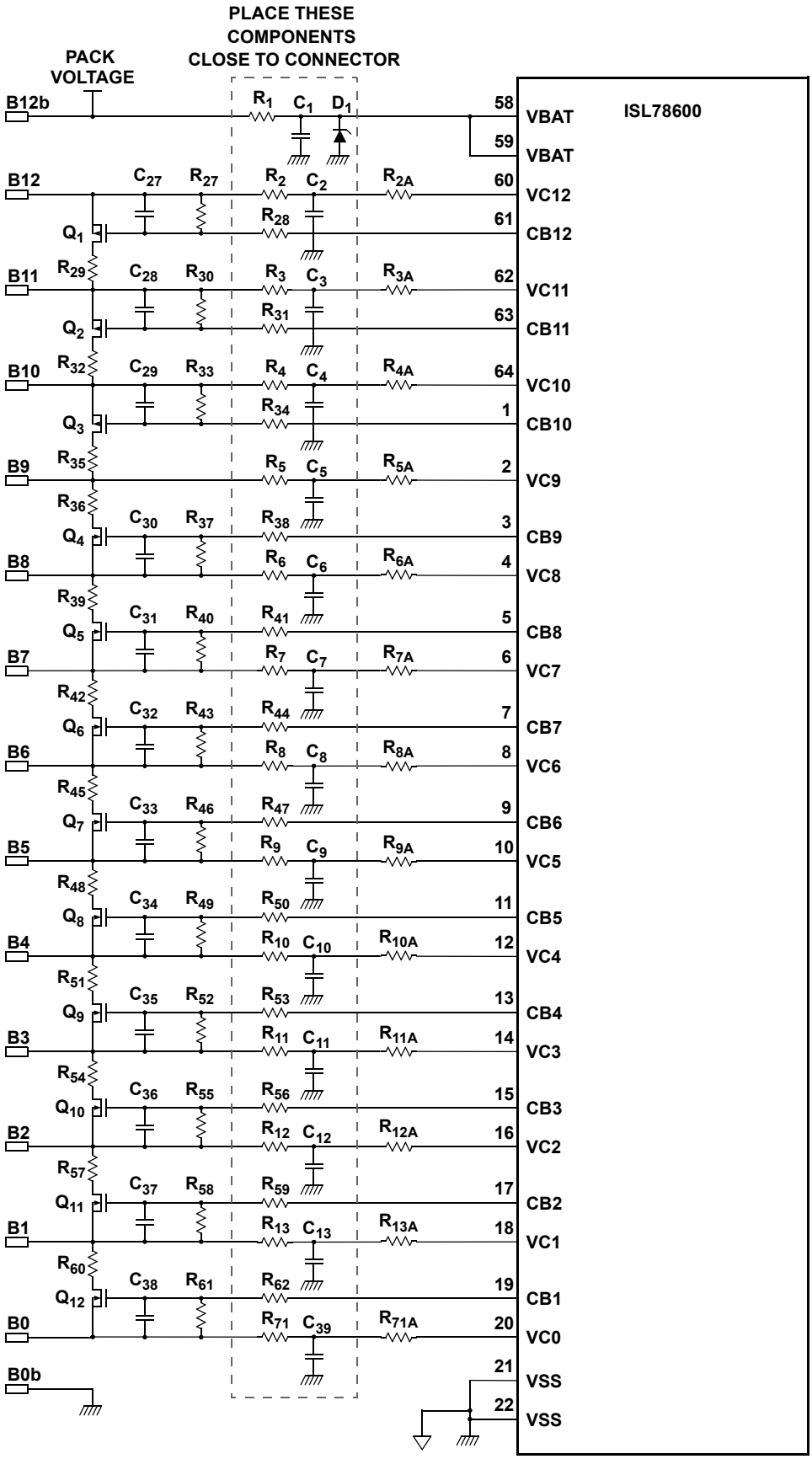


Figure 54. Alternate Battery Connection Circuit

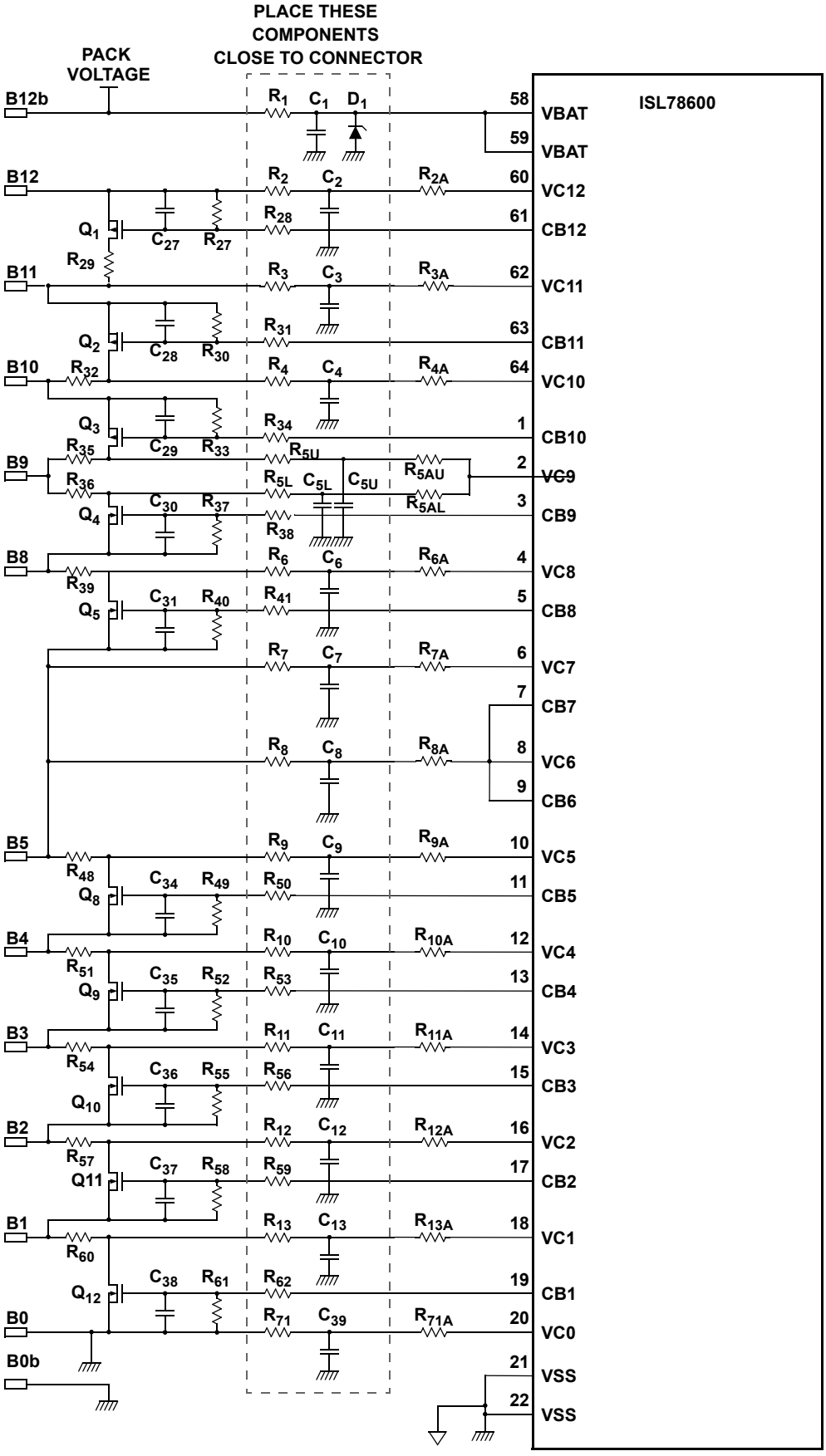


Figure 55. Typical 10 Cell Battery Connection Circuit

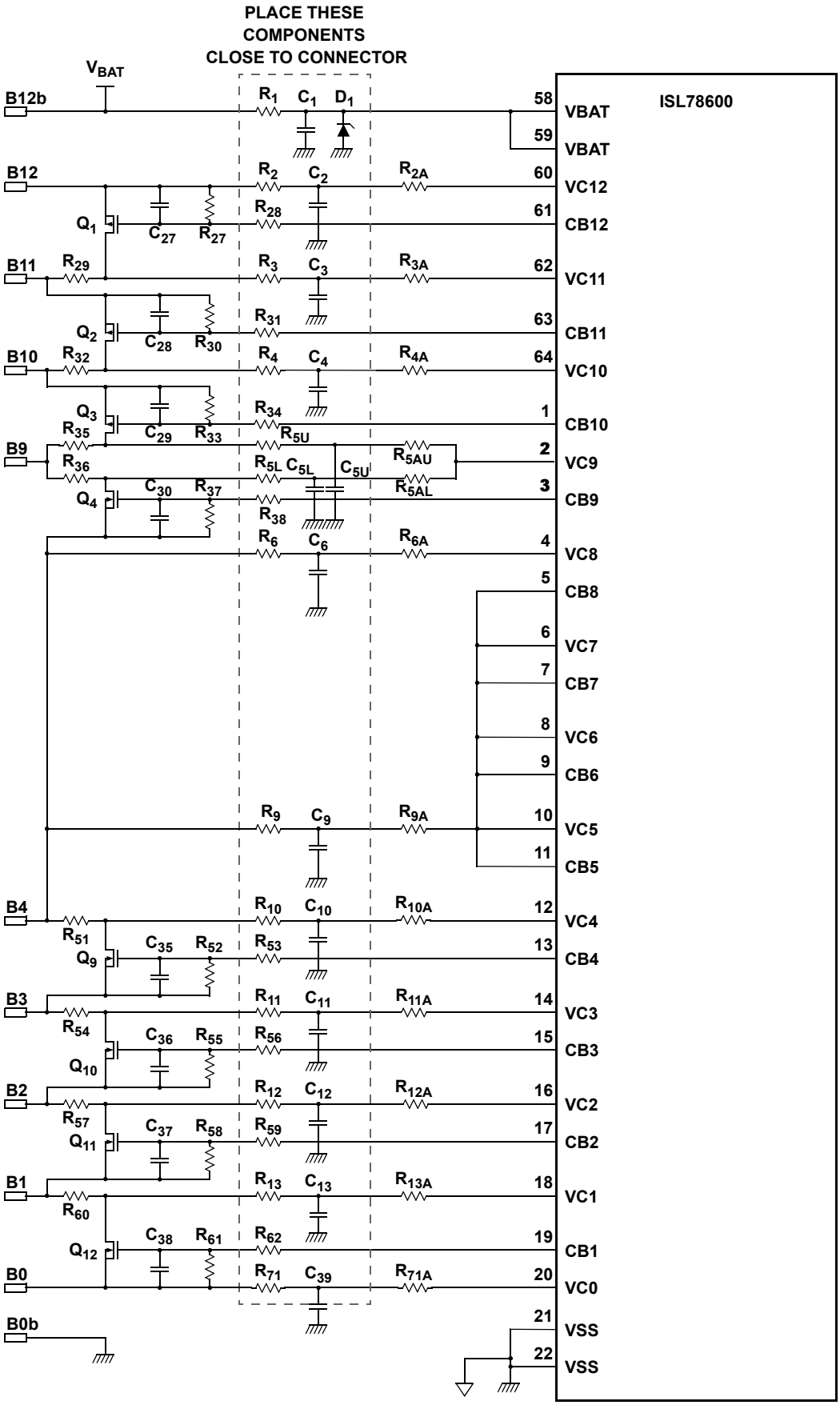


Figure 56. Typical 8 Cell Battery Connection Circuit

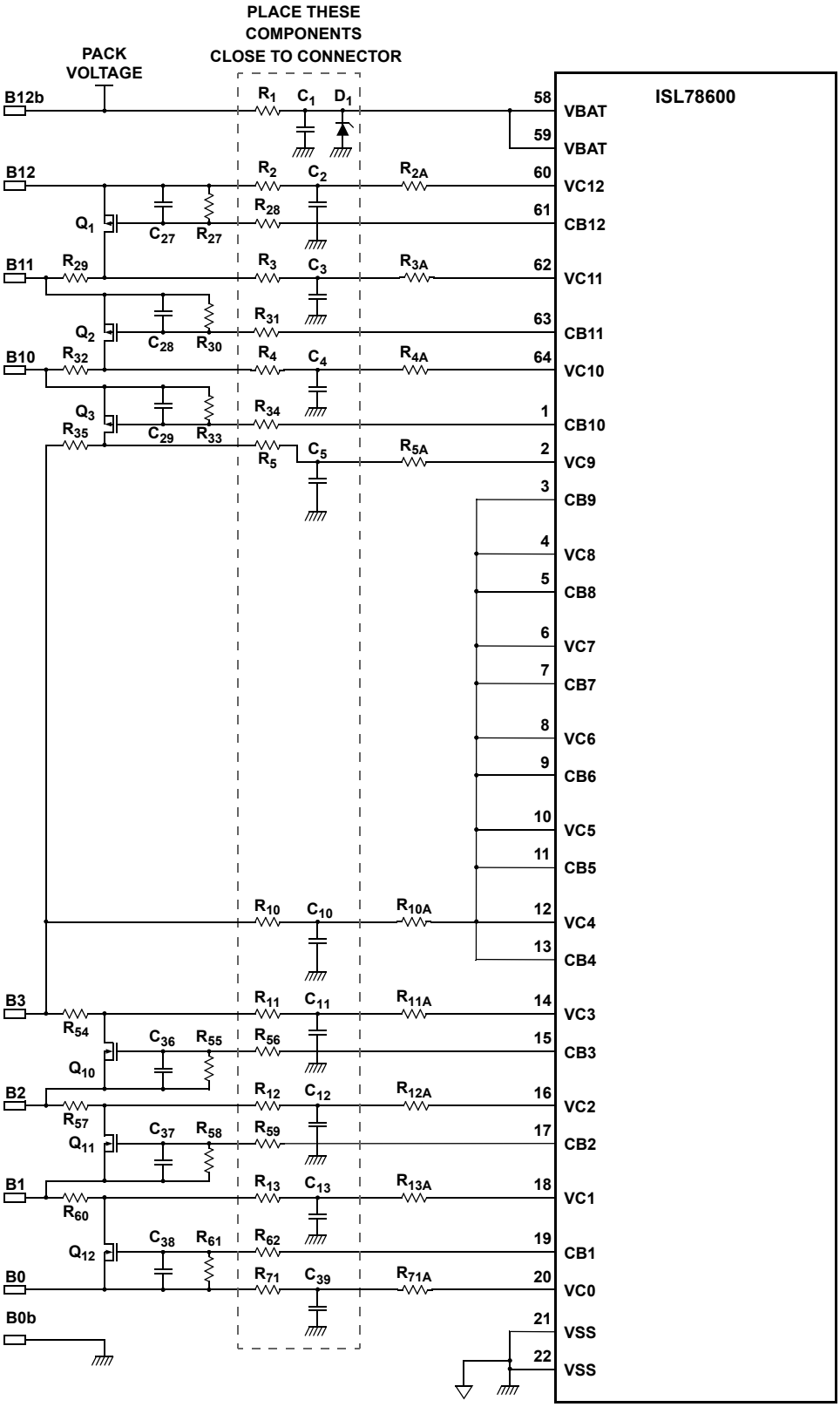


Figure 57. Typical 6 Cell Battery Connection Circuit

Table 13. Recommended Component Values for Circuits in (Figure 52 through Figure 57)

Value		Components
Resistors		
0		R_{101}
27		R_1
33		R_{82}
820		R_2, R_{71}
720	Figure 51 on page 41, Figure 55 on page 45, Figure 56 on page 46	R_3, R_4, R_6, R_7, R_8, R_9, R_{10}, R_{11}, R_{12}, R_{13}
1.54k		R_{5U}, R_{5L}
180		R_{2A}, R_{3A}, R_{4A}, R_{6A}, R_{7A}, R_{8A}, R_{9A}, R_{10A}, R_{11A}, R_{12A}, R_{13A}
360		R_{5AU}, R_{5AL}
910	Figure 54 on page 44	R_3, R_4, R_5, R_6, R_7, R_8, R_9, R_{10}, R_{11}, R_{12}, R_{13}
180		R_{2A}, R_{3A}, R_{4A}, R_{5A}, R_{6A}, R_{7A}, R_{8A}, R_{9A}, R_{10A}, R_{11A}, R_{12A}, R_{13A}
100	1/2W (or larger)	R_{29}, R_{32}, R_{35}, R_{36}, R_{39}, R_{42}, R_{45}, R_{48}, R_{51}, R_{54}, R_{57}, R_{60}
1.3k		R_{81} (assumes minimum pack voltage of 12V and maximum supply current of 6.5mA. Higher current or lower minimum pack voltage requires the use of a smaller resistor.)
100		R_{63}, R_{64}, R_{67}, R_{68}
1.4k		R_{5U}, R_{5L}
470		R_{65}, R_{66}, R_{69}, R_{70}
10k		R_{28}, R_{31}, R_{34}, R_{38}, R_{41}, R_{44}, R_{47}, R_{50}, R_{53}, R_{56}, R_{59}, R_{62}, R_{83}, R_{84}, R_{85}, R_{86}, R_{87}, R_{90}, R_{93}, R_{96}, R_{100a}, R_{100b}, R_{100c}, R_{100d}
330k		R_{27}, R_{30}, R_{33}, R_{37}, R_{40}, R_{43}, R_{46}, R_{49}, R_{52}, R_{55}, R_{58}, R_{61}
Capacitors		
Value	**Voltage**	**Components**
200p	100	C_{42}, C_{43}, C_{49}, C_{50}
220p	500	C_{44}, C_{45}, C_{51}, C_{52}
10n	50	C_{27}, C_{28}, C_{29}, C_{30}, C_{31}, C_{32}, C_{33}, C_{34}, C_{35}, C_{36}, C_{37}, C_{38}, C_{58}, C_{59}, C_{60}, C_{61}
22n	100	C_2, C_3, C_4, C_5, C_6, C_7, C_8, C_9, C_{10}, C_{11}, C_{12}, C_{13}, C_{39}
220n	100	C_1
1µ	10	C_{53}, C_{54}, C_{56}
1µ	100	C_{55}
2.2µ	10	C_{57}
Zener Diodes		
Value	**Example**	**Components**
54V	PTVS54VS1UTR	D_1 - DIODE-TVS, SMD, 2P, SOD-123W, 54VWM, 87.1VC

4.8 Board Layout Notes

For Figure 52 on page 42 (battery connection circuits), the basic input filter structure is composed of resistors R_2 to R_{13}, R_{71}, and capacitors C_2 to C_{13} and C_{39}. These components provide protection against transients and EMI for the cell inputs. They carry the loop currents produced by EMI and should be placed as close to the connector as possible. The ground terminals of the capacitors must be connected directly to a solid ground plane. Do not use vias to connect these capacitors to the input signal path or to ground. Any vias should be placed in line to the signal inputs so that the inductance of these forms a low pass filter with the grounded capacitors.

For Figure 53 on page 43, the daisy chain components are shown to the top right of the drawing. These are split into two sections. Components to the right of this section should be placed close to the board connector with the

ground terminals of capacitors connected directly to a solid ground plane. This is the same ground plane that serves the cell inputs. Components to the left of this section should be placed as closely to the device as possible.

The battery connector and daisy chain connectors should be placed closely to each other on the same edge of the board to minimize any loop current area.

Two grounds are identified on the circuit diagram. These are nominally referred to as noisy and quiet grounds. The noisy ground, denoted by an “earth” symbol carries the EMI loop currents and digital ground currents while the quiet ground is used to define the decoupling voltage for voltage reference and the analog power supply rail. The quiet and noisy grounds should be joined at the VSS pin. Keep the quiet ground area as small as possible.

The circuits shown to the bottom right of Figure 53 on page 43 provide signal conditioning and EMI protection for the external temperature inputs. These inputs are designed to operate with external NTC thermistors.

Each of the external inputs has an internal pull-up resistor, which is connected by a switch to the VCC pin whenever the TEMPREG output is active. This arrangement results in an open input being pulled up to the V_{CC} voltage.

4.9 Component Selection

Certain failures associated with external components can lead to unsafe conditions in electronic modules. A good example of this is a component that is connected between high energy signal sources failing short. Such a condition can easily lead to the component overheating and damaging the board and other components in its proximity.

One area to consider with the external circuits on the ISL78600 is the capacitors connected to the cell monitoring inputs. These capacitors are normally protected by the series protection resistors but could present a safety hazard in the event of a dual point fault where both the capacitor and associated series resistor fail short. Also, a short in one of these capacitors would dissipate the charge in the battery cell if left uncorrected for an extended period of time. It is recommended that capacitors C_1 to C_{13} be selected to be “fail safe” or “open mode” types. An alternative strategy would be to replace each of these capacitors with two devices in series, each with double the value of the single capacitor.

A dual point failure in the balancing resistors (R_{29}, R_{32}, R_{35}, etc.) of Figure 52 on page 42 and associated balancing MOSFET (Q_1 to Q_{12}) could also give rise to a shorted cell condition. It is recommended that the balancing resistor be replaced by two resistors in series.

4.10 Board Level Calibration

For best accuracy, the ISL78600 can be re-calibrated after soldering to a board using a simple resistor trim. The adjustment method involves obtaining the average cell reading error for the cell inputs at a single temperature and cell voltage value and applying a select on test resistor to zero the average cell reading error.

The adjustment system uses a resistor placed either between VDDEXT and V_{REF} or V_{REF} and VSS as shown in Figure 58. The value of resistor R_1 or R_2 is then selected based on the average error measured on all cells at 3.3V per cell and room temperature such as, with 3.3V on each cell input scan the voltage values using the ISL78600 and record the average reading error (ISL78600 reading – cell voltage value). Table 14 shows the value of R_1 and R_2 required for various measured errors.

To use Table 14, find the measured error value closest to the result obtained with measurements using the ISL78600 and select the corresponding resistor value. Alternatively, if finer adjustment resolution is required then this can be obtained by interpolation using Table 14.

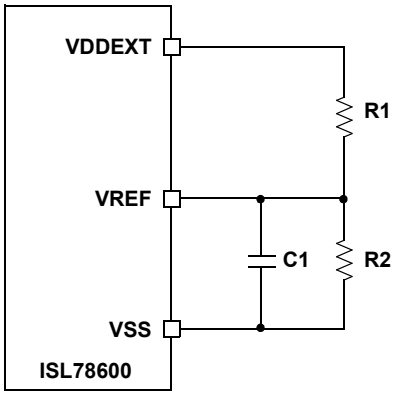


Figure 58. Cell Reading Accuracy Adjustment System

Table 14. Component Values for Accuracy Calibration Using Circuit of Figure 58

Measured Error at VCELL = 3.3V V_{78600} - V_{Meter} (mV)	R_1 (kΩ)	R_2 (kΩ)
4	205	DNP
3	274	DNP
2	412	DNP
1	825	DNP
0	DNP	DNP
-1	DNP	2550
-2	DNP	1270
-3	DNP	866
-4	DNP	649

Note: DNP = Do Not populate

5. System Commands

To control the operation of the ISL78600 system, to read and write data to any individual device, and to check system status, the ISL78600 has a series of commands available to the host microcontroller. There are four types of commands,

- Action commands that tell a device or a stack of devices to perform a specific operation. These commands respond with an “ACK” when the command has been successfully executed.
- Write commands load data into the register and device specified in the command. This command returns an ACK response when successfully executed.
- Read commands that return one or more bytes to the host. This command returns data corresponding to the contents of the device register.
- Scan commands that tell a device or a stack of devices to perform a scan operation. These commands do not have a response, but instead increment a scan counter when successfully executed.

These commands are listed in Table 15 on page 52 along with characteristics of the command. Each command is individually described in Sections below.

The attributes associated with each command are: the device response, whether the command can address all devices with a single command, and whether there is a response from the target device.

5.1 Device Response

In a stand-alone configuration, the host should only expect a response when reading data from a register. In all other cases, there is no response expected.

In a daisy chain configuration, all commands except Scan Voltages, Scan Temperatures, Scan Mixed, Scan Wires, Scan All, Measure, and Reset respond from either the stack Top device or the target device (see Table 15). Each device in the stack waits for a response from the stack device above. Correct receipt of a command is indicated by the correct response. The Wakeup command is a special case. If any Daisy Chain Middle device is in Sleep mode, while another device above it in the stack is not in Sleep mode, there is no response. Otherwise the Wakeup command responds with ACK.

When a device fails to receive a response from the device above within a timeout period, then that device transmits a Communications Failure response (which is identical to the response of a Read Status Register) back down the stack to the Master. The timeout value is stack position dependent.

The host microcontroller should build in handlers for commands that might be delayed within the communication structure and look for a Communications Failure response if the wait time expires. For more detail, see “Communication Faults” on page 103.

An Acknowledge (ACK) response indicates that the command was successfully received by the target device. A Not Acknowledge (NAK) indicates that there was an error in decoding the command.

Table 15. Command Attributes

Command	Valid In Standalone or Daisy Chain	Normal Device Response			Address All Compatible (Daisy Chain Only)	Increments Scan Counter
		Standalone	Top	Target		
Scan Voltages	Both	-	-	-	Yes	Yes
Scan Temperatures	Both	-	-	-	Yes	Yes
Scan Mixed	Both	-	-	-	Yes	Yes
Scan Wires	Both	-	-	-	Yes	Yes
Scan All	Both	-	-	-	Yes	Yes
Measure	Both	-	-	-	No	Yes
Reset	Both	-	-	-	No	No
Wakeup	Both	-	Note 13	Note 14	“Address All” Only	No
Sleep	Both	-	ACK	NAK	“Address All” Only	No
Identify (special command)	Daisy chain only	-	ACK	NAK	Special address	No
NAK	Daisy chain only	-	ACK	ACK	No	No
ACK	Daisy chain only	-	ACK	ACK	No	No
Read	Both	Data	ACK	Data	No	No
Write	Both	-	ACK	ACK	No	No
Scan Continuous	Both	-	Note 15	Note 15	Yes	No
Scan Inhibit	Both	-	Note 15	Note 15	Yes	No
Balance Enable	Both	-	Note 15	Note 15	Yes	No
Balance Inhibit	Both	-	Note 15	Note 15	Yes	No
Calculate Register Checksum	Both	-	ACK	ACK	No	No
Check Register Checksum	Both	-	ACK	ACK	No	No

13. If any Daisy Chain Middle stack device is asleep, but any device above it in the stack is not, there is no response. Otherwise, the response is “ACK”.
14. This is a “non-standard” response, since the command should use “Address All”. However, the target device responds with the Wakeup command if all devices are awake. If any device is in Sleep mode, there is no response.
15. These commands respond with an ACK from the target device. For commands with “Address All” the ACK is from the top device.

5.2 Address All

The “Address All” address is used only in a daisy chain configuration. See “Daisy Chain Commands” on page 69. To address a particular device, the host microcontroller specifies the address of that device (1 through 14) for each of the maximum 14 devices. To address all devices in a daisy chain stack, the host microcontroller uses an address of 15 (Hex ‘1111’) to cause all stack devices to perform functions simultaneously. Only some commands recognize “Address All”.

5.3 Read and Write Commands

Read and write commands are the primary communication mechanisms in the ISL78600 system. All commands use the read and write operations. See “Communications” on page 73 for a detailed description of these operations’ protocols, timing, and interactions.

Table 15 describes the commands and how they control the system.

5.4 Scan Voltages Command

When a device receives the Scan Voltages command to its Device Address (or an “Address All” address), it increments the scan counter (see “Scan Counter” on page 58) and begins a scan of the cell voltage inputs. It sequences through the cell voltage inputs in order from Cell 12 (top) to Cell 1 (bottom). This operation is followed by a scan of the pack voltage.

The scan operation forces a sample and hold on each input, an analog-to-digital conversion of the voltage, and the storage of the value in its appropriate register. The IC temperature is also recorded for use with the internal calibration routines.

The scan voltages command performs cell overvoltage and undervoltage comparisons on each cell input and checks the V_{BAT} and VSS connections for open wire at the end of the scan. If there is a fault condition (see "Fault Diagnostics" on page 107 for what constitutes a fault condition), the device sets the specific fault bit, sets the device $\overline{FAULT}$ pin active, and sends an "unprompted fault response" to the host down the daisy chain communication link. (A stand-alone device only sets the $\overline{FAULT}$ pin). The unprompted response is identical to a "read status register" command.

Devices revert to the standby state on completion of the scan activity.

Cell voltage and Pack Voltage data, along with any fault conditions are stored in local memory ready for reading by the system host microcontroller.

5.5 Scan Temperatures Command

When a device receives the Scan Temperatures command to its Device Address (or an "Address All" address), it increments the Scan counter (see "Scan Counter" on page 58) and begins a scan of the temperature inputs.

The Scan Temperatures command causes the addressed device (or all devices with an "Address All" address) to scan through the internal and four external temperature signals followed by multiplexer loopback and reference measurements. The loopback and reference measurements are part of the internal diagnostics function. Over-temperature compares are performed on each temperature measurement depending on the condition of the appropriate bit in the Fault Setup register.

Temperature data and any fault conditions are stored in local memory ready for reading by the system host microcontroller. If there is a fault condition, the device sets its $\overline{FAULT}$ pin active and on completion of a scan sends an "unprompted fault response" to the host down the daisy chain communication link. (A stand-alone device only sets the $\overline{FAULT}$ pin.) The unprompted response is identical to a "Read Status Register" command.

Devices revert to the standby state on completion of the scan activity.

See "Temperature Monitoring Operation" on page 58.

5.6 Scan Mixed Command

When a device receives the Scan Mixed command to its Device Address (or an "Address All" address), it increments the scan counter (see "Scan Counter" on page 58) and begins a Scan Mixed operation.

The Scan Mixed command causes the addressed device (or all devices with an "Address All" address) to scan through the cell voltage inputs in order from Cell 12 (top) to Cell 7. Then the external input ExT1 is measured, followed by a scan of Cell 6 to Cell 1. These operations are followed by a scan of the pack voltage and the IC temperature. The IC temperature is recorded for use with the internal calibration routines.

Scan Mixed also performs cell overvoltage and undervoltage comparisons on each cell voltage sampled. The V_{BAT} and VSS pins are also checked for open conditions at the end of the scan.

ExT1 is sampled in the middle of the cell voltage scan such that half the cells are sampled before ExT1 and half after ExT1. This mode allows ExT1 to be used for an external voltage measurement, such as a current sensing, so it is performed along with the cell voltage measurements, reducing the latency between measurements.

The Scan Mixed command is intended for use in stand-alone systems, or by the Master device in stacked applications, and would typically measure a single system parameter, such as battery current or pack voltage.

Cell voltage, pack voltage and ExT1 data, along with any fault conditions are stored in local memory ready for reading by the system host microcontroller. Access the data from the ExT1 measurement by a direct Read ET1 Voltage command or by the All Temperatures read command.

If there is a fault condition, (see "Fault Diagnostics" on page 107 for what constitutes a fault condition), the device sets the $\overline{FAULT}$ pin active, and on completion of a scan sends an "unprompted fault response" to the host down

the daisy chain communication link. (A stand-alone device only sets the $\overline{\text{FAULT}}$ pin). The unprompted response is identical to a “Read Status Register” command.

Devices revert to the standby state on completion of the scan activity.

5.7 Scan Wires Command

When a device receives the Scan Wires command to its Device Address (or an “Address All” address), it increments the Scan counter (see “Scan Counter” on page 58) and begins a Scan Wires operation.

The Scan Wires command causes the addressed device (or all devices with an “Address All” address) to measure all the VCn pin voltages, while applying load currents to each input pin in turn. This is part of the fault detection system.

If there is a fault condition, the device sets the $\overline{\text{FAULT}}$ pin and returns a fault signal (sent down the stack) on completion of a scan.

No cell voltage data is sent as a result of the Scan Wires command. Devices revert to the standby state on completion of this activity.

5.8 Scan All Command

When a device receives the Scan All command to its Device Address (or an “Address All” address), it increments the Scan counter (see “Scan Counter” on page 58) and begins a Scan All operation.

The Scan All command causes the addressed device (or all devices with an “Address All” address) to execute the Scan Voltages, Scan Wires, and Scan Temperatures commands in sequence one time (see Figure 59 on page 59 for example timing).

5.9 Scan Continuous Command

Scan Continuous mode is used primarily for fault monitoring and incorporates the Scan Voltages, Scan Temperatures, and Scan Wires commands.

See “Temperature Monitoring Operation” on page 58.

The Scan Continuous command causes the addressed device (or all devices when using an “Address All” address) to set the SCAN bit in the Device Setup register and performs a succession of scans at a predetermined scan rate. Each device operates asynchronously on its own clock. This is similar to the Scan All command except that the scans are repeated at intervals determined by the SCN0-3 bits in the Fault Setup register.

The ISL78600 provides an option that pauses cell balancing activity while measuring cell voltages in Scan Continuous mode. This is controlled by the BDDS bit in the Device Setup register. If BDDS is set, then cell balancing is inhibited during cell voltage measurement and for 10ms before the cell voltages are scanned. Balancing is re-enabled at the end of the scan to allow balancing to continue. This function applies during Scan Continuous and while either the Timed or Auto Balance functions are active. This “BDDS” action allows the implementation of a circuit arrangement that can be used to diagnose the condition of external balancing components (see “Cell Voltage Measurements during Balancing” on page 33). During Manual Balance this external circuit arrangement does not allow Scan Continuous without generating a fault condition. It is also up to the host microcontroller to stop balancing functions when performing a Scan or Measure command, as BDDS only works in conjunction with Scan Continuous.

The Scan Continuous scan interval is set using the SCN3:0 bits (lower nibble of the Fault Setup register.) The temperature and wire scans occur at slower rates and depend on the value of the scan interval selected. The scan system is synchronized so that the wire and temperature scans always follow a voltage scan. The three scan sequences, depending on the scans required at a particular instance, are as follows:

- Scan voltages
- Scan voltages, scan wires
- Scan voltages, scan wires, scan temperatures.

The temperature and wire scans occur at 1/5 the voltage scan rate for voltage scan intervals above 128ms. Below this value the temperature scan interval is fixed at 512ms.

The behavior of the wire scan interval is determined by the WSCN bit in the Fault Setup register. A bit value of ‘1’ causes the wire scan to be performed at the same rate as the temperature scan. A bit value of ‘0’ causes the wire scan rate to track the voltage scan rate for voltage scan intervals above 512ms while the wire scan is performed at a fixed 512ms rate at voltage scan intervals below this value. Table 16 shows the various scan rate combinations available.

Table 16. Scan Continuous Timing Modes

Scan Interval SCN3:0	Scan Interval (ms)	Temperature Scan (ms)	Wire Scan (ms) WSCN = 0	Wire Scan (ms) WSCN = 1
0000	16	512	512	512
0001	32	512	512	512
0010	64	512	512	512
0011	128	512	512	512
0100	256	1024	512	1024
0101	512	2048	512	2048
0110	1024	4096	1024	4096
0111	2048	8192	2048	8192
1000	4096	16384	4096	16384
1001	8192	32768	8192	32768
1010	16384	65536	16384	65536
1011	32768	131072	32768	131072
1100	65536	262144	65536	262144

Data is not automatically returned to the host microcontroller while devices are in Scan Continuous mode except when a fault condition is detected. The results of voltage and temperature scans are stored in local volatile memory and can be accessed at any time by the system host microcontroller. However, because the scan continuous operation is running asynchronously to any communications, it is recommended that the continuous scan be stopped before reading the registers.

Devices can be operated in Scan Continuous mode while in Normal mode or in Sleep mode. Devices revert to Sleep mode or remain in Normal mode, as applicable on completion of each scan.

To operate the “Scan Continuous” function in Sleep mode the host microcontroller configures the ISL78600, starts the Scan Continuous mode, and then sends the Sleep command. The ISL78600 then wakes itself up each time a scan is required. Note that it is recommended that the fastest times (scan interval codes 0000, 0001, and 0010) NOT be used when in Scan Continuous + Sleep mode, because in the fastest scan settings the main measurement functions do not power down between scans and remains in Normal mode.

While in Scan Continuous mode, the device responds to a detected fault condition by setting the Fault bits and setting the FAULT pin active.

For a stand-alone device, the host should monitor the FAULT pin, since this is the only indication that a fault occurred. A stand-alone device in the Scan Continuous + Sleep state remains in the same state, i.e. the device does not “Wake up” if a fault occurs.

For daisy chain devices in Scan Continuous mode, the device with a fault sends a Fault response signal to the Master. A Fault response signal is the same as the response to a Read Status Register command from the device with the fault. The host, seeing this “unprompted” response would poll the Status register of the device with the fault to determine specifics about the fault.

For daisy chain devices in Scan Continuous + Sleep mode, the device with a fault sends out a wakeup signal up and down the chain. This wakes all devices in the stack. The Top device then sends an ACK to the Master. The host, seeing this “unprompted” ACK would poll the Status register in each device to determine where the fault occurred. When the fault is cleared, the host needs to re-send the Sleep command to resume Scan Continuous + Sleep operations.

5.10 Scan Inhibit Command

The Scan Inhibit command stops a Continuous scan (that is, receipt of the command by the target device resets the SCAN bit and stops the Scan Continuous function).

Notes:

- If the stack is in a Scan Continuous + Sleep mode, the host should send the Wakeup command before sending the Scan Inhibit command.
- After sending a Scan Inhibit command, following a previous Scan Continuous command, the ISL78600 can re-enter a Scan Continuous + Sleep mode but cannot enter Sleep (only) mode. To re-enable Sleep mode requires resetting all devices (Reset command or EN toggle) or waiting for the expiration of the Watchdog timer (for Daisy Chained devices).

5.11 Measure Command

When a device receives the Measure command to its Device Address, it increments the Scan counter (see “Scan Counter” on page 58) and begins a Measure operation.

This command initiates the voltage measurement of a single cell voltage, internal temperature, any of the four external temperature inputs, or the secondary voltage reference. The command incorporates a 6-bit suffix that contains the address of the required measurement element. See Table 17 and Figure 66 on page 75.

The device matching the target address responds by conducting the single measurement and loading the result to local memory. The host microcontroller then reads from the target device to obtain the measurement result. All devices revert to the Standby state on completion of this activity.

Table 17. Measure Command Target Element Addresses

Measure Command (Suffix)	Description
6'h00	V_{BAT} voltage
6'h01	Cell 1 voltage
6'h02	Cell 2 voltage
6'h03	Cell 3 voltage
6'h04	Cell 4 voltage
6'h05	Cell 5 voltage
6'h06	Cell 6 voltage
6'h07	Cell 7 voltage
6'h08	Cell 8 voltage
6'h09	Cell 9 voltage
6'h0A	Cell 10 voltage
6'h0B	Cell 11 voltage
6'h0C	Cell 12 voltage
6'h10	Internal temperature reading.
6'h11	External temperature Input 1 reading.
6'h12	External temperature Input 2 reading.
6'h13	External temperature Input 3 reading.
6'h14	External temperature Input 4 reading.
6'h15	Reference voltage (raw ADC) value. Use this value to calculate corrected reference voltage using reference coefficient data.

5.12 Scan Counter

Because the Scan and Measure commands do not have a response, the scan counter is provided to allow confirmation of receipt of the Scan and Measure commands. This is a 4-bit counter located in the Scan Count register (page 1, address 6'h16). The counter increments each time a Scan or Measure command is received. This allows the host microcontroller to compare the counter value before and after the Scan or Measure command was sent to verify receipt. The counter wraps to zero when overflowed.

The Scan Counter increments whenever the ISL78600 receives a Scan or Measure command. The ISL78600 does not perform a requested Scan or Measure function if a Scan or Measure function is already in progress, but it still increments the Scan Counter.

5.13 Temperature Monitoring Operation

One internal and four external temperature inputs are provided together with a switched bias voltage output (TEMPREG, pin 29). The voltage at the TEMPREG output is nominally equal to the ADC reference voltage such that the external voltage measurements are ratiometric to the ADC reference (see Figure 50 on page 39).

The temperature inputs are intended for use with external resistor networks using NTC type thermistor sense elements but can also be used as general purpose analog inputs. Each temperature input is applied to the ADC through a multiplexer. The ISL78600 converts the voltage at each input and loads the 14-bit result to the appropriate register.

The TEMPREG output is turned "on" in response to a Scan Temperatures or Measure temperature command. A dwell time of 2.5ms is provided to allow external circuits to settle, after which the ADC measures each external input in turn. The TEMPREG output turns "off" after measurements are completed.

Figure 59 shows an example temperature scan with the ISL78600 operating in Scan Continuous mode with a scan interval of 512ms. The preceding voltage and wire scans are shown for comparison.

The external temperature inputs are designed such that an open connection results in the input being pulled up to the full scale input level. This function is provided by a switched 10MΩ pull-up from each input to VCC. This feature is part of the fault detection system and is used to detect open pins.

The internal IC temperature, Auxiliary Reference Voltage, and multiplexer loopback signals are sampled in sequence with the external signals using the Scan Temperatures command.

The converted value from each temperature input is also compared to the external over-temperature limit and open connection threshold values on condition of the [TST4:1] bits in the Fault Setup register (see Table 46 on page 101) If a TSTn bit is set to "1", then the temperature value is compared to the External Temperature threshold and a Fault occurs if the measured value is lower than the threshold value. If a TSTn bit is set to "0", then the temperature measurement is not compared to the threshold value and no fault occurs. The [TST4:1] bits are "0" by default.

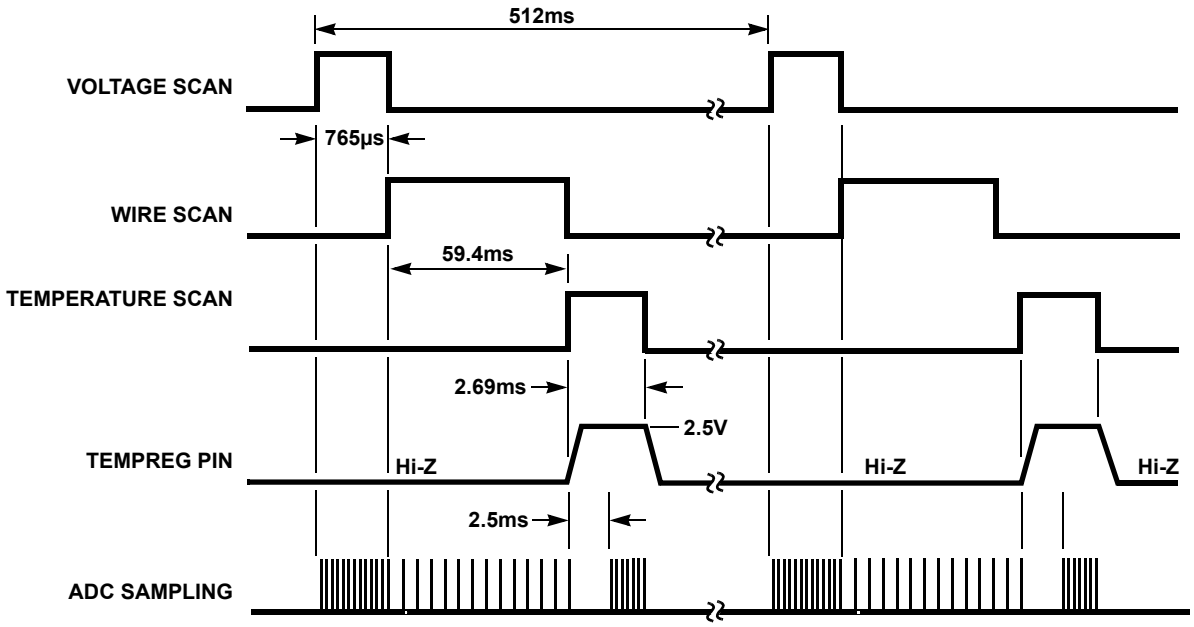


Figure 59. Scan Timing Example During Scan Continuous Mode or for Scan All Command

5.14 Sleep Command

Sleep mode is entered in response to a Sleep command. Only the communications input circuits, low speed oscillator, and internal registers are active in Sleep mode, allowing the part to perform timed scan and balancing activity and to wake up in response to communications.

Using a Sleep command does not require that the devices in a daisy chain stack be identified first. They do not need to know their position in the stack.

In a daisy chain system, the Sleep command must be written using the “Address All” address. The command is not recognized if sent with an individual device address and causes the addressed device to respond NAK. The Top stack device responds ACK on receiving a valid Sleep command.

After receiving a valid Sleep command, devices wait before entering Sleep mode. This is to allow time for the top stack device in a daisy chain to respond ACK, or for all devices that do not recognize the command to respond NAK, and for the host microcontroller to respond with another command. Receipt of any valid communications on Port 1 of the ISL78600 before the wait period expires cancels the Sleep command. Receipt of another Sleep command restarts the wait timers. Table 18 provides the maximum wait time for various daisy chain data rates. The communications fault checking timeout is not applied to the Sleep command. A problem with the communications is indicated by a lack of response to the host microcontroller. The host microcontroller may choose to do nothing if no response is received in which case devices that received the Sleep command go to sleep when the wait time expires. Devices that do not receive the message go to sleep when their watchdog timer expires (if this is enabled).

Devices exit Sleep mode on receipt of a valid Wakeup command.

Table 18. Maximum Wait Time for Devices Entering Sleep Mode

Parameter	Daisy Chain Data Rate (kHz)				Unit
	500	250	125	62.5	
Maximum Time from transmission of Sleep Command to Enter Sleep Mode	500	1000	2000	4000	µs

5.15 Wakeup Command

The communications pins are monitored when the device is in Sleep mode, allowing the part to respond to communications.

The host microcontroller wakes up a sleeping device, or a stack of sleeping devices, by sending the Wakeup command to a Stand-alone or a master stack device. In a daisy chain configuration, the Wakeup command should be written using the “Address All” address. Sending a Wakeup command with an individual address does not work. If all devices in the stack are in Normal or Sleep mode, then a Wakeup command responds with an ACK. If any Mid device in the stack is in Sleep mode, while devices above it are awake, then a Wakeup command has no response. A Wakeup command with a specific Device Address, when all devices are awake, returns the Wakeup command from that target device.

Using a Wakeup command does not require that the devices in a stack be identified first. They do not need to know their position in the stack.

The master exits Sleep mode on receipt of a valid Wakeup command and proceeds to transmit the Wakeup signal to the next device in the stack. The Wakeup signal is a few cycles of a 4kHz clock. Each device in the chain wakes up on receipt of the Wakeup signal and proceeds to send the signal on to the next device.

Any communications received on Port 1 by a device, which is transmitting the Wakeup signal on Port 2 are ignored.

The Top stack device, after waking up, waits for some time before sending an ACK response to the master. This wait time is necessary to allow receipt of the Wakeup signal being originated by a stack device other than the master. See “Fault Diagnostics” on page 107 for more information.

The master device passes the ACK on to the host microcontroller to complete the Wakeup sequence. The total time required to wake up a complete stack of devices is dependent on the number of devices in the stack. Table 19 gives the maximum time from Wakeup command transmission to receipt of an ACK response ($\overline{\text{DATA READY}}$ asserted low) for stacks of 3 devices, 8 devices, and 14 devices at various daisy chain data rates (interpolate linearly for different number of devices).

Table 19. Maximum Daisy Chain Wakeup Times

Maximum Wakeup Command to Devices Awake For:	Daisy Chain Data Rate (kHz)				Unit
	500	250	125	62.5	
Stack of 3 Devices	33	33	33	33	ms
Stack of 8 Devices	63	63	63	63	ms
Stack of 14 Devices	100	100	100	100	ms

There is no additional checking for communications faults while devices are waking up.

5.16 Reset Command

The Reset command performs a Software reset of the device. All digital registers are reset to their power-up condition and all Device Address and Stack Size information registers are set to zero in response to a Reset command.

Daisy chain devices must be reset in sequence from top stack device to stack bottom (master) device. Sending the Reset command to all devices using the “Address All” address has no effect and there is no response to the command.

After all devices have received the reset command:

1. The host sends the sequence of Identify commands.
2. The host checks the EEPROM MISR Data Register and MISR Calculated Checksum register on all devices. These two register values should match.
3. The host re-loads configuration settings (other than default values) in each device volatile memory.

4. The host sends the Calculate Register Checksum command to generate a new checksum for the volatile memory on each device.
5. The host sends the Check Register Checksum command to check that the checksum matches. The host can resend this command at any time to determine if there have been changes in the volatile memory contents. If there have been the device sends a fault response to the host.

5.17 Calc Register Checksum

The host sends this command to each device to re-calculate the checksum of the volatile registers. This should be done, whenever all changes have been made to the non-volatile registers, such as for the Over Voltage or Under Voltage limits. (See “Memory Checksum” on page 102.)Jun.12.20

5.18 Check Register Checksum

The host sends this command to check that the checksum for the volatile registers is unchanged from the last calculation.

5.19 Balance Enable Command

The Balance Enable Command sets the BEN bit, which starts the balancing operation. However, before this command becomes operational and before balancing can commence, the balance operation needs to be specified. See Cell Balancing Functions

The Balance Enable command can be sent to all devices with one command using Address All addressing.

5.20 Balance Inhibit Command

The Balance Inhibit Command clears the BEN bit, which stops the balancing operation. The Balance Inhibit command can be sent to all devices with one command using Address All addressing.

5.21 Cell Balancing Functions

Cell balancing is performed using external MOSFETs and external current balancing resistors (see Figure 52 on page 42). Each MOSFET is controlled independently by the CB1 to CB12 pins of the ISL78600. The CB1 to CB12 outputs are controlled either directly, or indirectly by an external microcontroller through bits in various control registers.

The three cell balance modes are Manual, Timed, and Auto.

Table 20. Registers Controlling Balance

REGISTER	BALANCE MODE	REFERENCE
Balance Setup	Manual, Timed, Auto	Table 21 on page 63
Balance Status	Manual, Timed, Auto	Table 21 on page 63
Watchdog/Balance Time	Timed, Auto	Table 23 on page 65
Device Setup	Timed, Auto	“Setup Registers” on page 124
Balance Value	Auto only	Table 24 on page 67

5.21.1 Balance Mode

Set the Balance mode with the BMD1 and BMD0 bits in the Balance Setup Register. See Table 21 on page 63.

In Manual mode, the host microcontroller directly controls the state of each MOSFET output.

In Timed mode, the host microcontroller programs a balance duration value and selects which cells are to be balanced, then starts the balance operation. The ISL78600 turns all the FETs off when the balance duration has been reached.

In Auto Balance mode, the host microcontroller programs the ISL78600 to control the balance MOSFETs to remove a programmed “charge delta” value from each cell. The ISL78600 does this by controlling the amount of charge removed from each cell over a number of cycles, rather than trying to balance all cells to a specific voltage.

5.21.2 Balance Wait Time

The balance wait time is the interval between balancing operations in Auto Balance mode. See Table 21 on page 63.

5.21.3 Balance Enable

When all of the other balance control bits are properly set, setting the balance enable bit (BEN) to “1” starts the balance operation. The BEN bit can be set by writing directly to the Balance Setup register or by sending a Balance Enable command. See Table 21 on page 63.

5.21.4 Balance Status Register

The Balance Status register contents control which external balance FET is turned on during a balance event. Each of the 12 bits in the Balance Status register controls one external balancing FET, such that Bit 0 [BAL1] controls the FET for Cell 1 and Bit 11 [BAL12] controls the FET for Cell 12. Bits are set to ‘1’ to enable the balancing for that cell and cleared to ‘0’ to disable balancing.

5.21.5 Balance Status Pointer

The Balance Status register is a “multiple instance” register. See Balance Status Register. There are 13 locations within this register and only one location can be accessed at a time. The balance status pointer in the Balance Setup Register points to one of these 13 locations (see Table 21 on page 63).

Manual Balance mode and Timed Balance mode require a balance status pointer value of ‘0’. In this case, the bits in the balance status register directly select the cells to be balanced.

The Auto Balance mode uses Balance Status register locations 1 to 12 (see Table 21 on page 63). In Auto Balance mode, the ISL78600 increments the Balance status pointer on each auto balance cycle to step through Balance Status register locations 1 to 12. This allows the programming of up to twelve different balance profiles for each Auto Balance operation. When the operation encounters a zero value at a pointer location, the auto balance operation returns to the pattern at location 1 and resumes balancing with that pattern.

More information about the auto balance mode is provided in “Auto Balance Mode” on page 65. Example balancing setup information is provided in “Auto Balance Mode Cell Balancing Example” on page 113.

Table 21. Balance Setup Register

Register Bits													
9		8	7	6	5		4	3	2		1	0	
BEN	Balance	BSP3	BSP2	BSP1	BSP0	Point to Register	BWT2	BWT1	BWT0	Seconds Between Balance Cycles	BMD1	BMD0	Balance Mode
0	Off	0	0	0	0	Balance Status 0 12 11 10 9 8 7 6 5 4 3 2 1 Set bit to 1 to enable balance	0	0	0	0	0	0	Off
1	On	0	0	0	1	Balance Status 1	0	0	1	1	0	1	Manual
		0	0	1	0	Balance Status 2	0	1	0	2	1	0	Timed
		0	0	1	1	Balance Status 3	0	1	1	4	1	1	Auto
		0	1	0	0	Balance Status 4	1	0	0	8			
		0	1	0	1	Balance Status 5	1	0	1	16			
		0	1	1	0	Balance Status 6	1	1	0	32			
		0	1	1	1	Balance Status 7	1	1	1	64			
		1	0	0	0	Balance Status 8							
		1	0	0	1	Balance Status 9							
		1	0	1	0	Balance Status 10							
		1	0	1	1	Balance Status 11							
		1	1	0	0	Balance Status 12							

Manual/Timed

Auto Balance Mode Only

5.22 Manual Balance Mode

In Manual Balance mode, the host microcontroller specifies which cell is balanced and controls when balancing starts and stops.

To manually control the cells to be balanced, do the following:

1. Set the Balance mode bits to ‘01’ for “Manual”.
2. Set the Balance Status Pointer to zero.
3. Set bits in the Balance Status register to program the cells to be balanced (such as, to balance Cell 5, set the BAL5 bit to 1).
4. Enable balancing, either by setting the BEN bit in the Balance Setup register or by sending a Balance Enable command.
5. Disable balancing either by resetting the *BEN* bit or by sending a Balance Inhibit command.

The Balance Enable and Balance Inhibit commands can be used with the “Address All” device address to control all devices in a stack simultaneously.

The ISL78600 has a watchdog timer function that protects the battery from excess discharge due to balancing. In the event that communications is lost, the watchdog begins a countdown. If the timeout value is exceeded while the part is in Manual Balance mode all balancing ceases and the device goes into Sleep mode (see Table 22).

If the device was performing a manual balance operation prior to a Sleep Command, then receiving a Wake command resumes balancing.

Manual Balance mode cannot operate while the ISL78600 is in Sleep mode. If the watchdog timer is off and the Sleep command is received during Manual balance, then balancing stops immediately and the device goes into Sleep mode.

If the watchdog timer is active during Manual balance and the device receives the Sleep command, then balancing stops immediately and the device goes into Sleep mode, but the WDTM bit is set when the watchdog timer expires (see Table 22).

5.23 Timed Balance Mode

In Timed Balance mode, the host microcontroller specifies which cells are to be balanced and sets a balance time out period. Balancing starts by control of the microcontroller and stops at the end of a time out period (or by command from the microcontroller.)

To set up a timed balance operation, do the following:

1. Set the Balance mode bits to ‘10’ for “Timed”
2. Set the Balance Status Pointer to zero
3. Set bits in the Balance Status register to program the cells to be balanced. (For example, to balance Cells 7 and 10, set BAL7 and BAL10 bits to 1.)
4. Set the balance on time. The balance on time is programmable in 20 second intervals from 20 seconds to 42.5 minutes using BTM[6:0] bits (see Table 23 on page 65).
5. Enable balancing, either by setting the BEN bit in the Balance Setup register or by sending a Balance Enable command. When BEN is reasserted, or when a new Balance Enable command is received, balancing resumes, using the full time specified by the BTM[6:0] bits.
6. Disable balancing either by resetting the BEN bit or by sending a Balance Inhibit command. Resetting BEN stops the balancing functions and resets the timer values.
7. When the balance timeout period is met, the End Of Balance (EOB) bit in the Device Setup register is set and BEN is reset.

Table 22. Balance, Sleep, Wakeup, Watchdog Timer Operation

		Balance Mode Response To:		Receive Wake Command In:		
Operating In	**Watchdog Timer**	**Receive Sleep Command**	**Watchdog Times Out**	**Manual Balance**	**Timed Balance**	**Auto Balance**
Normal Mode	Off	Stop balancing Device enters Sleep mode.	N/A	N/A	N/A	N/A
	On	Stop balancing. Device enters Sleep mode. Set the WDTM bit when the watchdog timer expires.	Stop balancing. Device enters Sleep mode. Set the WDTM bit.	N/A	N/A	N/A
Sleep Mode	N/A	N/A	N/A	Resume balancing	Resume balancing Balance time reduced by the time spent in sleep	Resume balancing with auto balance settings suspended during sleep

Table 23. Watchdog/Balance Time Register

Register Bits							
13	12	11	10	9	8	7	
BTM6	BTM5	BTM4	BTM3	BTM2	BTM1	BTM0	Balance Time (Minutes)
0	0	0	0	0	0	0	Disabled
0	0	0	0	0	0	1	0.33
0	0	0	0	0	1	0	0.67
0	0	0	0	0	1	1	1.00
•••							-
1	1	1	1	1	0	1	41.67
1	1	1	1	1	1	0	42.00
1	1	1	1	1	1	1	42.33

Timed Balance mode cannot operate while the ISL78600 is in Sleep mode. If the watchdog timer is off and the Sleep command is received during Manual balance, then balancing stops immediately and the device goes into Sleep mode.

If the watchdog timer is active during Timed balance and the device receives the Sleep command, then balancing stops immediately and the device goes into Sleep mode, but the WDTM bit is set when the watchdog timer expires, (see Table 22 on page 64).

If the watchdog timeout value is exceeded while the part is in Manual Balance mode all balancing ceases and the device goes into Sleep mode (see Table 22).

If the device was performing a Timed balance operation before a Sleep Command, then receiving a Wake command resumes balancing. However, the balance timer continues during Sleep mode, so if the Balance timer expires before a Wake command, then Balance does not resume until the host microcontroller starts another balance cycle.

5.24 Auto Balance Mode

In Auto Balance mode, the host microcontroller specifies an amount of charge to be removed from each cell to be balanced. Balancing starts by control of the microcontroller and stops when all cells have had the specified charge removed (or by command from the microcontroller.)

Auto Balance mode performs balancing autonomously and in an intelligent manner. Thermal issues are accommodated by the provision of auto balance sequencing (see “Auto Balance Sequencing” on page 66), a multiple instance Balance Status register, and a balance wait time.

During Auto Balance mode the ISL78600 cycles through each Balance Status register instance, which turns on the balancing outputs corresponding to the bits set in each Balance Status register instance. While each cell is being balanced, the amount of charge withdrawn is calculated. Balancing stops for a cell when the specified amount of charge has been removed. See “Auto Balance SOC Adjustment value” on page 66.

When Auto Balancing is complete, the End Of Balance (EOB) bit in the Device Setup register is set and BEN bit is reset.

To set up an auto balance operation, do the following:

1. Set the Balance mode bits to ‘11’ for Auto.
2. Set the Balance Status Pointer to ‘1’.
3. Set bits in the Balance Status register to program the cells to be balanced in the first cycle (such as, to balance odd cells, set Bits 1, 3, 5, 7, 9, and 11).

4. Set the Balance Status Pointer to ‘2’.
5. Set bits in the Balance Status register to program the cells to be balanced in the second cycle (such as, to balance even cells, set Bits 2, 4, 6, 8, 10, and 12).
6. Set the Balance Status Pointer to ‘3’.
7. Set bits in the Balance Status register at this location to zero to terminate the sequence. The next cycle goes back to balance at status pointer = 1.
8. Write the B values into the Balance Value Registers for each cell to be balanced.
9. Enable balancing, either by setting the BEN bit in the Balance Setup register or by sending a Balance Enable command.
   When enabled, the ISL78600 cycles through each instance of the Balance Status register for the duration given by the balance timeout. Between each Balance Status register instance, the device does a Scan All operation and inserts a delay equal to the balance wait time. The process continues with the balance status pointer wrapping back to 1, until all the Balance Value registers equal zero. If one cell Balance Value register reaches zero before the others, balancing for that cell stops, but the others continue.
10. Disable balancing either by resetting the BEN bit or by sending a Balance Inhibit command. Resetting BEN, either directly or by using the Balance Inhibit command, stops the balancing functions but maintains the current Balance Value register contents. Auto Balancing continues from Balance Status register location 1 when BEN is reasserted.

5.24.1 Auto Balance Sequencing

The first cycle of the Auto Balance operation begins with the balance status pointer at location 1, specifying the first Balance Status register instance. For the next auto balance cycle, the balance status pointer increments to location 2. For each subsequent cycle, the pointer increments to the next Balance Status register instance, until a zero value instance is encountered. At this point the sequence repeats from the Balance Status register instance at balance status pointer location 1.

For example, using two Balance Status registers, the ISL78600 can balance odd numbered cells during the first cycle and even numbered cells on the second cycle.

There is a delay time between each cycle. This delay is set by the Balance Wait time bits. See Table 21 on page 63.

Cells are balanced with periodic measurements being performed during the balance time interval (see Table 23). These measurements are used to calculate the reduction in State of Charge (SOC) with each balancing cycle.

As individual cells reach their programmed SOC adjustment, that cell balance terminates, but the balance operation continues cycling through all instances until all cells have met their SOC adjustment value.

5.24.2 Auto Balance SOC Adjustment value

The balance value (delta SOC) is the difference between the present charge in a cell and the desired charge for that cell.

The method for calculating the state of charge for a cell is left to the system designer. Typically, determining the state of charge is dependent on the chosen cell type and manufacturer, cell voltage, charge and discharge rates, temperature, age of the cell, number of cycles, and other factors. Tables for determining SOC are often available from the battery cell manufacturer.

The balance value itself is a function of the current SOC, required SOC, balancing leg impedance, and sample interval. This value is calculated by the host microcontroller for each cell. The balancing leg impedance is made up of the external balance FET and balancing resistor. The sample interval is equal to the balance cycle on time period (such as, each cell voltage is sampled at the end of the balance on time).

The balancing value B for each cell is calculated using the formula shown in Equation 1. See also “Balance Value Calculation Example” on page 113:

(EQ. 1) $$B = \frac{8191}{5} \times (CurrentSOC - TargetSOC) \times \frac{Z}{dt}$$

where:

B = the balance register value
CurrentSOC = the present SOC of the cell (Coulombs)
TargetSOC = the required SOC value (Coulombs)
Z = the balancing leg impedance (ohms)
dt = the sampling time interval (Balance cycle on time in seconds)
8191/5 = a voltage to Hex conversion value

The balancing leg impedance is normally the sum of the balance FET $r_{DS(ON)}$ and the balance resistor.

The balancing value (B) can also be defined as in the set of equations following. Auto balance is guided by Equations 2 and 3.

(EQ. 2) $$SOC = I \times t = \frac{V}{Z} \times t$$

(EQ. 3) $$B = SOC \times \frac{Z}{dt} = \frac{V}{Z} \times t \times \frac{Z}{dt} = \frac{V}{dt} \times t$$

where:

dt = Balance cycle on time
t = Total balance time

Equations 2 and 3 show that the impedance drops out of the equation, leaving only voltage and time elements. So, “B” becomes a collection of voltages that integrate during the balance cycle on time, and accumulate over the total balance time period, to equal the programmed delta capacity.

Twelve 28-bit registers are provided for the balance value for each cell. The balance values are programmed for all cells as needed using Balance Value registers 6’h20 to 6’h37. (See Table 24 for the contents of the Cell 1 and Cell 2 Balance Values Registers.

Table 24. Balance Values Register Cell 1 and Cell 2

ADDR	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6’20	Cell 1 Balance Value bits [13:0]													
6’21	Cell 1 Balance Value bits [27:14]													
6’22	Cell 2 Balance Value bits [13:0]													
6’23	Cell 2 Balance Value bits [27:14]													

At the end of each balance cycle on time interval the ISL78600 measures the voltage on each of the cells that were balanced during that interval. The measured values are then subtracted from the balance values for those cells. This process continues until the balance value for each cell is zero, at which time the auto balancing process is complete.

Auto Balance mode cannot operate while the ISL78600 is in Sleep mode. If the Sleep command is received while the device is auto balancing (and the watchdog timer is off) then balancing continues until it is finished, and then the device enters Sleep mode. If the watchdog timer is active during the Auto Balance mode and the device receives the Sleep command, then balancing stops immediately, the device enters Sleep mode immediately. The WDTM bit is set when the watchdog timer expires (see Table 22).

If the device was performing an auto balance operation prior to a Sleep Command, then receiving a Wake command resumes balancing with the same SOC calculations that were in place when the device entered Sleep Mode.

5.24.3 Balancing In Scan Continuous Mode

Cell balancing may be active while the ISL78600 is operating in Scan Continuous mode. This is especially important to maintain error detection while the host is busy with other tasks during a Timed or Auto Balance operation. In Scan Continuous mode the ISL78600 scans cell voltages, temperatures, and open-wire conditions at a rate determined by the Scan Interval bits in the Fault Setup register (see Table 16 on page 55). The behavior of the balancing functions while operating in Scan Continuous mode is controlled by the BDDS bit in the Device Setup register. If BDDS is set, then cell balancing is inhibited during cell voltage measurements and for 10ms before the cell voltage scan to allow the balance devices to turn off. Balancing is re-enabled automatically at the end of the scan. Scan Continuous and the BDDS function are available during both Timed and Auto Balance modes, but not during Manual Balance.

5.24.4 Monitoring Cell Balance

To facilitate the system monitoring of the cell balance operation, the ISL78600 has a Cells Balanced Enabled register that shows the present state of the balance drivers. A “1” indicates that the CBn output is enabled. A “0” indicates that the CBn output is disabled. This register is valid only in a Stand-Alone configuration. Reading this register in any other mode results in a NAK response.

Table 25. Cells Being Balanced Register

11	10	9	8	7	6	5	4	3	2	1	0
CBEN12	CBEN11	CBEN10	CBEN9	CBEN8	CBEN7	CBEN6	CBEN5	CBEN4	CBEN3	CBEN2	CBEN1

6. Daisy Chain Commands

Daisy chain devices require some special commands that are not needed by a stand-alone device. These commands are Identify, ACK, and NAK. Identify is needed to enumerate the devices in the stack. ACK is used as a command to check the communications hardware and to indicate proper communications status. A NAK response indicates that there was some problem with the addressed device recognizing the command.

6.1 Identify Command

Identify mode is a special case mode that must be executed before any other communications to daisy chained devices, except for the Sleep command and Wakeup command. The Identify command initiates address assignments to the devices in the daisy chain stack.

Devices determine their stack position while in Identify mode.

To start the address identification process, the host sends an Identify command with Device Address bits, Stack Address bits, and Comms Select bits all set to 0. See Figure 60.

When receiving such command, the device at the far end of the stack, a.k.a: top device, enters the Identify mode and responds with ACK, with the Device Address set to 0 because its address has not yet been determined. See Figure 61.

The other stack devices enter Identify mode when receiving the ACK response from the top device.

When in Identify mode, all stack devices except the Master initialize their Device Address register to 4'h0. The Master (identified by the state of the COMMS SELECT pins = 2'b01) sets its Device Address to 4'h1.

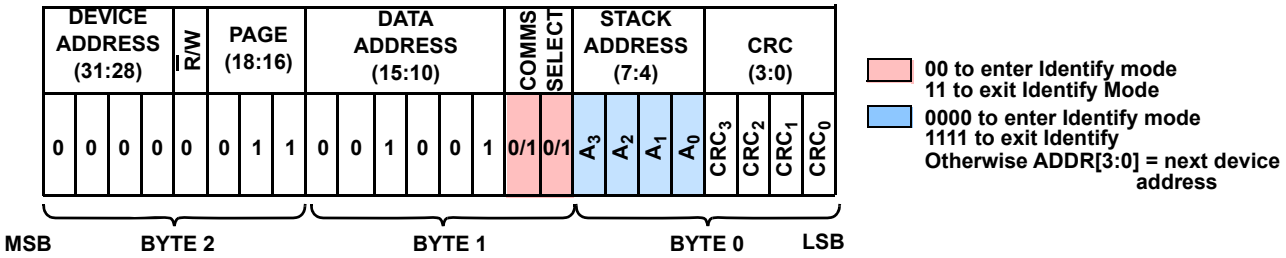


Figure 60. Identify Command

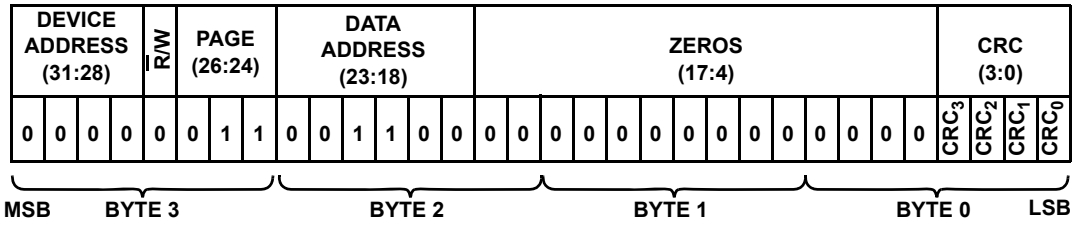


Figure 61. First Response to Identify Command (ACK)

After receiving the ACK response, the host microcontroller sends the Identify command with stack address bits set to 4'b0010 (i.e. 24'h0000 0011 0010 0100 **0010** 0110). The stack address is in blue. The last four bits are the corresponding CRC value. The Master passes the command onto the stack. The device at stack position 2 responds by setting its Comms Setup register device address bits (ADDR[3:0]) to 4'h2 and stack size bits (SIZE[3:0]) to 4'h2 and returns the Identify Response to the Master. The response includes the state of the device COMMS SELECT pins (2'b11 in red) and the stack address of the device (4'b0010) in blue (32'b0000 0011 0010 01**11** **0010** 0000 0000 1111). See Figure 62. Identified devices update their stack size information with each new transmission.

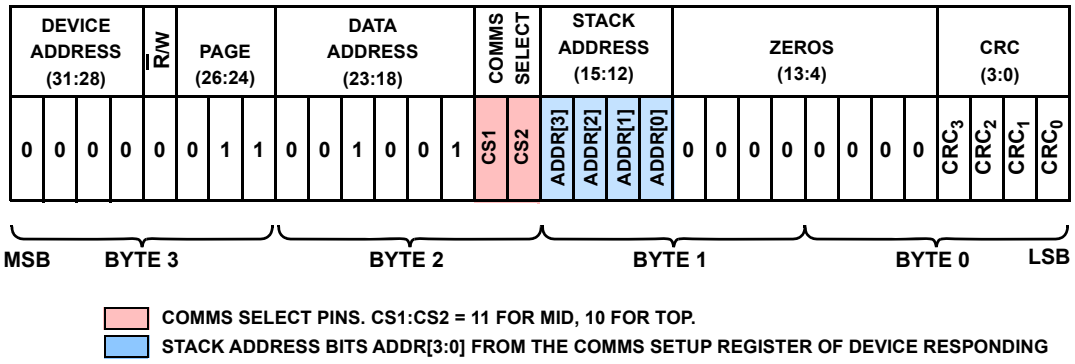


Figure 62. Identify Response From Mid/Top Device

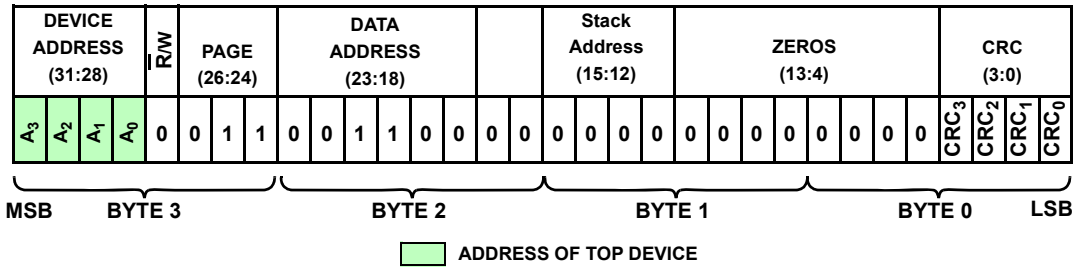


Figure 63. Response to Exit Identify Command

The host microcontroller then sends the Identify command with stack address 6'h3. Device 3 responds by setting its device address and stack size information and returning the Identify Response with COMMS SELECT pins of 2'b11 and an address 4'h3.

The process continues with the host microcontroller incrementing the stack address and sending Identify commands until the response indicates that it is from the Top device (as identified by the COMMS SELECT pins value of 2'b10). The Master then loads its device address and stack size information.

All devices in the stack have now been assigned their device address. The host microcontroller recognizes the top stack response and loads the total number of stack devices to local memory.

To complete the operation the host sends the Identify command with the Comms Select bits set to 2'b11 and the Stack Address bits set to 4'b1111. Devices exit Identify mode on receipt of this command. The stack Top device responds with ACK, Figure 63.

For an example of the full sequence when the stack has three devices, see Figure 64.

When in Normal mode, devices only recognize as valid the Identify command with Device Address bits, Stack Address bits, and Comms Select bits all set to 0. Any other Identify command variant causes a NAK response from the addressed device(s).

Send Identify Command	Tx	0000 0011 0010 0100 0000 0100	03 24 04
	Rx	0000 0011 0011 0000 0000 0000 0000 1100	03 30 00 0C (ACK FROM MASTER)
Send Identify Device 2	Tx	0000 0011 0010 0100 0010 0110	03 24 26
	Rx	0000 0011 0010 0111 0010 0000 0000 1111	03 27 20 0F
Send Identify Device 3	Tx	0000 0011 0010 0100 0011 0111	03 24 37
	Rx	0000 0011 0010 0110 0011 0000 0000 0101	03 26 30 05
Send Identify Complete	Tx	0000 0011 0010 0111 1111 1110	03 27 FE
	Rx	0011 0011 0011 0000 0000 0000 0000 0001	33 30 00 01 (ACK FROM TOP)

Figure 64. Identify Example - Stack of 3 Devices

6.1.1 Identify Timing

To determine the time required to complete an Identify operation, see Table 26. In the table are two SPI command columns showing the time required to send the Identify command and receive the response (with an SPI clock of 1MHz.) In the case of the Master, there are no daisy chain clocks, so all three bytes of the send and four bytes of the receive are accumulated. For the daisy chain devices, the daisy communication overlaps with two of the SPI send bytes and with three of the SPI receive bytes, so there is no extra time needed for these bits.

When the device receives the Identify command, it adds a delay time before sending the response back to the master. Then, on receiving the daisy response, the master sends the response to the host through the SPI port.

The “Time for Each Device” column shows the time for the Identify commands to be sent and propagate through each numbered device. The “Identify Total Time” column shows the total accumulated time required for Identify commands to be sent and propagate through all devices in the battery stack configuration. The “Identify + Identify Complete Time” column adds the identify complete timing to the total. The Identify Complete command takes the same number of clock cycles as the last Identify command.

Table 26. Identify Timing With Daisy Chain Operating at 500kHz

Number of Devices (2 Minimum)	SPI Command Send Time (µs)	Daisy Transmit Time (µs)	Response Delay (µs)	Daisy Receive Time (µs)	SPI Command Receive Time (µs)	Time for Each Device (µs)	Identify Total Time (µs)	Identify + Identify Complete Time (µs)
1 (Master)	24	0	0	0	32	56	56	56
2	8	50	18	66	8	150	206	356
3	8	52	18	68	8	154	360	514
4	8	54	18	70	8	158	518	676
5	8	56	18	72	8	162	680	842
6	8	58	18	74	8	166	846	1012
7	8	60	18	76	8	170	1016	1186
8	8	62	18	78	8	174	1190	1364
9	8	64	18	80	8	178	1368	1546
10	8	66	18	82	8	182	1550	1732
11	8	68	18	84	8	186	1736	1922

Table 26. Identify Timing With Daisy Chain Operating at 500kHz (Continued)

Number of Devices (2 Minimum)	SPI Command Send Time (µs)	Daisy Transmit Time (µs)	Response Delay (µs)	Daisy Receive Time (µs)	SPI Command Receive Time (µs)	Time for Each Device (µs)	Identify Total Time (µs)	Identify + Identify Complete Time (µs)
12	8	70	18	86	8	190	1926	2116
13	8	72	18	88	8	194	2120	2314
14	8	74	18	90	8	198	2318	2516

Table 27. Identify Timing With Daisy Chain Operating at 250kHz

Number of Devices (2 Minimum)	SPI Command Send Time (µs)	Daisy Transmit Time (µs)	Response Delay (µs)	Daisy Receive Time (µs)	SPI Command Receive Time (µs)	Time for Each Device (µs)	Identify Total Time (µs)	Identify + Identify Complete Time (µs)
1 (Master)	24	0	0	0	32	56	56	56
2	8	100	34	132	8	282	338	620
3	8	104	34	136	8	290	628	918
4	8	108	34	140	8	298	926	1224
5	8	112	34	144	8	306	1232	1538
6	8	116	34	148	8	314	1546	1860
7	8	120	34	152	8	322	1868	2190
8	8	124	34	156	8	330	2198	2528
9	8	128	34	160	8	338	2536	2874
10	8	132	34	164	8	346	2882	3228
11	8	136	34	168	8	354	3236	3590
12	8	140	34	172	8	362	3598	3960
13	8	144	34	176	8	370	3968	4338
14	8	148	34	180	8	378	4346	4724

6.2 ACK (Acknowledge) Command

Daisy chain devices use ACK to acknowledge receipt of a valid command. ACK is also useful as a communications test command: the stack Top device returns ACK in response to successful receipt of the ACK command. No other action is performed in response to an ACK.

6.3 NAK (Not Acknowledge) Command

The target device and top stack device return a NAK if they receive an unrecognized command. If a command addressed to all devices using the “Address All” address (1111) or the Identify stack address (0000) is not recognized by any devices then all devices not recognizing the command respond NAK. In this case, the host microcontroller receives the NAK response from the lowest stack device that failed to recognize the command. An incomplete command (such as one that is less than the length required) also causes a NAK to be returned.

7. Communications

All communications are conducted through the SPI port in single 8-bit byte increments. The MSB is transmitted first and the LSB is transmitted last.

Maximum operating data rates is 2Mbps for the SPI interface. When using the daisy chain communications system it is recommended that the synchronous communications data rate be at least twice that of the daisy chain system (see Table 8 on page 36).

In stand-alone applications (non-daisy chain) data is sent without additional address information. This maximizes the throughput for full duplex SPI operation.

In daisy chain applications all measurement data is sent with the corresponding Device Address (the position within the daisy chain), parameter identifier, and data address. Daisy chain communication throughput is maximized by allowing streamed data (accessed by a “read all data” address).

7.1 SPI Interface

The ISL78600 operates as an SPI slave capable of bus speeds up to 2Mbps. Four lines make up the SPI interface: SCLK, DIN, DOUT, and $\overline{CS}$. The SPI interface operates in either full duplex or half duplex mode depending on the daisy chain status of the part.

The DOUT line is normally tri-stated (high impedance) to allow use in a multidrop bus. DOUT is only active when $\overline{CS}$ is low.

An additional output $\overline{DATA\ READY}$ is used in the daisy chain configuration to notify the host microcontroller that responses have been received from a device in the chain.

7.1.1 Full Duplex (Stand-alone) SPI operation

In non-daisy chain applications, the SPI bus operates as a standard, full duplex, SPI port. Read and write commands are sent to the ISL78600 in 8-bit blocks. $\overline{CS}$ is taken high between each block.

Data flow is controlled by interpreting the first bit of each transaction and counting the requisite number of bytes. It is the responsibility of the host microcontroller to ensure that commands are correctly formulated, as an incorrect formulation, (such as, read bit instead of write bit), would cause the port to lose synchronization.

There is a timeout period associated with the $\overline{CS}$ inactive (high) condition, which resets all the communications counters. This effectively resets the SPI port to a known starting condition. If $\overline{CS}$ stays high for more than 100µs, then the SPI state machine resets.

A pending device response from a previous command is sent by the ISL78600 during the first 2 bytes of the 3-byte Write transaction. The third byte from the ISL78600 is then discarded by the host microcontroller. This maintains sequencing during 3-byte (Write) transactions.

Interface timing for full duplex SPI transfers are shown in Figure 3 on page 19.

7.1.2 Half Duplex (DAISY CHAIN) Operation

The SPI operates in half duplex mode when configured as a daisy chain application (see Table 7 on page 35). Data flow is controlled by a handshake system using the $\overline{DATA\ READY}$ and $\overline{CS}$ signals. $\overline{DATA\ READY}$ is controlled by the ISL78600. $\overline{CS}$ is controlled by the host microcontroller. This handshake accommodates the delay between command receipt and device response due to the latency of the daisy chain communications system.

A timeout period associated with the $\overline{CS}$ inactive (high) condition resets all the communications counters. This effectively resets the SPI port to a known starting condition. If $\overline{CS}$ stays high for more than 100µs, then the SPI state machine resets.

Responses from stack devices are received by the stack Master (stack bottom device). The stack Master then asserts its $\overline{DATA\ READY}$ output when the first full data byte is available. The host microcontroller responds by asserting $\overline{CS}$ and clocking the data out of the DOUT port. The $\overline{DATA\ READY}$ line is then cleared and DOUT is tri-stated in response to CS being taken high. In this mode the DIN and DOUT lines can be connected externally.

Half duplex communications are conducted using the $\overline{\text{DATA READY}}$/$\overline{\text{CS}}$ handshake as follows:

1. The host microcontroller sends a command to the ISL78600 using the $\overline{\text{CS}}$ line to select the ISL78600 and clocking data into the ISL78600 DIN pin.
2. The ISL78600 asserts $\overline{\text{DATA READY}}$ low when it is ready to send data to the host microcontroller. When $\overline{\text{DATA READY}}$ is low, the ISL78600 is in transmit mode and ignores any data on DIN.
3. The host microcontroller asserts $\overline{\text{CS}}$ low and clocks 8 bits of data out of DOUT using SCLK.
4. The host microcontroller then raises $\overline{\text{CS}}$. The ISL78600 responds by raising $\overline{\text{DATA READY}}$ and tri-stating DOUT.
5. The ISL78600 reasserts $\overline{\text{DATA READY}}$ for the next byte, and so on.

The host microcontroller must service the ISL78600 if $\overline{\text{DATA READY}}$ is low before sending further commands. The ISL78600 ignores any data sent to DIN while $\overline{\text{DATA READY}}$ is low.

The $\overline{\text{DATA READY}}$ output from the ISL78600 is not asserted if $\overline{\text{CS}}$ is already asserted. The microcontroller can interrupt a sequential data transfer by asserting $\overline{\text{CS}}$ before the ISL78600 asserts $\overline{\text{DATA READY}}$. This causes a conflict with the communications and is not recommended. A conflict created in this manner would be recognized by the microcontroller either not receiving the expected response or receiving a communications failure notification.

Interface timing for half duplex SPI transfers are shown in Figure 4 on page 19.

7.2 Non-Daisy Chain Communications

In non-daisy chain (stand-alone) systems, all communications sent from the master are 2 or 3 bytes in length. Data read, action, and scan commands are 2 bytes. Data writes are 3 bytes. Device responses are 2 bytes in length and contain data only.

Write commands in non-daisy chain systems are composed of a $\overline{\text{read}}$/write bit, page address (3 bits), data address (6 bits), and data (14 bits) - Three bytes.

Read commands in non-daisy chain systems are composed of a $\overline{\text{read}}$/write bit, page address (3 bits), data address (6 bits), fill (6 bits), and 16 bits of returned data (ignore the first most significant bits of data returned) - Four bytes.

The ISL78600 responds to read commands by loading the requested data to its output buffer. The output buffer contents are then loaded to the shift register when $\overline{\text{CS}}$ goes low and are shifted out on the DOUT line on the falling edges of SCLK. This sequence continues until all the requested data has been sent.

Commands and data are memory mapped to 14-bit data locations. The memory map is arranged in pages. Pages 1 and 2 are used for volatile data. Page 3 contains the scan, action, and communications administration commands. Page 4 accesses nonvolatile memory. Page 5 is used for factory test.

All commands, except register writes, are treated as reads.

Non-daisy chain devices do not generate a response to write or system level commands. Data integrity can be verified by reading register contents after writing. The ISL78600 does nothing in response to a write or administration command that is not recognized. An unrecognized read command returns 16'h0000. An incomplete command, such as may occur if communications are interrupted, is registered as an unrecognized command either when $\overline{\text{CS}}$ is taken high or after a timeout period. The communications interface is reset after the timeout period.

Non-daisy chain communications are conducted without CRC (Cyclical Redundancy Check) error detection. The following commands have no meaning in non-daisy chain systems: Identify, ACK, NAK.

The rules for non-daisy chain installations are shown in Table 28.

Examples of full duplex SPI read and write sequences are shown in Figure 70 through 72 on page 76.

7.2.1 Examples of Non-Daisy Communications

An example Device Read (Cell 7), with response, is shown in Figure 72 on page 76.

Examples of the various command structures for non-daisy chain installations are shown in Figures 65 through 69.

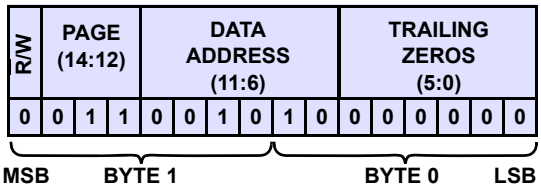


Figure 65. SLEEP Command

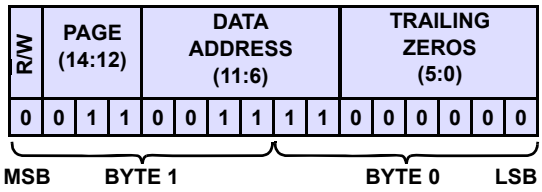


Figure 66. WAKEUP Command

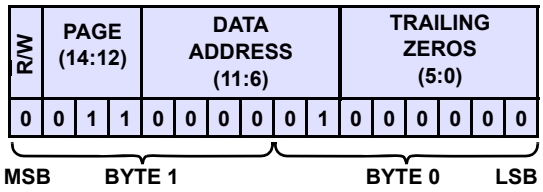


Figure 67. SCAN VOLTAGES Command

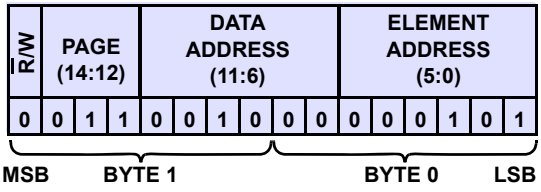


Figure 68. MEASURE Command: Cell 5 Voltage

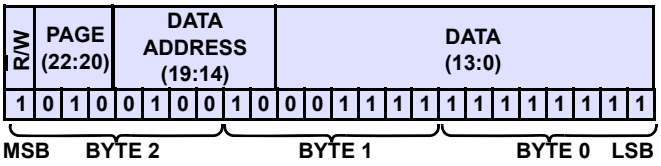


Figure 69. WRITE Command: External Temperature Limit = 14'h0FFF

Table 28. ISL78600 Data Interpretation Rules for Non-Daisy Installations

First Bit in Sequence	Page Address	Data Address	Interpretation
0	011	001000	Measure command. Last six bits of transmission contain element address.
0	Any	All other	Device scan, read, or action command. Last six bits of transmission are zero.
1	Any	Any	Device write command.

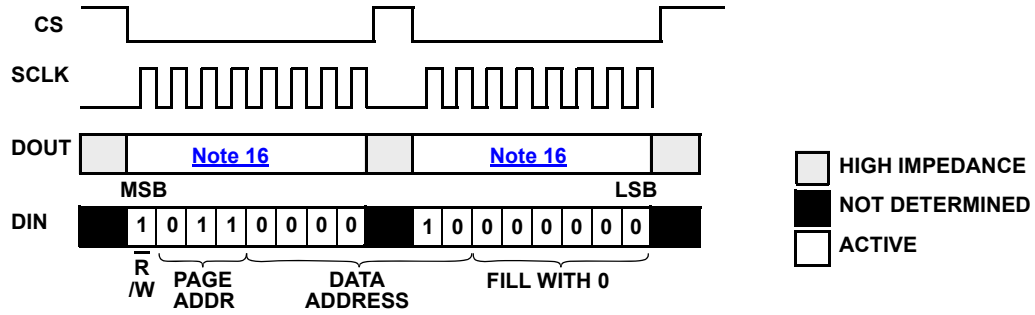
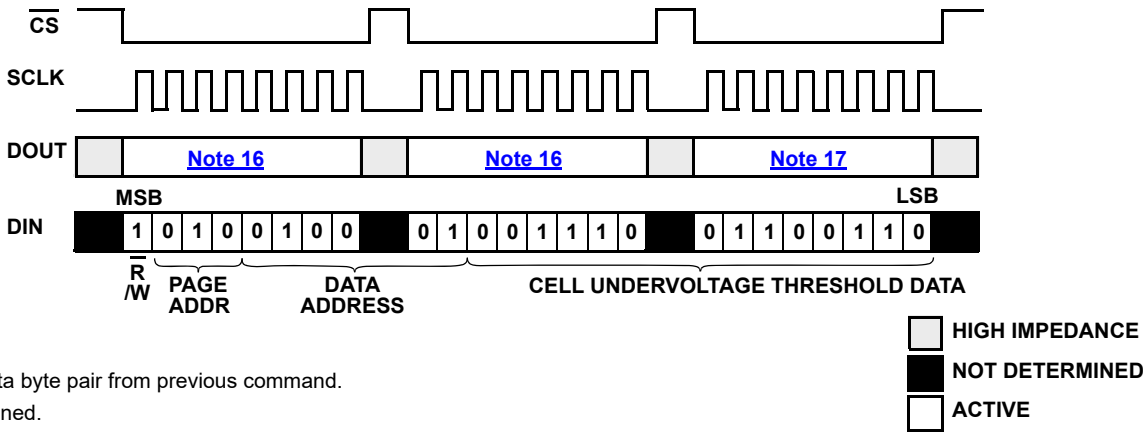
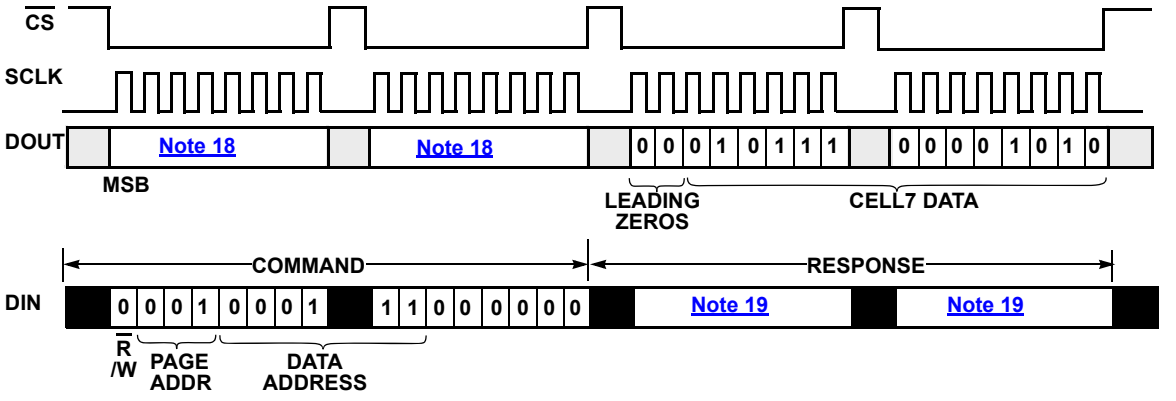


Figure 70. SPI Full Duplex (Stand-Alone) Command Example: MEASURE ExT4 Voltage



Notes:
16. Last data byte pair from previous command.
17. Not defined.

Figure 71. SPI Full Duplex (Stand-Alone) Command Example: WRITE Undervoltage Threshold Data



Notes:
18. Last data byte pair from previous command.
19. Next command (or 8'h00 if no command).
20. Host should start to clock data out within 30µs of $\overline{CS}$ going low.

Figure 72. SPI Full Duplex (Stand-Alone) Command Example: READ Cell 7 Data

7.3 Daisy Chain Communications

Commands in daisy chain systems are transmitted and received through the SPI port and are composed of a device address (4 bits), a $\overline{read}$/write bit, page address (3 bits), data address (6 bits), data (6 bits), and CRC (4 bits).

Device commands and data are memory mapped to 14-bit data locations. The memory map is arranged in pages. Pages 1 and 2 are used for volatile data. Page 3 contains the scan, action, and communications administration commands. Page 4 accesses nonvolatile memory. Page 5 is used for factory test.

The daisy chain communication is intended for use with large stacks of battery cells where a number of ISL78600 devices are used.

7.4 Communications Protocol

All daisy chain communications are passed from device to device such that all devices in the stack receive the same information. Each device then decodes the message and responds as needed. The originating device (master in the case of commands, addressed device or Top stack device in the case of responses) generates the system clock and data stream. Each device delays the data stream by one clock cycle. Each device knows its stack location (see the Identify command on page 69) and the total number of devices in the stack. Each originating device adds a number of clock pulses to the daisy chain data stream to allow transmission through the stack.

All communications from the host microcontroller are passed from device to device to the last device in the chain (Top device). The Top device responds to read and write messages with an “ACK” (or with the requested data if this is the addressed device and the message was a read command). The addressed device then waits to receive the “ACK” before responding, either with data in the case of a read, or with an “ACK” in the case of a write or other action command (like the Balance Enable command). Scan commands, such as Scan Voltages, do not respond.

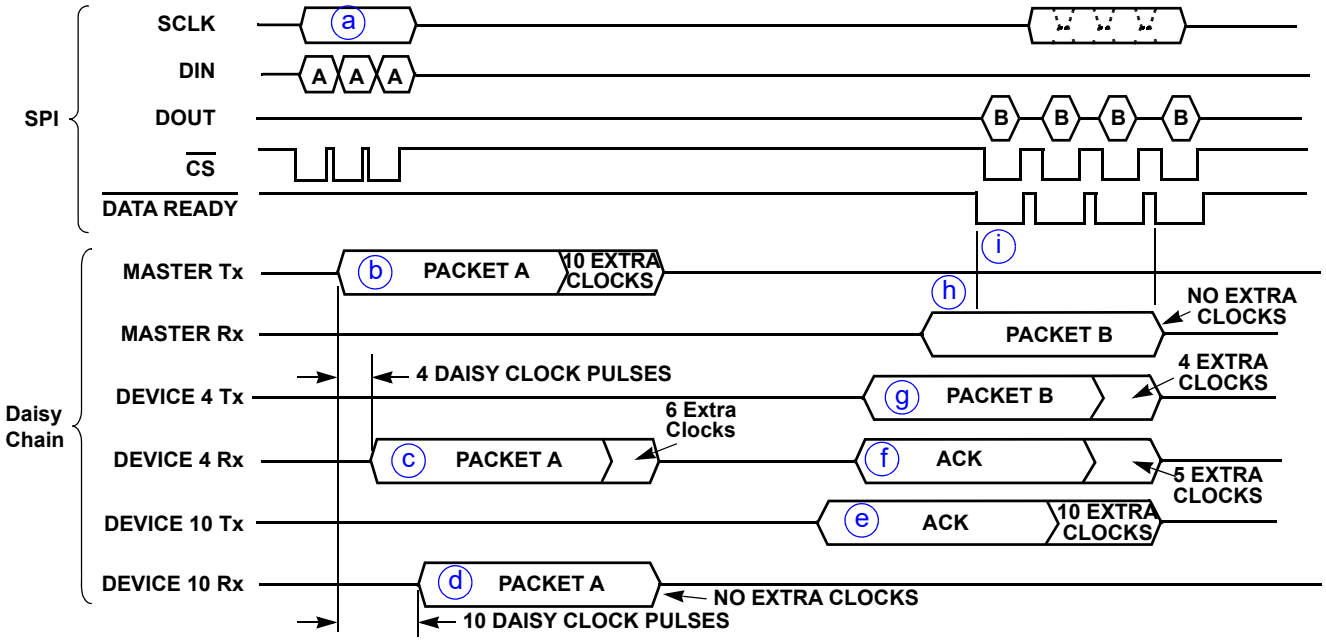
A read, write, or action command communications transmission is only considered to be complete following receipt of a valid response from the target device or a Communications Failure response (see “Communications Failure” on page 103). The host microcontroller should not transmit additional commands until either response has been received from the target stack device.

Figure 73 on page 78 shows a typical communication sequence to “Read Device 4, Cell 7” data from a stack of 10 devices. The typical response time from the rising edge of $\overline{CS}$ at the end of the first byte of a read/write/action command, sent by the host microcontroller, to the assertion of $\overline{DATA\ READY}$ by the master device, indicating that the response is ready, is given in Table 29 for various daisy chain data rates. This is an indication how long the host has between a command and the response, however, when implementing a communications time out, the timing for Communications Failure response should be used.

Table 29. Typical Response Times for Daisy Chain Commands with Response

Response Time (for Commands with Response) Number of Devices	Typical Daisy Chain Data Rate (kHz)				Units
	500	250	125	62.5	
3	172	336	664	1320	µs
4	176	344	680	1352	µs
5	180	352	696	1384	µs
6	184	360	712	1416	µs
7	188	368	728	1448	µs
8	192	376	744	1480	µs
9	196	384	760	1512	µs
10	200	392	776	1544	µs
11	204	400	792	1576	µs
12	208	408	808	1608	µs
13	212	416	824	1640	µs
14	216	424	840	1672	µs

Note: This table presents the time from the rising edge of CS at the end of the first byte of a read/write/action command, sent by the host microcontroller, to the assertion of $\overline{DATA\ READY}$ signal by the master device.



a. The Host microcontroller sends “Read device 4, Cell 7” = Packet A

b. The Master begins relaying Packet A following receipt of the first byte of A. Master adds an extra byte, plus 10 clock cycles to allow all stack devices to relay the message.

c. Device 4 receives and decodes “Read device 4, Cell 7” and waits for a response from top stack device.

d. Top of stack (Device 10) receives and decodes Packet A.

e. Device 10 responds “ACK”. Device 10 adds 10 clock cycles to allow all stack devices to relay the message.

f. Device 4 receives and decodes an ACK.

g. Device 4 transmits the Cell 7 data = Packet B. Device 4 subtracts one clock cycle to synchronize timing for lower stack devices to relay the message.

h. The Master asserts $\overline{DATA\ READY}$ after receiving the first byte of Packet B.

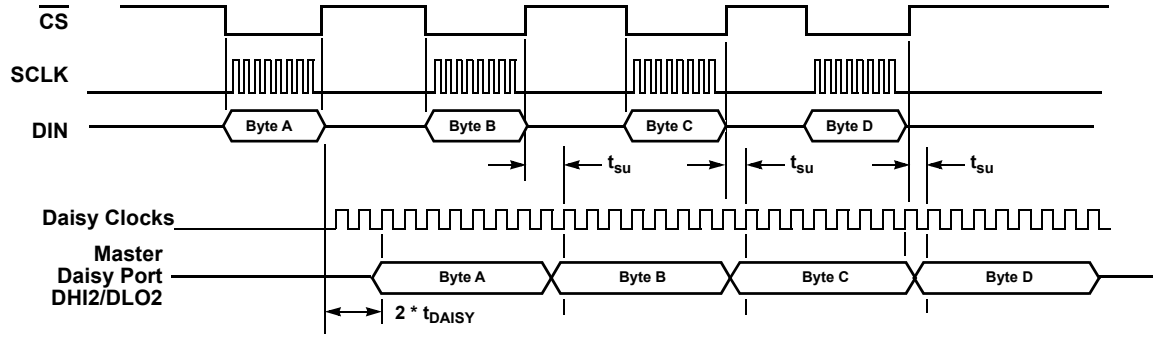
i. The Host responds by asserting $\overline{CS}$ and clocking out eight bits of data from DOUT. $\overline{CS}$ is taken high following the 8th bit. The master responds by taking $\overline{DATA\ READY}$ high and tri-stating DOUT. Master asserts $\overline{DATA\ READY}$ after receiving the next byte and so on.

Figure 73. Daisy Chain Read example “READ Device 4, Cell 7”. Stack of 10 Devices

7.4.1 Daisy Chain Transmit Buffer

A 4-byte data buffer is provided between the SPI and Daisy Chain communications. A command sent on the SPI port is passed to the Daisy Chain, starting two Daisy Chain clock cycles after the rising edge of $\overline{CS}$ (at the end of the first byte of the command). The Daisy Chain then clocks data out of the transmit buffer.

IMPORTANT: The host microcontroller must continue to feed the buffer with command bytes before all bytes have been clocked out on the Daisy Chain. If the Host MCU cannot keep the buffer full with proper command bytes, the Daisy Chain sends bad data to the devices on the Daisy Chain. This results in the Daisy Chain device receiving a command with a bad CRC and that device responds with a NAK.



Note: A command byte needs to be clocked into the SPI port at least one Daisy Chain clock prior to the first Daisy clock placing that byte on the DHI2/DLO2 port. (t_{su} > 1*t_{DAISY})

Figure 74. Command Timing to Avoid Daisy Buffer Underflow

7.4.2 Daisy Chain Receive Buffer

A 4-byte data buffer is provided between the Daisy Chain and SPI communications. This accommodates all single transaction responses. Multiple byte responses, such as Identify, Read All Voltages, Read All Temperatures, Read All Faults, and responses that may include a fault response from a device detecting an error, would overflow this buffer. It is important therefore that the host microcontroller completes a read of the first byte of data before a fifth byte arrives on the Master device's daisy chain port and to clock data out from the SPI port faster than data is clocked in through the Daisy port so as not to risk losing data.

For example, when performing the first step in an IDENTIFY operation (see "Identify Command" on page 69) the daisy chain top device returns a 4-byte response plus 14 extra zeros (because it does not yet know how many devices are in the stack.) If the Host does not read the first byte from the Master before the 32nd daisy clock, the extra zeros overwrite the first byte of the response. In another example, a Read All Faults returns 22 bytes. It is important for the Host to read data from the ISL78600 faster than 4 bytes every 31.5 Daisy clocks. (see Figure 75 on page 79).

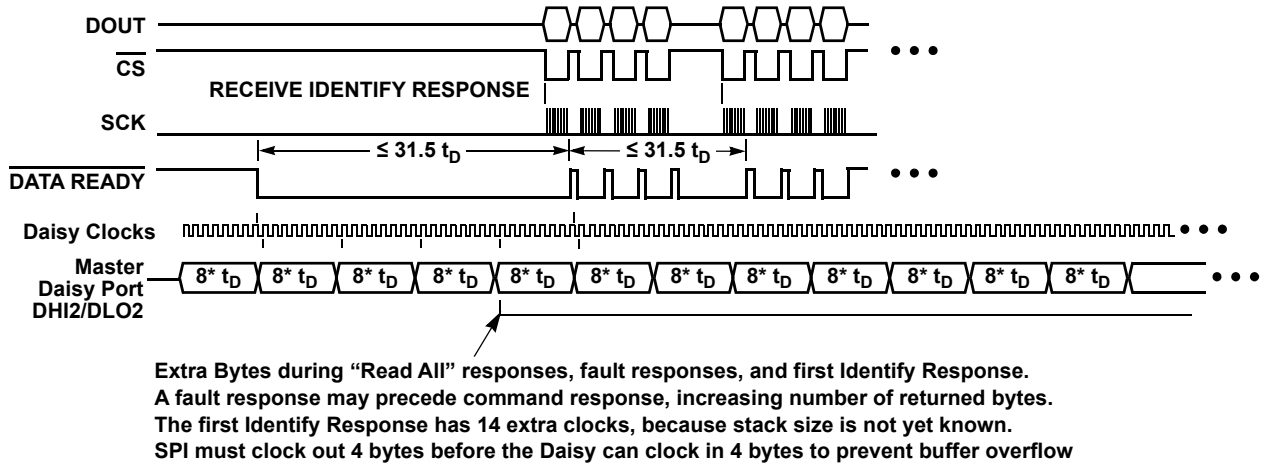


Figure 75. Example Worst Case Timing to Avoid Daisy Buffer Overflow

7.4.3 Communication Sequences

All daisy chain device responses are 4-byte sequences, except for the responses to the Read All command. All responses start with the Device Address and use a 4-bit CRC. The response to the “Read All Commands” is to send a normal 4-byte data response for the first data segment and continue sending the remaining data segments in 3-byte sections composed of data address, data, and CRC. This creates an anomaly with the normal CRC usage in that the first four bytes have a 4-bit CRC at the end (operating on 3.5 bytes of data) while the remaining bytes have a CRC, which only operates on 2.5 bytes. The host microcontroller, having requested the data, must be prepared for this.

Daisy chain devices require Device Address information to be added to the basic command set. Daisy chain writes are 4-byte sequences. Daisy chain reads are three bytes. All commands, except register write operations, are treated as reads. Daisy chain communications employ a 4-bit CRC (Cyclic Redundancy Check) using a polynomial of the form $1 + X + X^4$. The first four bits of each daisy chain transmission contain the Device Address, which can be any number from 0001 to 1110. All devices respond to the “Address All” (1111) and Identify (0000) Device Addresses. The fifth bit is set to ‘1’ for write and ‘0’ for read. The rules for daisy chain installations are shown in Table 30.

Table 30. ISL78600 Data Interpretation Rules for Daisy Chain Installations

First Four Bits in Sequence	Fifth Bit ($\overline{R/W}$)	Page	Data Address	Interpretation
Device Address [3:0] (Nonzero)	0	011	001000	Measure command. Data address is followed by 6-bit element address.
0000	0	011	001001	Identify command. Data address is followed by device count data.
Device Address [3:0] (Nonzero)	0	Any	All other	Device Read command. Data address is followed by 6 zeros.
Device Address [3:0] (Nonzero)	1	Any	Any	Device Write command.

7.4.4 CRC Calculation

Daisy chain communications employ a 4-bit CRC using a polynomial of the form $1 + X + X^4$. The polynomial is implemented as a 4-stage internal XOR standard linear feedback shift register as shown in Figure 76. The CRC value is calculated using the base command data only. The CRC value is not included in the calculation.

The host microcontroller calculates the CRC when sending commands or writing data. The calculation is repeated in the ISL78600 and checked for compliance. The ISL78600 calculates the CRC when responding with data (device reads). The host microcontroller then repeats the calculation and checks for compliance.

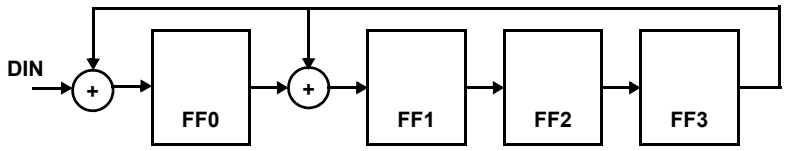


Figure 76. 4-Bit CRC Calculation

```
Attribute VB_Name = "isl78600evb_crc4_lib"
' File - isl78600evb_crc4_lib.bas
' Copyright (c) 2010 Intersil
' ------------------------------------------------------------------------------
Option Explicit
'*****************************************************************
' CRC4 Routines
'*****************************************************************
 Public Function CheckCRC4(myArray() As Byte) As Boolean
    'returns True if CRC4 checksum (low nibble of last byte in myarray)
    'is good. Array can be any length

    Dim crc4 As Byte
    Dim lastnibble As Byte

    lastnibble = myArray(UBound(myArray)) And &HF
    crc4 = CalculateCRC4(myArray)

    If lastnibble = crc4 Then
       CheckCRC4 = True
    Else
       CheckCRC4 = False
    End If

End Function

Public Sub AddCRC4(myArray() As Byte)
    'adds CRC4 checksum (low nibble in last byte in array)
    'array can be any length

    Dim crc4 As Byte

    crc4 = CalculateCRC4(myArray)
    myArray(UBound(myArray)) = (myArray(UBound(myArray)) And &HF0) Or
crc4

End Sub

Public Function CalculateCRC4(ByRef myArray() As Byte) As Byte
    'calculates/returns the CRC4 checksum of array contents excluding
    'last low nibble. Array can be any length

    Dim size As Integer
    Dim i As Integer
    Dim j As Integer
    Dim k As Integer
    Dim bit0 As Boolean, bit1 As Boolean, bit2 As Boolean, bit3 As Boolean
    Dim ff0 As Boolean, ff1 As Boolean, ff2 As Boolean, ff3 As Boolean
    Dim carry As Boolean
    Dim arraycopy() As Byte
    Dim result As Byte

    'copy data so we do not clobber source array
    ReDim arraycopy(LBound(myArray) To UBound(myArray)) As Byte
    For i = LBound(myArray) To UBound(myArray)
       arraycopy(i) = myArray(i)
    Next

    'initialize bits
    bit0 = False
    bit1 = False
    bit2 = False
    bit3 = False

    'simple implementation of CRC4 (using polynomial 1 + X + X^4)
    For i = LBound(arraycopy) To UBound(arraycopy)

       'last nibble is ignored for CRC4 calculations
       If i = UBound(arraycopy) Then
          k = 4
       Else
          k = 8
       End If

       For j = 1 To k
          'shift left one bit
          carry = (arraycopy(i) And &H80) > 0
          arraycopy(i) = (arraycopy(i) And &H7F) * 2

          'see ISL78600 datasheet, Fig 11: 4-bit CRC calculation
          ff0 = carry Xor bit3
          ff1 = bit0 Xor bit3
          ff2 = bit1
          ff3 = bit2
          bit0 = ff0
          bit1 = ff1
          bit2 = ff2
          bit3 = ff3
       Next j
    Next i

    'combine bits to obtain CRC4 result
    result = 0
    If bit0 Then
       result = result + 1
    End If
    If bit1 Then
       result = result + 2
    End If
    If bit2 Then
       result = result + 4
    End If
    If bit3 Then
       result = result + 8
    End If

    CalculateCRC4 = result

End Function
```

Figure 77. Example CRC Calculation Routine (Visual BASIC)

7.5 Daisy Chain Commands/Responses

When used in a daisy chain system each individual device dynamically assigns itself a unique address (see “Identify Command” on page 69). In addition, all daisy chain devices respond to a common address allowing them to be controlled simultaneously. For example, when using the Scan Voltages and Balance Enable commands (see “Communication Timing” on page 84).

Examples of the various read and write command structures for daisy chain installations are shown in Figures 79 through 84. The MSB is transmitted first and the LSB is transmitted last.

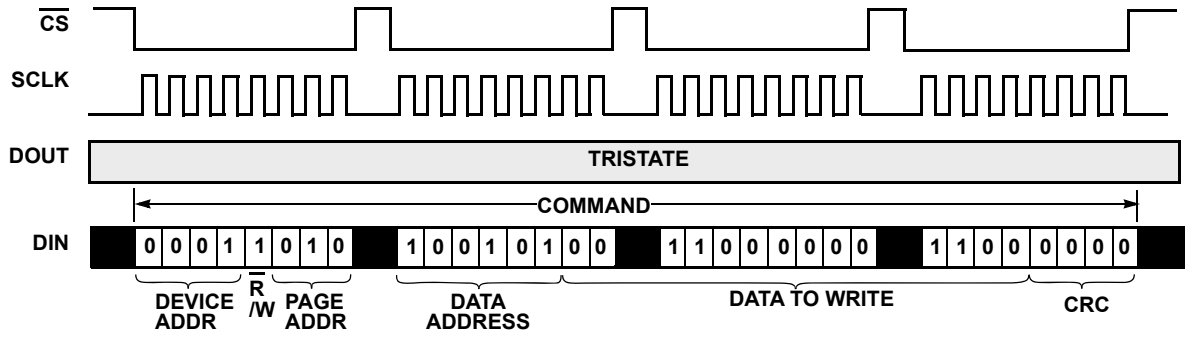


Figure 78. SPI Half Duplex (Daisy Chain) Example: WRITE Device 1, Device Setup Register

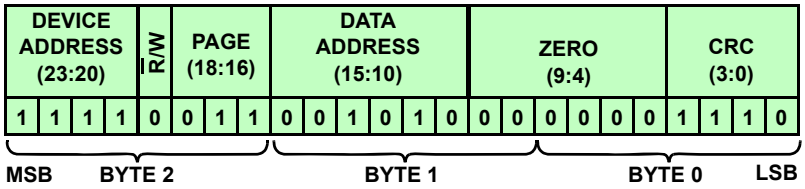


Figure 79. Daisy SLEEP Command

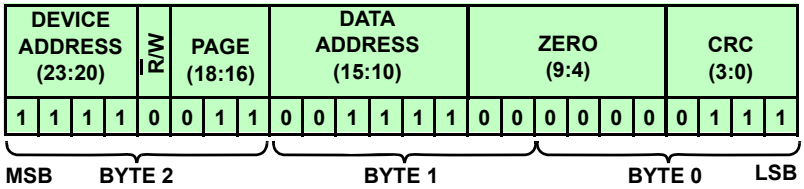


Figure 80. Daisy WAKEUP Command

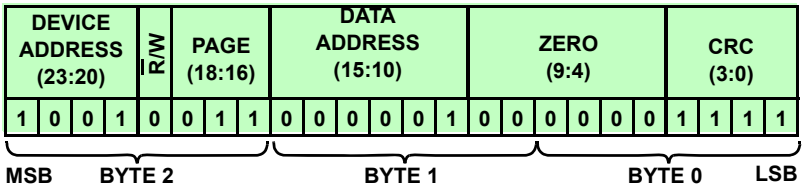


Figure 81. Daisy SCAN VOLTAGES Command: Device 9,

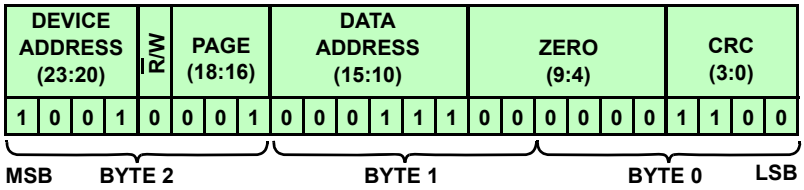


Figure 82. Daisy READ Command: Device 9, Cell 7 Register

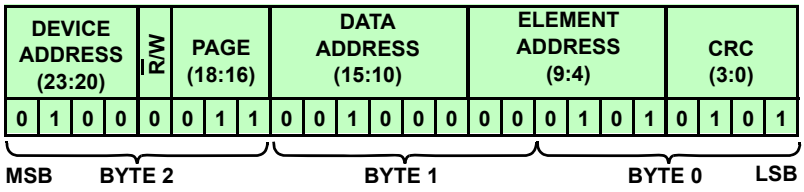


Figure 83. Daisy MEASURE Command: Device 4, Cell 5 Voltage

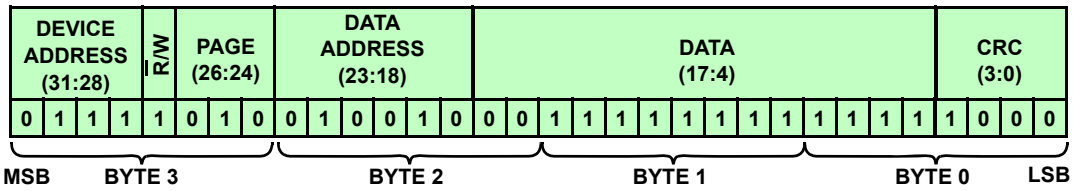


Figure 84. Daisy WRITE Command: Device 7, External Temperature Limit Value = 14'h0FFF

Response examples are shown in Figures 85 through 88.

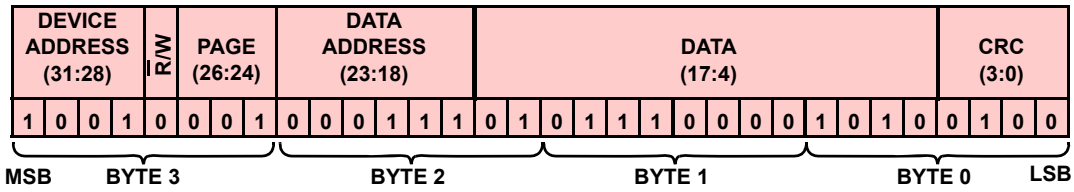


Figure 85. Daisy RESPONSE: Device 9, Cell 7 Voltage = 14'h170A (3.6V)

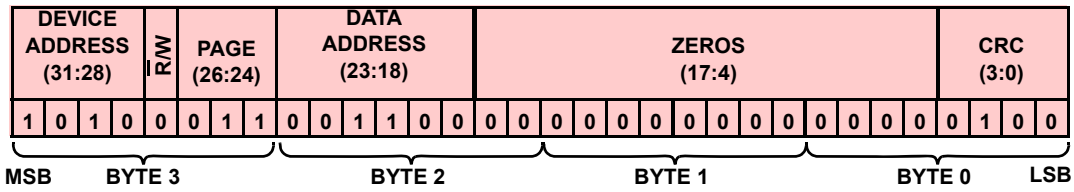


Figure 86. Daisy RESPONSE: Device 10, ACK

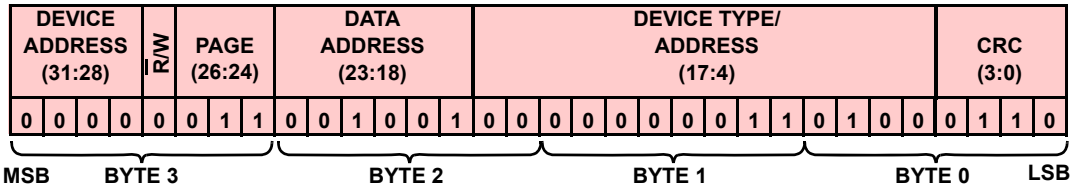


Figure 87. Daisy RESPONSE: Device 4, IDENTIFY (Middle Stack Device)

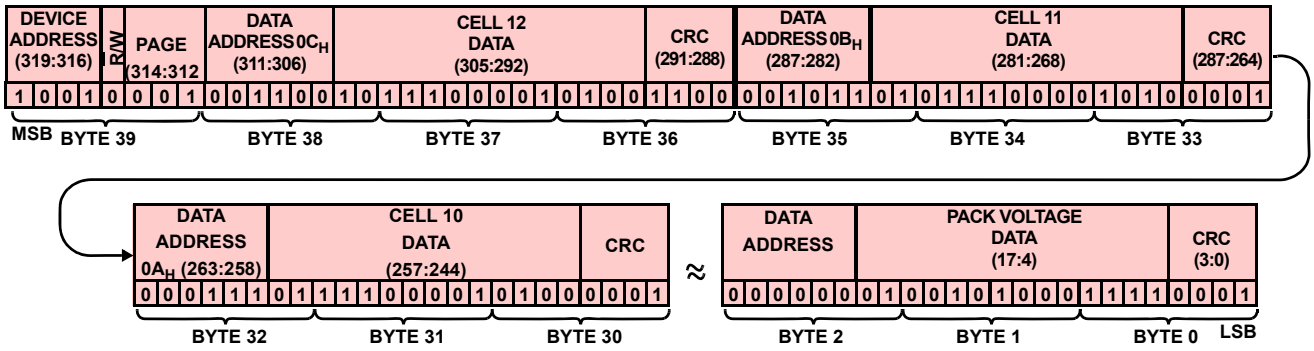


Figure 88. Daisy RESPONSE: Device 9, READ All Cell Voltage Data

7.6 Communication Timing

Collecting voltage and temperature data from daisy chained ISL78600 devices consists of three separate types of operations: A command to initiate measurement, the Measurement itself, and a command and response to retrieve data.

Commands are the same for all types of operations, but the timing is dependent on the number of devices in the stack, the daisy chain clock rate, and the SPI clock rate.

Actual measurement operations occur within the device and start with the last bit of the command byte and end with data being placed in a register. Measurement times are dependent on the ISL78600 internal clock. This clock has the same variations (and is related to) as the daisy chain clock.

Responses have different timing calculations, based on the position of the addressed device in the daisy chain stack and the daisy chain and SPI clock rates.

7.7 Measurement Timing Diagrams

All measurement timing is derived from the ISL78600's internal oscillators. The figures shown in the following as typical are those obtained with the oscillators operating at their nominal frequencies and with any synchronization timing also at nominal value. Maximum figures are those obtained with the oscillators operating at their minimum frequencies and with the maximum time for any synchronization timing.

Measurement timing begins with a Start Scan signal. This signal is generated internally by the ISL78600 at the last clock falling edge of the Scan or Measure command. (This is the last falling edge of the SPI clock in the case of a stand-alone or master device, or the last falling edge of the daisy chain clock, in the case of a daisy chain device). Daisy chain middle or top devices impose additional synchronization delays. Communications sent on the SPI port are passed on to the master device's daisy chain port at the end of the first byte of data. Then, for each device, there is an additional delay of one daisy chain clock cycle.

On receiving the Start Scan signal, the device initializes measurement circuits and proceeds to perform the requested measurement(s). When the measurements are made, some devices perform additional operations, such as checking for overvoltage conditions. The measurement command ends when registers are updated. At this time the registers can be read using a separate command. A detailed timing breakdown is provided for each measurement type as follows.

See Figure 89 for the measurement timing for a stand-alone device.

See Figure 90 for the measurement timing for daisy chain devices.

Table 34 on page 93 through Table 39 on page 95 give the typical and maximum timing for the critical elements of the device internal measurement process. Each table shows the timing from the last edge of the Scan command clock to the completion of the internal register update.

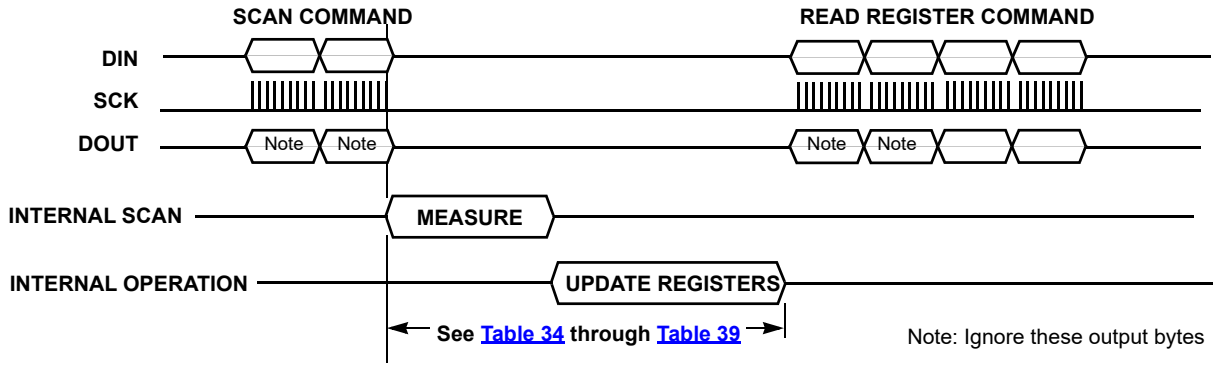


Figure 89. Scan/Measure Command Timing With Response (Stand-Alone)

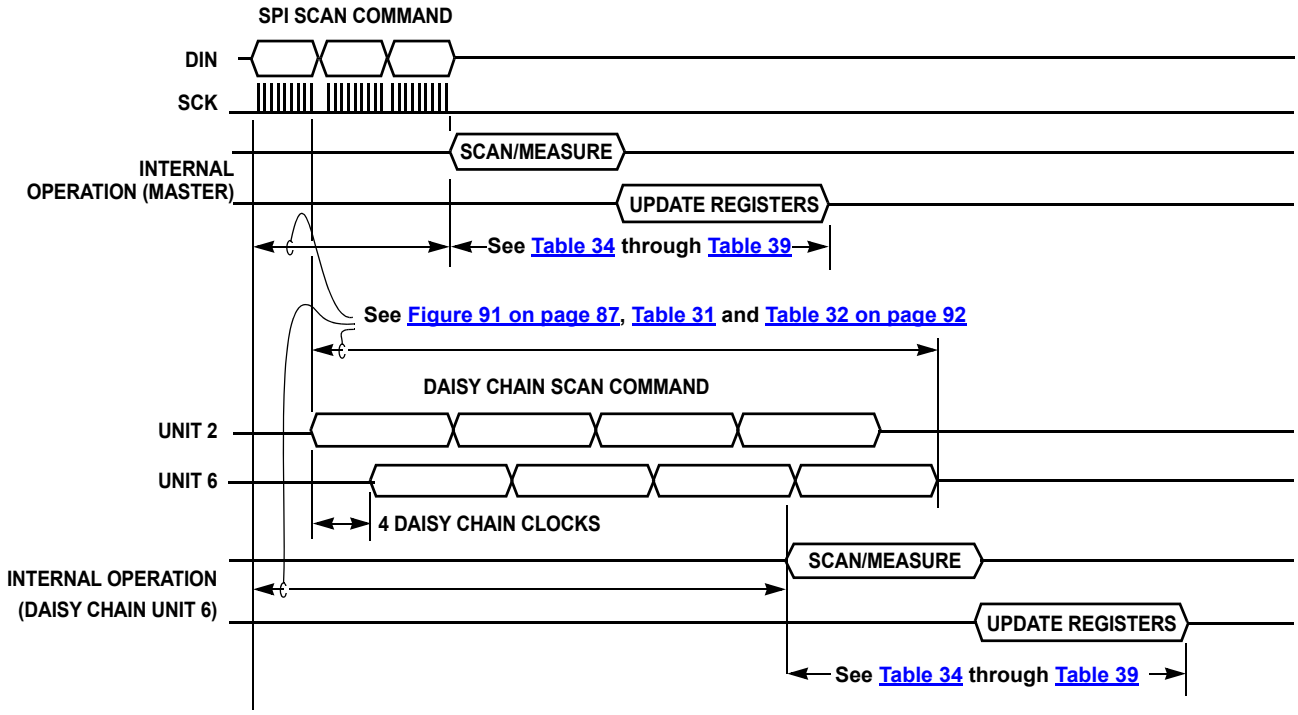
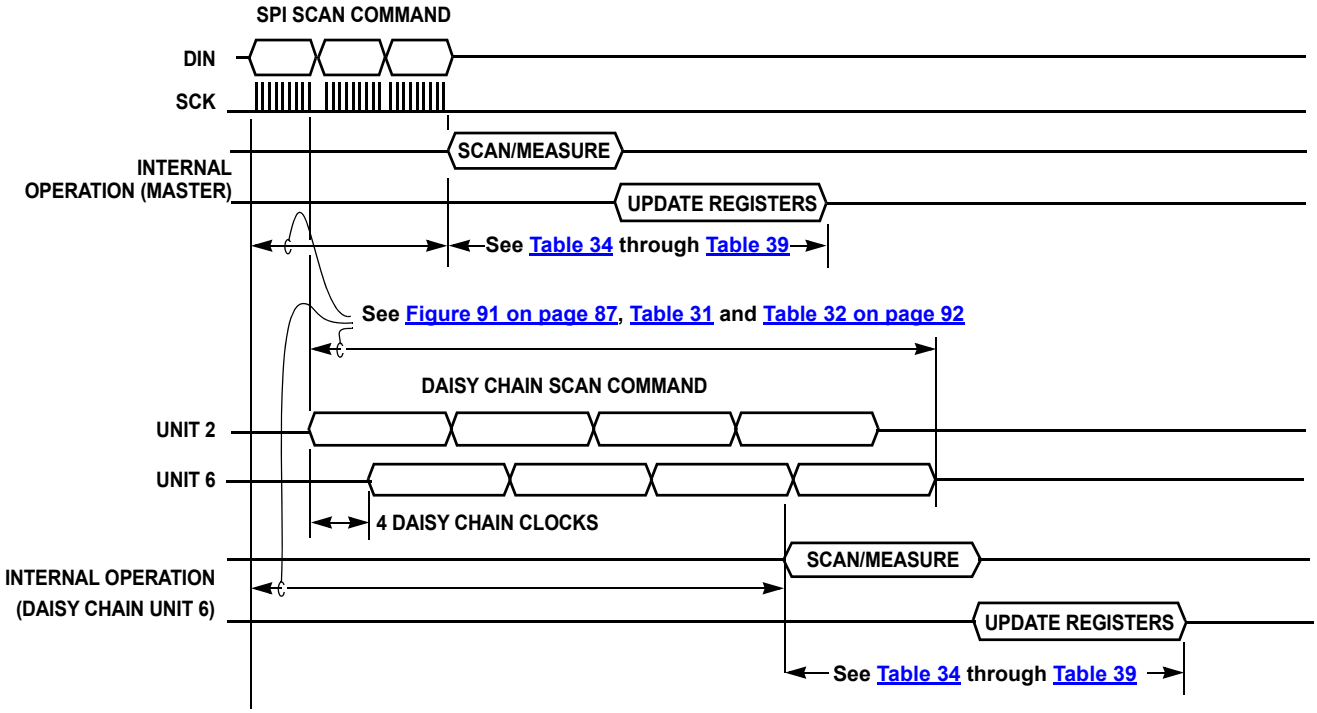
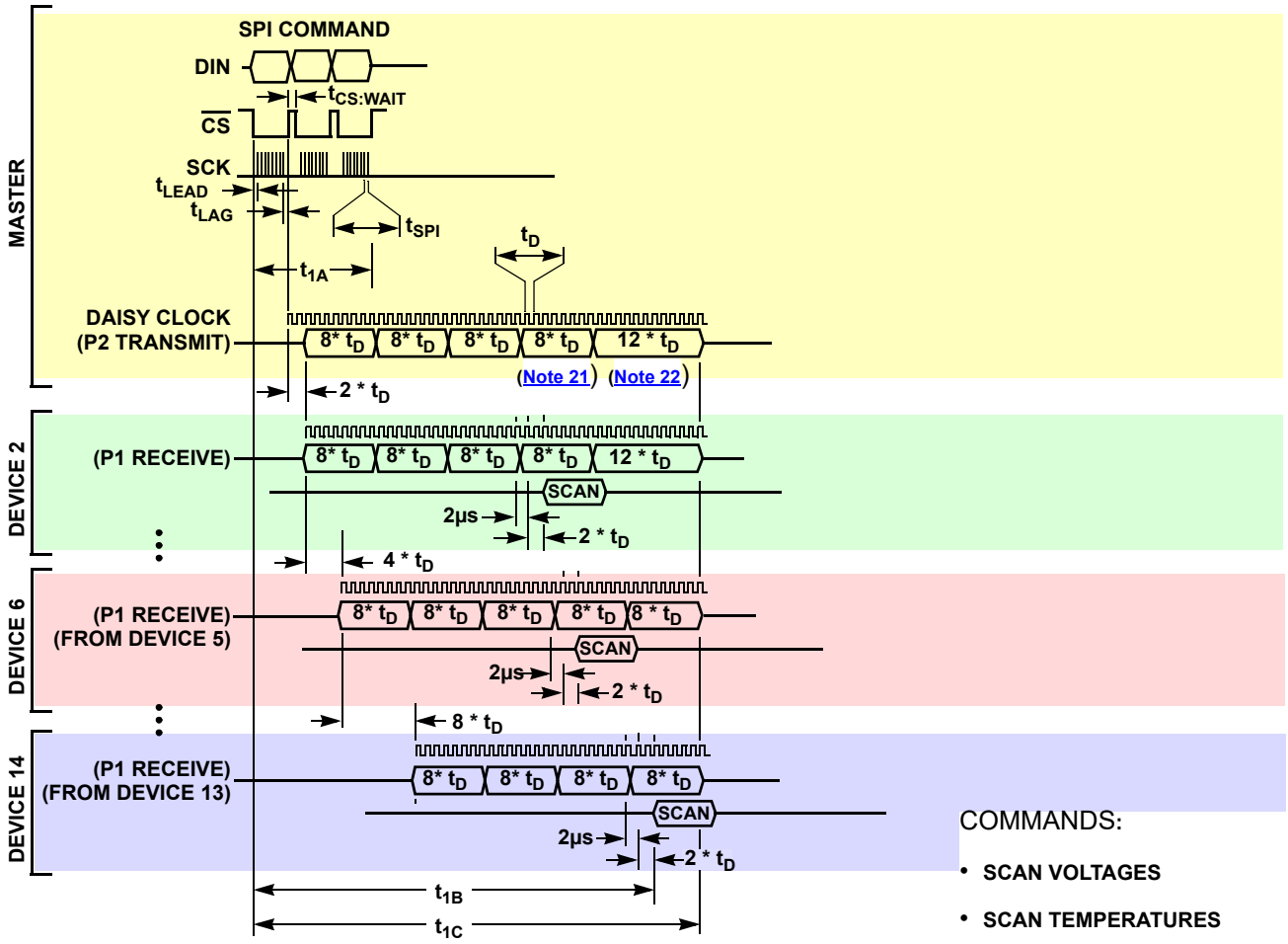


Figure 90. Scan/Measure Timing (6 Device Daisy Chain)



Scan/Measure Timing (6 Device Daisy Chain)

7.8 Command Timing Diagram



COMMANDS:

- SCAN VOLTAGES
- SCAN TEMPERATURES
- SCAN MIXED
- SCAN WIRES
- SCAN ALL
- MEASURE
- READ
- WRITE
- SCAN CONTINUOUS
- SCAN INHIBIT
- SLEEP
- NAK
- ACK
- BALANCE INHIBIT
- CALC CHECKSUM
- CHECK CHECKSUM

To Start of Scan (Master)

$$t_{1A} = (t_{SPI} \times 8 + t_{LEAD} + t_{LAG}) \times 3 + 2 \times t_{CSWAIT}$$

To Start of Scan (Top/Middle)

$$t_{1B} = t_{SPI} \times 8 + t_{LEAD} + t_{LAG} + t_D \times (28 + n - 2) + 2\mu s$$

To End of Command

$$t_{1C} = t_{SPI} \times 8 + t_{LEAD} + t_{LAG} + t_D \times (34 + N - 2)$$

where:

t_{SPI} = SPI clock period
t_D = Daisy chain clock period
$t_{CS:WAIT}$ = $\overline{CS}$ High time
t_{LEAD} = $\overline{CS}$ Low to first SPI Clock
t_{LAG} = Last SPI Clock $\overline{CS}$ High
n = Stack position of target device

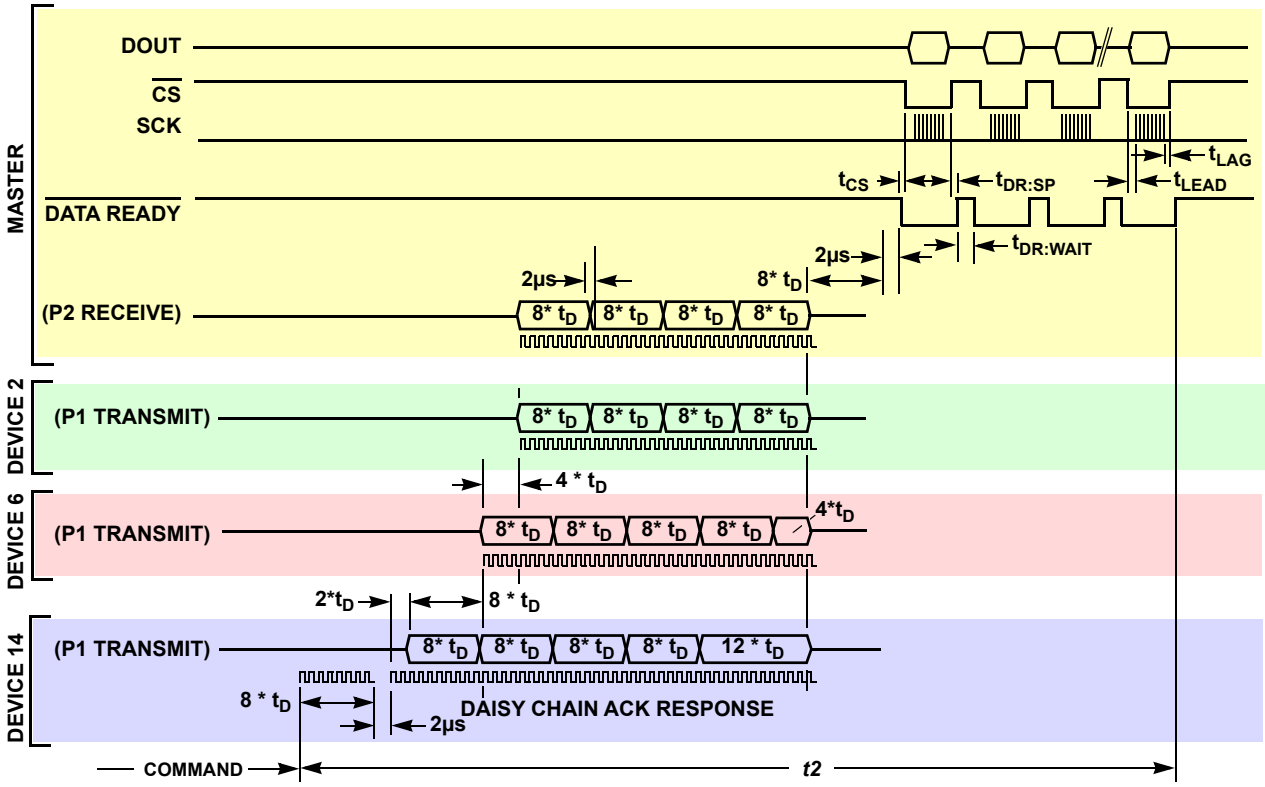
Notes:

21. Master adds extra byte of zeros as part of daisy protocol
22. Master adds N-2 clocks to allow communication to the end of the chain.

Figure 91. Command Timing

7.9 Response Timing Diagrams

Responses are different for Master, Middle, and Top devices. The response timings are shown in Figures 92, 92, and 93. **(Continued)**



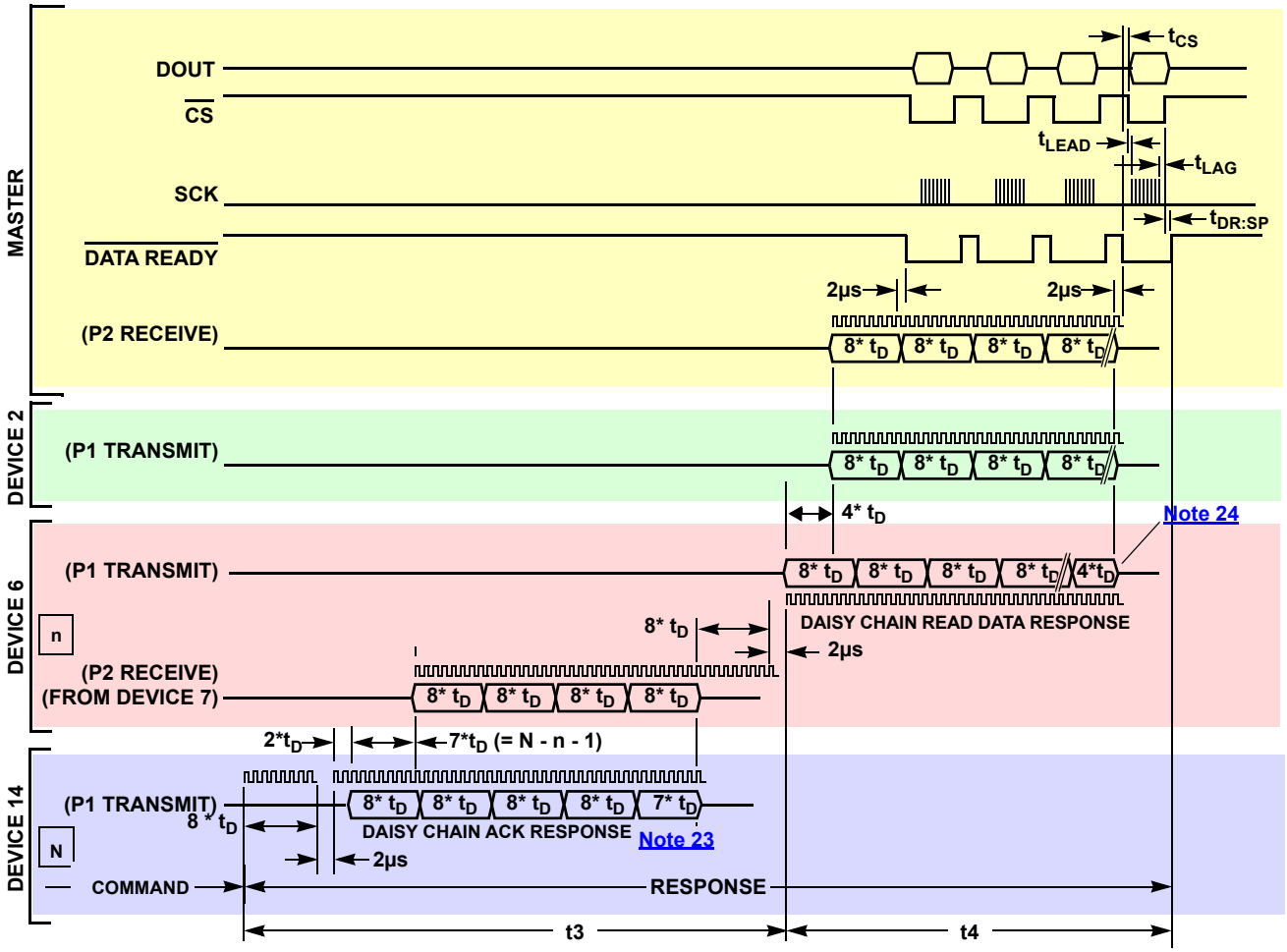
$$t2 = (8 \times t_{SPI} + t_{DRSP} + t_{DRWAIT} + t_{CS} + t_{LEAD} + t_{LAG}) \times D - t_{DRSP} + t_D \times (50 + N - 2) + 4\mu s$$

where:

t_{SPI} = SPI clock period
t_D = Daisy chain clock period
t_{CS} = Host delay from $\overline{\text{DATA READY}}$ Low to the $\overline{\text{CS}}$ Low
t_{DRSP} = $\overline{\text{CS}}$ High to $\overline{\text{DATA READY}}$ High
t_{DRWAIT} = $\overline{\text{DATA READY}}$ High time
t_{LEAD} = $\overline{\text{CS}}$ Low to first SPI Clock
t_{LAG} = Last SPI Clock $\overline{\text{CS}}$ High
N = Stack position of TOP device
D = Number of data bytes

D = 4 for one register read (or ACK/NAK/Identify Response)
D = 40 for read all voltages
D = 22 for read all temperatures
D = 22 for read all faults
D = 43 for read all setup

Figure 92. Response Timing (Master Device)



$$t3 = t_D \times (50 + N - n - 1) + 4\mu s$$

$$t4 = t_{SPI} \times 8 + t_{CS} + t_{LEAD} + t_{LAG} + t_{DRSP} + t_D \times (D \times 8 + n - 2) + 2\mu s$$

where:

t_D = Daisy Chain clock period

t_{SPI} = SPI Clock Period

N = Stack position of TOP device

n = Stack position of middle stack device

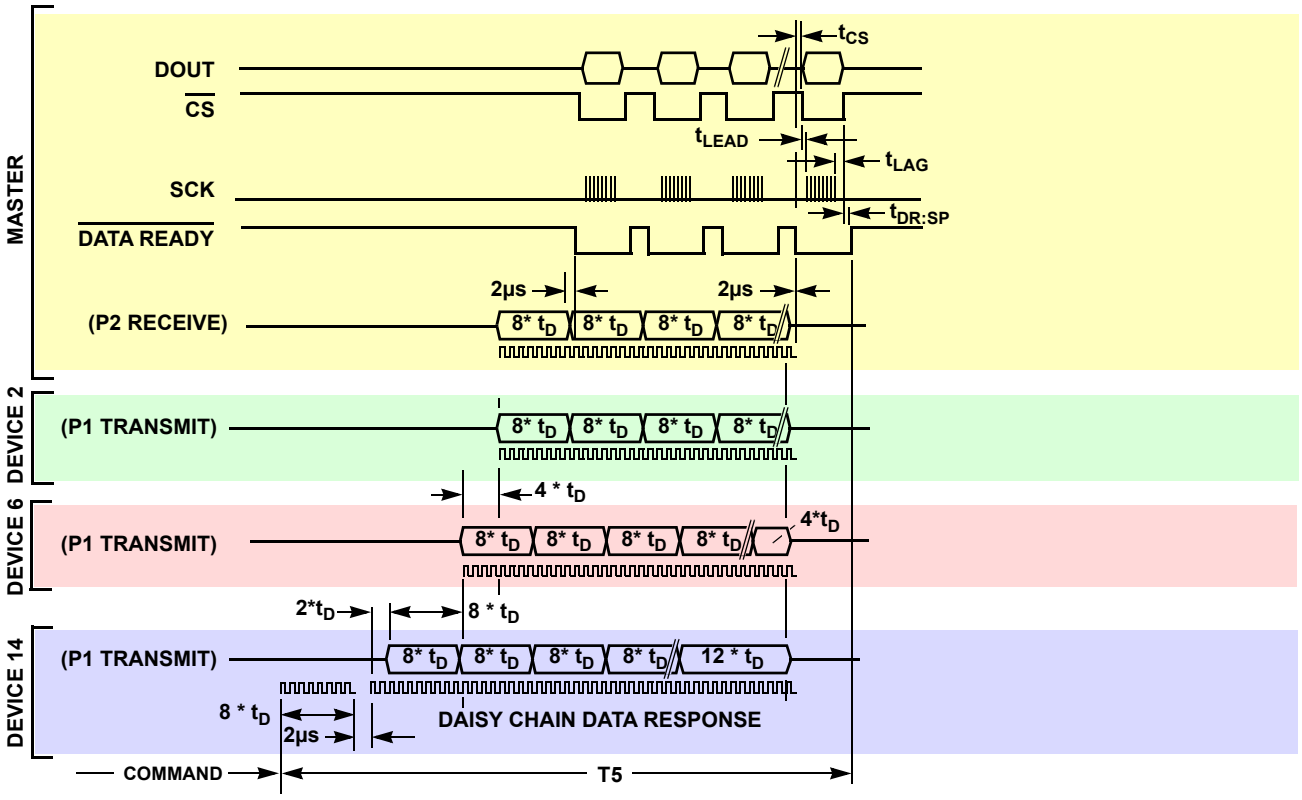
t_{CS} = Delay imposed by host from $\overline{\text{DATA READY}}$ to the $\overline{\text{CS}}$ Low.

D = Number of bytes in the Middle stack device response e.g. read all cell data = 40 bytes, Register or *ACK* response = 4 bytes.

Notes:

23. Top device adds (N - n - 1) Daisy clocks to allow communications to the targeted middle stack device.
24. Middle stack device adds (n - 2) Daisy clocks to allow communications to the master device.

Figure 93. Response Timing (Middle Stack Device)



$$t5 = t_{SPI} \times 8 + t_{LEAD} + t_{LAG} + t_{DRSP} + t_{CS} + t_D \times (D \times 8 + 10 + N - 2) + 4\mu s$$

where:

t_{SPI} = SPI clock period
t_D = Daisy chain clock period
t_{CS} = Host delay from $\overline{\text{DATA READY}}$ to the $\overline{\text{CS}}$ Low.
t_{DRSP} = $\overline{\text{CS}}$ High to $\overline{\text{DATA READY}}$ High
t_{LEAD} = $\overline{\text{CS}}$ Low to first SPI Clock
t_{LAG} = Last SPI Clock $\overline{\text{CS}}$ High
N = stack position of TOP device
D = Number of bytes in response

Figure 94. Response Timing (Top Device)

8. System Timing Tables

8.1 Command Timing Tables

The command timing Table 31 includes the time from the start of the command to the start of an internal operation for each device in a stack. Table 32 shows the time required for the command to complete. For a stand-alone device the two values are the same, because the internal operation starts at the end of the command. For a daisy chain operation, the internal operation begins before the end of the command.

When calculating overall timing for a command, start with the time from start of the command to the start of the internal operation for the Target device. Add to this the time for the internal operation, see "Measurement Timing Tables" on page 93. Add to this the time it takes to read back the data. See "Response Timing Tables" on page 96. Also needed is a wait time between sending each command (see Table 33 on page 92).

When using the Address All option, the command timing for the Top device in the stack determines when the command ends, but use the Time to Start of Scan for each device to determine when that device begins its internal operation. For example, in a stack of six devices, it takes 90.9µs for the command to complete, but internal operations start at 13.8µs for the Master, 68.7µs for Device 2, 70.9µs for Device 3, etc.

In Tables 31 and 32, the calculation assumes a daisy chain (and internal) clock that is 10% slower than the nominal and an SPI clock that is running at the nominal speed (because the SPI clock is normally crystal controlled.) For the 500kHz daisy setting, timing assumes a 450kHz clock.

Table 31. Time to Start of Internal Operation

Time to Start of Internal Operation for Target Device	SPI Clock = 2MHz		Units
	Daisy Clock = 500kHz	Daisy Clock = 250kHz	
1	17.5	17.5	µs
2	68.7	130.9	µs
3	70.9	135.4	µs
4	73.2	139.8	µs
5	75.4	144.3	µs
6	77.6	148.7	µs
7	79.8	153.2	µs
8	82.1	157.6	µs
9	84.3	162.1	µs
10	86.5	166.5	µs
11	88.7	170.9	µs
12	90.9	175.4	µs
13	93.2	179.8	µs
14	95.4	184.3	µs

Table 32. Time to End of Command

Time to End of Command for Number of Devices	SPI Clock = 2MHz		Units
	Daisy Clock = 500kHz	Daisy Clock = 250kHz	
1	17.5	17.5	µs
2	82.0	157.6	µs
3	84.2	162.0	µs
4	86.5	166.5	µs
5	88.7	170.9	µs
6	90.9	175.3	µs
7	93.1	179.8	µs
8	95.3	184.2	µs
9	97.6	188.7	µs
10	99.8	193.1	µs
11	102.0	197.6	µs
12	104.2	202.0	µs
13	106.5	206.5	µs
14	108.7	210.9	µs

8.1.1 Sequential Daisy Chain communications

When sending a sequence of commands to the master device, the host must allow time, after each response and before sending the next command, for the daisy chain ports of all stack devices (other than the master) to switch to receive mode. This wait time is equal to eight daisy chain clock cycles and is imposed from the time of the last edge on the Master's input daisy chain port to the last edge of the first byte of the subsequent command on the SPI (see Figure 95). The minimum recommended wait time, between the host receiving a response and sending the next command, is given in Equation 4. For definition of terms, see Figure 94. Also, see Table 33.

$$t_{WAIT} = t_{CLR} - 2 \times ((8 \times t_{SPI}) + t_{LEAD} + t_{LAG}) + t_{DRSP} + t_{CS} \quad \text{(EQ. 4)}$$

Table 33. Minimum Recommended Communications Wait Time

	Daisy Chain Data Rate (kHz)				
	500	250	125	62.5	UNITS
Maximum Time for Daisy Chain Ports to Clear. See Figure 95.	18	36	72	144	µs

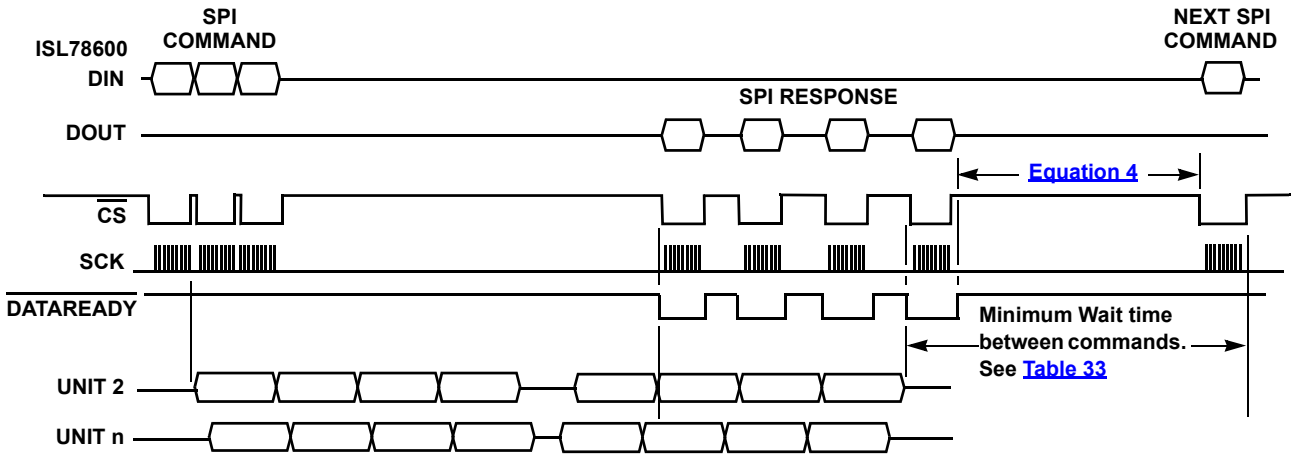


Figure 95. Minimum Wait Time Between Commands (Daisy Chain Response - TOP Device)

8.2 Measurement Timing Tables

8.2.1 Scan Voltages

The Scan Voltages command initiates a sequence of measurements starting with a scan of each cell input from Cell 12 to Cell 1, followed by a measurement of pack voltage. Additional measurements are then performed for the internal temperature and to check the connection integrity test of the VSS and VBAT inputs. The process completes with the application of calibration parameters and the loading of registers. Table 34 shows the times after the start of scan that the cell voltage inputs are sampled. The voltages are held until the ADC completes its conversion.

Table 34. Scan Voltages Function Timing - Daisy Chain Master or Stand-Alone Device

EVENT	Elapsed Time (µs)	
	TYP	MAX
Sample Cell 12	17	19
Sample Cell 11	38	42
Sample Cell 10	59	65
Sample Cell 9	81	89
Sample Cell 8	102	112
Sample Cell 7	123	135
Sample Cell 6	144	159
Sample Cell 5	166	182
Sample Cell 4	187	206
Sample Cell 3	208	229
Sample Cell 2	229	252
Sample Cell 1	251	276
Complete Cell Voltage Capture (ADC complete) Sample V_{BAT}	304	334
Complete V_{BAT} Voltage Capture	318	349
Measure Internal Temperature	423	465
Complete VSS Test	550	605
Complete V_{BAT} Test	726	799
Load Registers	766	842

8.2.2 Scan Temperatures

The Scan Temperatures command turns on the TEMPREG output and, after a 2.5ms settling interval, samples the ExT1 to ExT4 inputs. TEMPREG turns off on completion of the ExT4 measurement. The Reference Voltage, IC Temperature, and Multiplexer loopback function are also measured. The sequence is completed with respective registers being loaded.

Table 35. Scan Temperatures Function Timing – Daisy Chain Master or Stand-Alone Device

Event	Elapsed Time (µs)	
	Typical	Maximum
Turn On TEMPREG	2	2
Sample ExT1	2518	2770
~		
Sample ExT4	2564	2820
Sample Reference	2584	2842
Measure Internal Temperature	2689	2958
Load Registers	2689	2958

8.2.3 Scan Mixed

The Scan Mixed command performs all the functions of the Scan Voltages command but interposes a measurement of the ExT1 input between the Cell 7 and Cell 6 measurements.

Table 36. Scan Mixed Function Timing – Daisy Chain Master or Stand-Alone Device

Event	Elapsed Time (µs)	
	Typical	Maximum
Sample Cell 12	17	19
Sample Cell 11	38	42
Sample Cell 10	59	65
Sample Cell 9	80	88
Sample Cell 8	101	111
Sample Cell 7	122	134
Complete Cell Voltage Capture, Cells 12-7 and Sample Ext1	176	194
Complete Ext1 Capture	192	211
Sample Cell 6	207	228
Sample Cell 5	228	251
Sample Cell 4	249	274
Sample Cell 3	270	297
Sample Cell 2	291	321
Sample Cell 1	312	344
Complete Cell Voltage Capture Cells 6-1 ad Sample V_{BAT}	367	404
Complete V_{BAT} Voltage Capture	381	419
Load Registers	829	911

8.2.4 Scan Wires

The Scan Wires command initiates a sequence in which each input is loaded in turn with a test current for a duration of 4.5ms (default). At the end of this time the input voltage is checked and the test current is turned off. The result of each test is recorded and the Open-Wire Fault and Fault Status registers are updated (data latched) at the conclusion of the tests.

Table 37. Scan Wires Function Timing – Daisy Chain Master or Stand-Alone Device

Event	Elapsed Time (ms)	
	Typical	Maximum
Turn On VC0 Current	0.03	0.05
Test VC0	4.5	5.0
Turn On VC1 Current	4.6	5.1
Test VC1	9.1	10.0
~		
Turn On VC12 Current	54.9	60.3
Test VC12	59.4	65.3
Load Registers	59.4	65.3

8.2.5 Scan All

The Scan All command combines the Scan Voltages, Scan Wires, and Scan Temperatures commands into a single scan function.

Table 38. Scan All Function Timing – Daisy Chain Master or Stand-Alone Device

Event	Elapsed Time (ms)	
	Typical	Maximum
Start Scan Voltages	0	0
Start Scan Wires	0.8	0.9
Start Scan Temperatures	60.1	66.2
Complete sequence	62.8	69.1

8.2.6 Measure Command

Single parameter measurements of the cell voltages, Pack Voltage, ExT1 to ExT4 inputs, IC temperature, and Reference voltage are performed using the Measure command.

Table 39. Various Measure Function Timings – Daisy Chain Master or Stand-Alone Device

Event	Elapsed Time (µs)	
	Typical	Maximum
Measure Cell Voltage	178	196
Measure Pack Voltage	122	134
Measure ExT Input	2517	2768
Measure IC Temperature	106	116
Measure Reference Voltage	106	116

8.3 Response Timing Tables

Response Timing depends on the number of devices in the Stack, the position of the device in the stack, and how many bytes are read back. The following are the four types of responses:

- Single register read or ACK/NAK responses, where four bytes are returned by the Read Command
- Read All Voltage response, which returns 40 bytes
- Read all Temps or Read All Faults responses, which returns 22 bytes
- Read All Setup Registers response, which returns 43 bytes

In the following tables, the Master, Middle, and Top device response times for any number of daisy chain devices are included with the command timing for that configuration. The right hand column shows the total time to complete the read operation. This is calculated in Equation 5:

$$(N \times T_{COMMAND}) + ((N-2) \times T_{MID}) + T_{TOP} + T_{MASTER} \quad \text{(EQ. 5)}$$

where N = Number of devices in the stack.

In Tables 40 through 45, internal and daisy clocks are assumed to be slow by 10% and the SPI clock is assumed to be at the stated speed.

For an example, consider a stack of six devices. To get the full scan time with a daisy clock of 500kHz and SPI clock of 2MHz, it takes 77.6µs from the start of the Scan All command to the start of the internal scan of the Top device (see Table 31), 842µs to complete an internal scan of all voltages (see Table 34 on page 93), 5.337ms to read all cell voltages from all devices (see Table 42 on page 97), and 18µs delay before issuing another command. In this case, all cell voltages in the host controller can be updated every 6.28ms.

8.3.1 4-Byte Response

Tables 40 and 41 show the calculated timing for read operations for 4 byte responses. This is the timing for an ACK or NAK, as well as Read Register command.

8.3.2 40-Byte Response

Tables 42 and 43 on page 98 show the calculated timing for read operations for 40-byte responses. Specifically, this is the timing for a Read All Voltages command.

Table 40. Read Timing (Max): 4-Byte Response, Daisy Clock = 500kHz, SPI Clock = 2MHz

Top Stack Device	Command Time to Start of Response (Each Daisy Device) (µs)	Time to Complete Response (Daisy Chain) (µs)				Command + Response All Devices (µs)
		Master Device	Middle Device	Top Device	All Devices	
2	80	138		110	249	409
3	82	141	201	113	454	701
4	85	143	203	115	665	1003
5	87	145	206	117	879	1313
6	89	147	208	119	1098	1632
7	91	150	210	121	1322	1960
8	93	152	212	124	1549	2297
9	96	154	215	126	1782	2642
10	98	156	217	128	2019	2997
11	100	158	219	130	2260	3360
12	102	161	221	133	2505	3733
13	105	163	223	135	2756	4114
14	107	165	226	137	3010	4504

Table 41. Read Timing (Max): 4-Byte Response, Daisy Clock = 250kHz, SPI Clock = 2MHz

Top Stack Device	Command Time to Start of Response (Each Daisy Device) (µs)	Time to Complete Response (Daisy Chain) (µs)				Command + Response All Devices (µs)
		Master Device	Middle Device	Top Device	All Devices	
2	156	227		204	431	742
3	160	232	383	208	823	1303
4	165	236	388	213	1225	1883
5	169	241	392	217	1635	2479
6	173	245	397	221	2054	3094
7	178	250	401	226	2482	3726
8	182	254	406	230	2918	4377
9	187	258	410	235	3364	5044
10	191	263	415	239	3819	5730
11	196	267	419	244	4282	6434
12	200	272	423	248	4754	7155
13	205	276	428	253	5236	7894
14	209	281	432	257	5726	8651

Table 42. Read Timing (Max): 40-Byte Response, Daisy Clock = 500kHz, SPI Clock = 2MHz

Top Stack Device	Command Time to Start of Response (Each Daisy Device) (µs)	Time to Complete Response (Daisy Chain) (µs)				Command + Response All Devices (µs)
		Master Device	Middle Device	Top Device	All Devices	
2	80	642		750	1393	1553
3	82	645	841	753	2238	2485
4	85	647	843	755	3089	3427
5	87	649	846	757	3943	4377
6	89	651	848	759	4802	5336
7	91	654	850	761	5666	6304
8	93	656	852	764	6533	7281
9	96	658	855	766	7406	8266
10	98	660	857	768	8283	9261
11	100	662	859	770	9164	10264
12	102	665	861	773	10049	11277
13	105	667	863	775	10940	12298
14	107	669	866	777	11834	13328

Table 43. Read Timing (Max): 40-Byte Response, Daisy Clock = 250kHz, SPI Clock = 2MHz

Top Stack Device	Command Time to Start of Response (Each Daisy Device) (µs)	Time to Complete Response (Daisy Chain) (µs)				Command + Response All Devices (µs)
		Master Device	Middle Device	Top Device	All Devices	
2	156	731		1484	2215	2526
3	160	736	1663	1488	3887	4367
4	165	740	1668	1493	5569	6227
5	169	745	1672	1497	7259	8103
6	173	749	1677	1501	8958	9998
7	178	754	1681	1506	10666	11910
8	182	758	1686	1510	12382	13841
9	187	762	1690	1515	14108	15788
10	191	767	1695	1519	15843	17754
11	196	771	1699	1524	17586	19738
12	200	776	1703	1528	19338	21739
13	205	780	1708	1533	21100	23758
14	209	785	1712	1537	22870	25795

8.3.3 22-Byte Response

Table 44 and Table 45 show the calculated timing of read operations for 22-byte responses. This is the timing for Read All Temperature or Read All Faults command.

Table 44. Read Timing (Max): 22-Byte Response, Daisy Clock = 500kHz, SPI Clock = 2MHz

Top Stack Device	Command Time to Start of Response (Each Daisy Device) (µs)	Time to Complete Response (Daisy Chain) (µs)				Command + Response All Devices (µs)
		Master Device	Middle Device	Top Device	All Devices	
2	80	390		430	821	981
3	82	393	521	433	1346	1593
4	85	395	523	435	1877	2215
5	87	397	526	437	2411	2845
6	89	399	528	439	2950	3484
7	91	402	530	441	3494	4132
8	93	404	532	444	4041	4789
9	96	406	535	446	4594	5454
10	98	408	537	448	5151	6129
11	100	410	539	450	5712	6812
12	102	413	541	453	6277	7505
13	105	415	543	455	6848	8206
14	107	417	546	457	7422	8916

Table 45. Read Timing (Max): 22-Byte Response, Daisy Clock = 250kHz, SPI Clock = 2MHz

Top Stack Device	Command Time to Start of Response (Each Daisy Device) (µs)	Time to Complete Response (Daisy Chain) (µs)				Command + Response All Devices (µs)
		Master Device	Middle Device	Top Device	All Devices	
2	156	479		844	1323	1634
3	160	484	1023	848	2355	2835
4	165	488	1028	853	3397	4055
5	169	493	1032	857	4447	5291
6	173	497	1037	861	5506	6546
7	178	502	1041	866	6574	7818
8	182	506	1046	870	7650	9109
9	187	510	1050	875	8736	10416
10	191	515	1055	879	9831	11742
11	196	519	1059	884	10934	13086
12	200	524	1063	888	12046	14447
13	205	528	1068	893	13168	15826
14	209	533	1072	897	14298	17223

9. System Diagnostics Functions

The system uses the following four types of faults to determine the overall health of the system.

- Automatic Fault detection within the IC.
- Fault detection that is automatic, but requires the host microcontroller to initiate an operation.
- Faults that are detected by the host microcontroller during normal communication. This includes lack of response or responses that indicate a fault condition.
- Faults that are detected by the host microcontroller following a series of commands and responses that check various internal and external circuits.

9.1 Hardware Fault Detection

The ISL78600 is always checking the internal V3P3, V2P5, and VREF power supplies using window comparators. If any of these voltages exceed a programmed limit (either too high or too low), then a REG fault exists. This immediately starts an alarm response. See “Alarm Response” on page 106.

The ISL78600 also checks the two oscillators continually. The high speed and low speed oscillators are compared against limits and against each other. If there is a deviation greater than programmed, then an OSC fault exists. This immediately starts an alarm response. See “Alarm Response” on page 106.

9.2 System Out of Limit Detection

Bits are set in the fault data registers for detection of:

- Overvoltage
- Undervoltage
- Open wires
- Over-temperature
- Open V_{BAT}
- Open VSS

The overvoltage, undervoltage, over-temperature, and open-wire conditions have individual fault bits for each cell input. These bits are OR’d and reflected to bits in the Fault Status register (one bit per data register). The Open V_{BAT} and Open VSS have one bit each in the Fault Status register.

These conditions are not detected unless the host initiates a scan operation. The cell overvoltage, cell undervoltage, V_{BAT} open, and VSS open faults are sampled at the same time at the end of a Scan Voltages command. The cell undervoltage and cell overvoltage signals are also checked following a Measure cell voltage command. These conditions are also checked during a scan continuous operation. If the host initiates a scan continuous operation, then the status is checked automatically every scan cycle, without further host involvement. For any other scan command, the host needs to periodically send the command to perform another check of the system.

9.3 Fault Signal Filtering

Filtering is provided for the cell overvoltage, cell undervoltage, V_{BAT} open, and VSS open tests. These fault signals use a totalizing method in which an unbroken sequence of positive results is required to validate a fault condition. The sequence length (number of sequential positive samples) is set by the [TOT2:0] bits in the Fault Setup register (see Table 46 on page 101).

Table 46. Fault Setup Register

REGISTER BITS																	
12	11	10	9		8		7	6	5		4		3	2	1	0	
TST4	TST3	TST2	TST1	Enable	TST0	Internal Temperature	TOT2	TOT1	TOT0	Totalizer Count	WSCN	Scan Wires	SCN1	SCN0	SCN1	SCN0	Scan Interval Time (ms)
0	0	0	0	None	0	Disable	0	0	0	1	0	Track Voltage Scan	0	0	0	0	16
x	x	x	1	ExT1	1	Enable	0	0	1	2	1	Track Temp Scan	0	0	0	1	32
x	x	1	x	ExT2			0	1	0	4			0	0	1	0	64
x	1	x	x	ExT3			0	1	1	8			0	0	1	1	128
1	x	x	x	ExT4			1	0	0	16			0	1	0	0	256
							1	0	1	32			0	1	0	1	512
							1	1	0	64			0	1	1	0	1024
							1	1	1	128			0	1	1	1	2048
													1	0	0	0	4096
													1	0	0	1	8192
													1	0	1	0	16384
													1	0	1	1	32768
													1	1	0	0	65536

If the host sends a Scan Continuous command, then the Scan Interval code and the totalizer count value set the Fault Detection time (see Table 47).

Each cell input, V_{BAT}, and VSS open circuits has separate filter functions. The filter is reset whenever a test results in a negative result (no fault). All filters are reset when the Fault Status register bits are changed. When a fault is detected, the bits must be rewritten.

Any out of limit condition generates an Alarm response. See “Alarm Response” on page 106.

Table 47. Fault Detection Time as a Function of Scan Interval and Number of Totalizer Samples

Fault Setup Register Bits (TOT2:TOT0)		000	001	010	011	100	101	110	111
Totalizer Count		1	2	4	8	16	32	64	128
Scan Interval Code	Scan Interval (ms)	Fault Detection Time (ms)							
0000	16	16	32	64	128	256	512	1024	2048
0001	32	32	64	128	256	512	1024	2048	4096
0010	64	64	128	256	512	1024	2048	4096	8192
0011	128	128	256	512	1024	2048	4096	8192	16384
0100	256	256	512	1024	2048	4096	8192	16384	32768
0101	512	512	1024	2048	4096	8192	16384	32768	65536
0110	1024	1024	2048	4096	8192	16384	32768	65536	131072
0111	2048	2048	4096	8192	16384	32768	65536	131072	262144
1000	4096	4096	8192	16384	32768	65536	131072	262144	524288
1001	8192	8192	16384	32768	65536	131072	262144	524288	1048576
1010	16384	16384	32768	65536	131072	262144	524288	1048576	2097152
1011	32768	32768	65536	131072	262144	524288	1048576	2097152	4194304
1100	65536	65536	131072	262144	524288	1048576	2097152	4194304	8388608

9.4 Diagnostic Activity Settling Time

The majority of diagnostic functions within the ISL78600 do not affect other system activity and there is no requirement to wait before conducting further measurements. The exceptions to this are the open-wire test and cell balancing functions.

9.4.1 Open-Wire Test

The open-wire test loads each VCn pin in turn with 150µA or 1mA current. This disturbs the cell voltage measurement while the test is being applied such as, a 1mA test current applied with an input path resistance of 1kΩ reduces the pin voltage by 1V. The time required for the cell voltage to settle following the open-wire test is dependent on the time constant of components used in the cell input circuit. The standard input circuit (Figure 52 on page 42) with the components given in Table 13 on page 48 provide settling to within 0.1mV in approximately 2.8ms. This time should be added at the end of each open-wire scan to allow the cell voltages to settle.

9.4.2 Cell Balancing

The standard applications circuit (Figure 52 on page 42) configures the balancing circuits so that the cell input measurement reads close to zero volts when balancing is activated. There are time constants associated with the turn-on and turn-off characteristics of the cell balancing system that must be allowed for when conducting cell voltage measurements.

The turn-on time of the balancing circuit is primarily a function of the 25µA drive current of the cell balancing output and the gate charge characteristic of the MOSFET and needs to be determined for a particular setup. Turn-on settling times to within 2mV of final “on” value are typically less than 5ms.

The turn-off time is a function of the MOSFET gate charge and the VGS connected resistor and capacitor values (for example R_{27} and C_{27} in Figure 52 on page 42) and is generally longer than the turn-on time. As with the turn-on case, the turn-off time needs to be determined for the particular components used. Turn-off settling times in the range 10ms to 15ms are typical for settling to within 0.1mV of final value.

9.5 Memory Checksum

Two checksum operations are available to the host microcontroller for checking memory integrity, one for the EEPROM and one for the Page 2 registers.

Two registers are provided to verify the contents of EEPROM memory. One (Page 4, address 6’h3F) contains the correct checksum value, which is calculated during factory testing. The other (Page 5, address 6’h00) contains the checksum value calculated each time the nonvolatile memory is loaded to shadow registers, either after a power cycle or after a software reset (receiving a Reset command). An inequality between these two numbers indicates corruption of the shadow register contents (and possible corruption of EEPROM data). The external microcontroller needs to compare the two registers, because it is not automatic. Resetting the device (using the Reset command) reloads the shadow registers. A persistent difference between these two checksum register values indicates EEPROM corruption.

All Page 2 registers (device configuration registers) are subject to a checksum calculation. A Calculate Register Checksum command calculates the Page 2 checksum and saves the value internally (it is not accessible). The Calculate Register Checksum command can be run any time, but should be sent whenever a Page 2 register is changed.

A Check Register Checksum command recalculates the Page 2 checksum and compares it to the internal value. The occurrence of a Page 2 checksum error sets the PAR bit in the Fault Status register and causes a Fault response accordingly. The normal response to a PAR error is for the host microcontroller to rewrite the Page 2 register contents. A PAR fault also causes the device to cease any scanning or cell balancing activity.

See items 42 through 49 in Table 51 on page 107.

9.6 Communication Faults

There is no specific flag to indicate a communications fault. A fault is indicated by receiving an abnormal communications response or by an absence of all communications.

Non-daisy chain device commands and responses use CRC (Cyclical Redundancy Check) error detection. Stand-alone systems do not use the CRC. If a CRC is not recognized by a target device, a command includes an Address All when it is not allowed, or if there are too few bits in the sequence there is a NAK response. The host can tell where this fault occurred by reading the Device address.

If there is no response, then there is a communications failure.

9.7 Communications Failure

All commands except the Scan Voltages, Scan Temperatures, Scan Mixed, Scan Wires, Scan All, Measure, and Reset have a response from either the stack Top device or the target device. Correct receipt of a command is indicated by the correct response. The Wakeup command is a special case. If any Daisy Chain Middle device is in Sleep mode, while another device above it in the stack is not in Sleep mode, there is no response. Otherwise the Wakeup command responds with ACK. (For a summary of Command responses, see Table 15 on page 52).

Each device in the stack waits for a response from the stack device above. A device that does not receive a response within a timeout period reports a Communications Failure. The timeout value in each device is stack position dependent, with a device farther from the top waiting longer for the response. The device that detects the fault transmits the Communications Failure response, which includes its Device Address.

Table 48 shows the minimum time the host should wait for a response before sending a new command to the Master device.

Table 48. Maximum Time to Communications Failure Response

Communications Failure Wait Time For	Daisy Chain Data Rate (kHz) Note 25				Unit
	500	250	125	62.5	
2 Devices in the stack	330	660	1320	2640	µs
3 Devices in the stack	510	1010	2010	4010	µs
4 Devices in the stack	700	1390	2780	5550	µs
5 Devices in the stack	950	1900	3790	7570	µs
6 Devices in the stack	1250	2490	4980	9950	µs
7 Devices in the stack	1610	3220	6430	12850	µs
8 Devices in the stack	2070	4140	8280	16550	µs
9 Devices in the stack	2620	5240	10480	20950	µs
10 Devices in the stack	3280	6560	13120	26230	µs
11 Devices in the stack	4070	8140	16280	32560	µs
12 Devices in the stack	5170	10340	20680	41360	µs
13 Devices in the stack	6270	12540	25080	50160	µs
14 Devices in the stack	7810	15620	31240	62480	µs

25. The times are the longest expected wait times for communications to time-out. Typical wait times are approximately 10% shorter than the times in the table. The times are measured from the falling edge of the eighth clock in the first byte of the command received by the Master to the first falling edge of the $\overline{\text{DataReady}}$ signal.

As an example, assume that the system has a stack of ten devices. Since a break in the daisy chain can happen anywhere, and since the wait times are different for each device, it is likely best for the system programmer to build in a delay time equal to the response from the device farthest from the top. In this case, the host would wait at least 3.28ms for a response before issuing a command to try to clear the fault or declaring a daisy chain no-response fault.

If the target device receives a Communications Failure response from the device above, then the target device relays the Communications Failure followed by the requested data (in the case of a read) or simply relays the Communications Failure only (in the case of a Write, Balance command, etc).

A Communications Failure response can be caused by one of three circumstances:

- The communications system has been compromised, such as a component failure or broken wire,
- One or more devices in the stack are in Sleep mode. A device would go to Sleep mode if it doesn't receive valid communications before its watchdog timer expires. There are three ways this might occur in a system. Different devices might have been programmed with different WDT timeout values. Each device has its own oscillator, so the timeout is a little different for each device. Finally, if the system communicates with some, but not all devices, such as if the host repeatedly reads the status of the top device in a stack of four devices, then the top device and the master receive valid communications, but the middle two devices do not. So the middle devices time out.
- A daisy chain input port is in the wrong idle state.

This latter condition is unlikely but could arise in response to external influence, such as a large transient event. The daisy chain ports are forced to the correct idle condition at the end of each communication. An external event would have the potential to “flip” the input such that the port settles in the inverse state.

A flipped input condition recovers during the normal course of communications. If a flipped input is suspected, having received notification of a communications fault condition for example, the user can send a sequence of all 1s (that is, a command of FF FF FF FF) to clear the fault. Wait for the resulting NAK response and then send an ACK to the device that reported the fault. The “all 1” sequence allows a device to correct a flipped condition through the normal end of the communication process. If the microcontroller communication code requires that the command CRC be valid, the command FB FF FF FF also works to return to the idle state.

If a command results in a Communications Failure response, the next steps for the host microcontroller are:

1. Send a Sleep command (this makes sure that the Master is asleep prior to sending the Wakeup command, because if the Master is awake when it receives the Wakeup command, it does not send the Wakeup command on to the other stack devices),
2. Wait for all stack devices to go to sleep,
3. Send a Wakeup command,
4. Wait for the Wakeup command to propagate through the stack,
5. If successful, then the host microcontroller receives an ACK indicating that all devices are awake.
6. If there is no response, it could be an indication that more than one device was asleep (separated by devices that are awake.) If this is the case, repeat steps 1 through 5, until there is an ACK response.
7. If this loop is executed more times that there are devices in the stack, then there is likely a more significant break in communications.

9.8 Daisy Chain Communications Conflicts

Conflicts in the daisy chain system can occur if both a stack device and the host microcontroller are transmitting at the same time, or if more than one stack device transmits at the same time. Conflicts caused by a stack device transmitting at the same time as the host microcontroller are recognized by the absence of the required response (such as, an ACK response to a write command), or by the scan counter not being incremented in the case of Scan and Measure commands.

Conflicts which arise from more than one device transmitting simultaneously can occur if two devices detect faults at the same time. This can occur when the stack is operating normally (such as, if two devices register an undervoltage fault in response to a Scan Voltages command sent to all devices). It is recommended that the host microcontroller checks the Fault Status register contents of all devices whenever a Fault response is received from one device.

9.9 Loss of Signal From Host

A watchdog timer is provided as part of the daisy chain communications fault detection system. The watchdog has no effect in non-daisy chain systems.

Each device must receive a valid communications sequence before its watchdog timeout period is exceeded. A valid communications sequence is one that requires an action or response from the device. Address All commands, such as the Scan and Balance commands provide a simple way to reset the watchdog timers on all devices with a single communication. Single device communications (such as ACK) must be sent individually to each device to reset the watchdog timer in that device. A read of the Fault Status register of each device is also a good way to reset the watchdog timer on each device. This functionality guards against situations where a runaway host microcontroller might continually send data.

Failure to receive valid communications within the required time causes the WDGF bit to be set in the Fault Status register and the device to be placed in Sleep mode, with all measurement and balancing functions disabled. Daisy chain devices assert the $\overline{\text{FAULT}}$ output in response to a watchdog fault and maintain this asserted state while in Sleep mode. Notice that no watchdog fault response is automatically sent on the daisy chain interface.

9.9.1 Watchdog Function

The watchdog timeout is settable in two ranges using the lower 7 bits of the Watchdog/Balance time register (see Table 49). The low range (7'b0000001 to 7'b0111111) provides timeout settings in 1 second increments from 1 second to 63 seconds. The high range (7'b1000000 to 7'b1111111) provides timeout settings in 2 minute intervals from 2 minutes to 128 minutes (see Table 49 for details).

Table 49. Watchdog/Balance Time Register

Register Bits							
6	5	4	3	2	1	0	
WDG6	WDG5	WDG4	WDG3	WDG2	WDG1	WDG0	Watchdog Timeout
0	0	0	0	0	0	0	Disabled
0	0	0	0	0	0	1	1s
0	0	0	0	0	1	0	2s
•••							-
0	1	1	1	1	1	0	62s
0	1	1	1	1	1	1	63s
1	0	0	0	0	0	0	2 min
1	0	0	0	0	0	1	4 min
•••							-
1	1	1	1	1	1	0	126 min
1	1	1	1	1	1	1	128 min

A zero setting (7'b0000000) disables the watchdog function. A watchdog password function is provided to guard against accidental disabling of the watchdog function. The upper 6 bits of the Device Setup register must be set to 6'h3A (111010) to allow the watchdog to be set to zero. The watchdog is disabled by first writing the password to the Device Setup register (see "Setup Registers" on page 124) and then writing zero to the lower bits of the Watchdog/Balance time register. The password function does not prevent changing the watchdog timeout setting to a different nonzero value.

The watchdog continues to function when the ISL78600 is in Sleep mode. Parts in Sleep mode assert the $\overline{\text{FAULT}}$ output when the watchdog timer expires.

9.9.2 Watchdog Password

Before writing a zero to the watchdog timer, which turns off the timer, it is necessary to write a password to the [WP5:0] bits. The password value is 6'h3A.

9.10 Alarm Response

If any of the fault bits are set, the $\overline{\text{FAULT}}$ logic output is asserted low in response to the fault condition. The output then remains low until the bits of the Fault Status register are reset. Individual bits in the fault data registers must first be cleared before the associated bits in the Fault Status register can be cleared.

If the device is in a daisy chain, the Fault logic also sends an "unprompted" response down the daisy chain to the Master, which notifies the Host microcontroller that a problem exists.

The daisy chain fault response is immediate, so long as there is no communications activity on the device ports, and comprises the normal Fault Status register read response. As such, it includes the contents of the Status Register and includes the device address that is reporting the fault.

The Fault response is only sent for the first fault occurrence. Subsequent faults do not activate the Fault response until after the Fault Status register has been cleared. If multiple devices report a fault, the response shows the results from the lowest stack device.

If a fault occurs while the device ports are active, then the device waits until communications activity ceases before sending the Fault response. The host microcontroller has the option to wait for this response before sending the next message. Alternately the host microcontroller may send the next message immediately (after allowing the daisy chain ports to clear (see "Sequential Daisy Chain communications" on page 92). Any conflicts resulting from additional transmissions from the stack are recognized by the lack of response from the stack.

Table 50 provides the maximum time from $\overline{\text{DATA READY}}$ going low for the last byte of the normal response to $\overline{\text{DATA READY}}$ going low for the first byte of the Fault response in the case where a Fault response is held up by active communications.

Table 50. Maximum Time Between Data Ready Signals and Delayed Fault Response

	Daisy Chain Data Rate (kHz)				Unit
	500	250	125	62.5	
Maximum Time between $\overline{\text{DATA READY}}$ Assertions during delayed Fault Response	68	136	272	544	µs

Further read communications to the device return the Fault response followed by the requested data. Write communications return only the fault response. Action commands return nothing. The host microcontroller resets the register bits corresponding to the fault by writing 14'h0000 to the Fault Status register, having first cleared the bits in the fault data register(s) if these are set. The device then responds ACK as with a normal write response because the fault status bits are now cleared. This also prevents further Fault responses unless the fault reappears, in which case the Fault response is repeated.

Additionally, the fault status of each part can be obtained at any time by reading the Fault Status register.

The $\overline{\text{FAULT}}$ logic output is asserted in Sleep mode, if a fault has been detected and has not been cleared.

10. Fault Diagnostics

Table 51 shows a summary of commands and responses for the various fault diagnostics functions.

Table 51. Summary of Fault Diagnostic Commands and Responses

Item	Diagnostic Function	Action Required	Register Read/write	Comments
1	Static Fault Detection Functions	Check fault status (or look for normal fault response)	Read Fault Status Register	The main internal functions of the ISL78600 are monitored continuously. Bits are set in the *Fault Status* register in response to faults being detected in these functions.
2	Oscillator Check Function	Check for device in Sleep mode if stack returns a Communications Failure response.		Oscillator faults are detected as part of the Static Fault detection functions. The response to an oscillator fault detection is to set the *OSC* bit in the Fault Status register and then to enter Sleep mode. A sleeping device does not respond to normal communications, producing a Communications Failure notification from the next device down the stack. The normal recovery procedure is send repeated Sleep and Wakeup commands ensure all devices are awake.
3	Cell Overvoltage	Set cell overvoltage limit	Write Overvoltage Limit Register	Full scale value 14'h1FFF = 5V
4		Set fault filter sample value	Write TOT bits in Fault Setup Register	Default is 3'b011 (eight samples) - (see Table 46 on page 101)
5		Identify which inputs have cells connected	Write Cell Setup Register	A '0' bit value indicates cell is connected. A '1' bit value indicates no cell connected to this input. The overvoltage test is not applied to unconnected cells.
6		Scan cell voltages	Send Scan Voltages Command	A cell overvoltage condition is flagged after a number of sequential overvoltage conditions are recorded for a single cell. The number is programmed above in item 4.
7		Check fault status	Read Fault Status Register	The device sends the *Fault Status* register contents automatically if a fault is detected, if the register value is zero before the fault is detected.
8		Check overvoltage fault register	Read Overvoltage Fault Register	Only required if the *Fault Status* register returns a fault condition.
9		Reset fault bits		Reset bits in the Overvoltage Fault register followed and bits in the Fault Status register.
10		Reset fault filter		Change the value of the *[TOT2:0]* bits in the Fault Setup register and then change back to the required value. This resets the filter. The filter is also reset if a false overvoltage test is encountered.
11	Cell Undervoltage	Set cell undervoltage limit	Write Undervoltage Limit Register	Full scale value 14'h1FFF = 5V
12		Set fault filter sample value	Write TOT Bits in Fault Setup Register	Default is 3'b011 (eight samples)
13		Identify which inputs have cells connected	Write Cell Setup Register	A '0' bit value indicates cell is connected. A '1' bit value indicates no cell connected to this input. The undervoltage test is not applied to unconnected cells.
14		Scan cell voltages	Send Scan Voltages Command	A cell undervoltage condition is flagged after a number of sequential undervoltage conditions are recorded for a single cell. The number is programmed above in item 12.
15		Check fault status	Read Fault Status Register	The device sends the *Fault Status* register contents automatically if a fault is detected, if the register value is zero before the fault is detected.
16		Check undervoltage fault register	Read Undervoltage Fault Register	Only required if the Fault Status register returns a fault condition.
17		Reset fault bits		Reset bits in the Undervoltage Fault register followed by bits in the Fault Status register.

Table 51. Summary of Fault Diagnostic Commands and Responses (Continued)

Item	Diagnostic Function	Action Required	Register Read/write	Comments
18		Reset fault filter		Change the value of the *[TOT2:0]* bits in the Fault Setup register and then change back to the required value. This resets the filter. The filter is also reset if a false undervoltage test is encountered.
19	V_{BAT} or VSS Connection Test	Set fault filter sample value	Write TOT bits in Fault Setup Register	Default is 3'b011 (eight samples)
20		Scan cell voltages	Send Scan Voltages Command	A open condition on V_{BAT} or VSS is flagged after a number of sequential open conditions are recorded for a single cell. The number is programmed above in item 19.
21		Check fault status	Read Fault Status Register	The device sends the *Fault Status* register contents automatically if a fault is detected, if the register value is zero before the fault is detected.
22		Reset fault bits		Reset bits in the Fault Status register.
23		Reset fault filter		Change the value of the *[TOT2:0]* bits in the Fault Setup register and then change back to the required value. This resets the filter. The filter is also reset if a false open test is encountered.
24	Open Wire Test	Set scan current value	Write Device Setup Register: ISCN = 1 or 0	Sets scan current to 1mA (recommended) by setting ISCN = 1. Or, set the scan current to 150µA by setting ISCN = 0.
25		Identify which inputs have cells connected	Write Cell Setup Register	A '0' bit value indicates cell is connected. A '1' bit value indicates no cell connected to this input. Cell inputs VC2 to VC12: the open-wire detection system is disabled for cell inputs with a '1' setting in the Cell Setup register. Cell inputs VC0 and VC1 are not affected by the Cell Setup register.
26		Activate scan wires function	Send Scan Wires Command	Wait for Scan Wires to complete.
27		Check fault status	Read Fault Status Register	The device sends the Fault Status register contents automatically if a fault is detected, if the register value is zero before the fault is detected.
28		Check open-wire fault register	Read Open-Wire Fault Register	Only required if the Fault Status register returns a fault condition.
29		Reset fault bits		Reset bits in the open-wire fault register followed by bits in the Fault Status register.
30	Over-Temperature Indication	Set external temperature limit	Write External Temperature Limit Register	Full scale value 14'h3FFF = 2.5V
31		Identify which inputs are required to be tested	Write Fault Setup Register Bits TST1 to TST4	A '1' bit value indicates input is tested. A '0' bit value indicates input is not tested.
32		Scan temperature inputs	Send Scan Temperatures Command	An over-temperature condition is flagged immediately if the input voltage is below the limit value.
33		Check fault status	Read Fault Status Register	The device sends the Fault Status register contents automatically if a fault is detected, if the register value is zero before the fault is detected.
34		Check over-temperature fault register	Read Over-Temperature Fault Register	Only required if the Fault Status register returns a fault condition.
35		Reset fault bits		Reset bits in the Over-temperature Fault register followed by bits in the Fault Status register.
36	Reference Check Function	Read reference coefficient A	Read Reference Coefficient A Register	
37		Read reference coefficient B	Read Reference Coefficient B Register	

Table 51. Summary of Fault Diagnostic Commands and Responses (Continued)

Item	Diagnostic Function	Action Required	Register Read/write	Comments
38		Read reference coefficient C	Read Reference Coefficient C Register	
39		Scan temperature inputs	Send Scan Temperatures Command	
40		Read reference voltage value	Read Reference Voltage Register	
41		Calculate voltage reference value		See Voltage Reference Check Calculation in the Worked Examples section of this data sheet (see ““Voltage Reference Check Calculation” on page 110).
42	Register Checksum	Calculate register checksum value	Send Calculate Register Checksum Command	This causes the ISL78600 to calculate a checksum based on the current contents of the page 2 registers. This action must be performed each time a change is made to the register contents. The checksum value is stored for later comparison.
43		Check register checksum value	Send Check Register Checksum Command	The checksum value is recalculated and compared to the value stored by the previous Calc Register Checksum command. The PAR bit in the Fault Status register is set if these two numbers are not the same.
44		Check fault status	Read Fault Status Register	The device sends the Fault Status register contents automatically if a fault is detected, if the register value is zero before the fault is detected.
45		Rewrite registers	Load all page 2 Registers With Their Correct Values.	This is only required if a PAR fault is registered. It is recommended that the host reads back the register contents to verify values prior to sending a Calculate Register Checksum command.
46		Reset fault bits		Reset bits in the Fault Status register.
47	EEPROM MISR Checksum	Read checksum value stored in EEPROM	Read the EEPROM MISR Register	
48		Read checksum value calculated by ISL78600	Read the MISR Checksum Register	The checksum value is calculated each time the EEPROM contents are loaded to registers, either following the initial application of power or the device receiving a *Reset* command.
49		Compare checksum values		Correct function is indicated by the two values being equal. Memory corruption is indicated by an unequal comparison. In this event the host should send a *Reset* command and repeat the check process.

11. Worked Examples

The following worked examples are provided to assist with the setup and calculations associated with various functions.

11.1 Voltage Reference Check Calculation

Table 52. Example Register Data

R/W	Page	Address	Parameter	Value (Hex)	Decimal
0	001	010000	IC Temperature	14'h2425	9253
0	001	010101	Reference Voltage	14'h20A7	8359
0	010	111000	Coefficient C	14'h00A4	164
0	010	111001	Coefficient B	14'h3FCD	-51
0	010	111010	Coefficient A	9'h006	6

Coefficients A, B, and C are two's complement numbers.

Coefficients B and C have a range +8191 to -8192.

Coefficient A has a range +255 to -256.

Coefficient B in the example is a negative number (Hex value > 1FFF). The value for Coefficient B is 14'h3FCD - 14h3FFF- 1 or (16333_{10} - 16383_{10} - 1) = -51.

Coefficient A occupies the upper nine bits of register 6'b111010 (6'h3A). One way to extract the coefficient data from this register is to divide the complete register value by 32 and rounding the result down to the nearest integer. With 9'h006 in the upper nine bits, and assuming the lower five bits are 0, the complete register value is 14'h0C0 = 192 decimal. Divide this by 32 to obtain 6.

Coefficients A, B, and C are used with the IC temperature reading to calibrate the Reference Voltage reading. The calibration is applied by subtracting, from the Reference Voltage reading, an adjustment of the form:

(EQ. 6) $$\text{Adjustment} = \frac{A}{256 \times 8192} \times dT^2 + \frac{B}{8192} \times dT + C$$

An example calculation using the data of Table 52 is given in Equation 7.

(EQ. 7) $$dT = \frac{9253 - 9180}{2} = 36.5$$

where 9180 is the Internal Temperature Monitor reading at +25°C (see the "Electrical Specifications" table, T_{INT25} on page 13).

(EQ. 8) $$\text{Adjustment} = \frac{6}{256 \times 8192} \times (36.5)^2 - \frac{51}{8192} \times 36.5 + 164 = 163.8$$

(EQ. 9) $$\text{Corrected } V_{REF} = 8359 - 163.8 = 8195.2$$

(EQ. 10) $$V_{REF} \text{ value} = \frac{8195.2}{16384} \times 5 = 2.5010$$

11.2 Cell Balancing – Manual Mode

See "Manual Balance Mode" on page 63.

11.2.1 Example: Activate balancing on cells 1, 5, 7 and 11

1. Write Balance Setup register: Set Manual Balance mode, Balance Status pointer, and turn off balance.

   BMD = 01 (**Manual Balance mode**)
   BWT = XXX
   BSP = 0000 (Balance status pointer location 0)
   BEN = 0 (Balancing disabled)

Table 53. Write Balance Setup Register (Manual Balance)

Device Address	R/W	Page	Address	Data	CRC
AAAA	1	010	010011	XX XX00 000X XX01	CCCC

X = Do not care
AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

2. Write Balance Status register: Set BAL[0], BAL[4], BAL[6], BAL[10]

   BAL12:1 = 0100 0101 0001

Table 54. Write Balance Status Register (Manual Balance)

Device Address	R/W	Page	Address	Data	CRC
AAAA	1	010	010100	XX 0100 0101 0001	CCCC

X = Do not care
AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

3. Enable balancing using Balance Enable command

Table 55. Send "Balance Enable" Command

Device Address	R/W	Page	Address	Data	CRC
AAAA	0	011	010000	00 0000	CCCC

AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

or enable balancing by setting BEN directly in the Balance Setup register:

BEN = 1

Table 56. Write Balance Setup Register

Device Address	R/W	Page	Address	Data	CRC
AAAA	1	010	010011	XX XX1X XXXX XXXX	CCCC

X = Do not care
AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

The balance FETs attached to Cells 1, 5, 7, and 11 turn on.

Turn balancing off by resetting BEN or by sending the Balance Inhibit command (Page 3, address 6'h11).

11.3 Cell Balancing – Timed Mode

See "Timed Balance Mode" on page 64.

11.3.1 Example: Activate Balancing on Cells 2 and 8 for 1 Minute

1. Write Balance Setup register: Set Timed Balance mode, Balance Status pointer, and turn off balance.

   BMD = 10 (Timed Balance mode)
   BWT = XXX
   BSP = 0000 (Balance status pointer location 0)
   BEN = 0 (BALANCING disabled)

Table 57. Write Balance Setup Register (Timed Balance)

Device Address	R/W	Page	Address	Data	CRC
AAAA	1	010	010011	XX XX00 000X XX10	CCCC

X = Do not care
AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

2. Write Balance Status register: Set BAL[1] and BAL[7]

   BAL12:1 = 0000 1000 0010

Table 58. Write Balance Status Register (Timed Balance)

Device Address	R/W	Page	Address	Data	CRC
AAAA	1	010	010100	XX 0000 1000 0010	CCCC

X = Do not care
AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

3. Write balance timeout setting to the Watchdog/Balance Time register (Page 2, address 6'h15, Bits [13:7])

   BTM6:1 = 0000011 (1 minute)

Table 59. Write Watchdog/Balance Time Register (Timed Balance)

Device Address	R/W	Page	Address	Data	CRC
AAAA	1	010	010101	00 0001 1XXX XXXX	CCCC

X = The lower bits are the watchdog timeout value and should be set to a time longer than the balance time. (111 1111) is suggested.
AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

4. Enable balancing using Balance Enable command

Table 60. Send "Balance Enable" Command (Timed Balance)

Device Address	R/W	Page	Address	Data	CRC
AAAA	0	011	010000	00 0000	CCCC

AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

or enable balancing by setting BEN directly in the Balance Setup register:

BEN = 1

Table 61. Write Balance Setup Register (Timed Balance)

Device Address	R/W	Page	Address	Data	CRC
AAAA	1	010	010011	XX XX1X XXXX XXXX	CCCC

X = Do not care.
AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

The balance FETs attached to Cells 2 and 8 turn on. The FETs turn off after 1 minute. Balancing can be stopped by resetting BEN or by sending the Balance Inhibit command.

11.4 Cell Balancing – Auto Mode

See "Auto Balance Mode" on page 65.

11.4.1 Balance Value Calculation Example

This example is based on a cell State of Charge (SOC) of 9360 coulombs, a target SOC of 8890 coulombs, a balancing leg impedance of 31Ω (30Ω resistor plus 1Ω FET on resistance) and a sampling time interval of 5 minutes (300 seconds).

The Balance Value is calculated using Equation 11.

(EQ. 11) $$B = \frac{8191}{5} \times (9360 - 8890) \times \frac{31}{300} = 79562 = 28'h00136CA$$

The value 8191/5 is the scaling factor of the cell voltage measurement.

The value of 28'h00136CA is loaded to the required Cell Balance Register and the value 7'b0001111 (5 minutes) is loaded to the Balance Time bits in the Watchdog/Balance time register.

In this example, the total coulomb difference to be balanced is: 470 coulomb (9360 - 8890). At 3.3V/31Ω * 300s = 31.9 coulomb per cycle it takes about 15 cycles for the balancing to terminate.

11.4.2 Auto Balance Mode Cell Balancing Example

The following describes a simple setup to demonstrate the Auto Balance mode cell balancing function of the ISL78600. Note that this balancing setup is not related to the balance value calculation in Equation 11.

Auto balance cells using the following criteria:

- Balance time = 20 seconds
- Balance wait time (dead time between balancing cycles) = 8 seconds
- Balancing disabled during cell measurements.
- Balance Values: See Table 62

Table 62. Cell Balance Values (HEX) for Each Cell

Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cell 8	Cell 9	Cell 10	Cell 11	Cell 12
28'h406A	28'h3E4D	28'h0	28'h292F	28'h3E00	28'h0	28'h2903	28'h3D06	28'h0	28'h151E	28'h502	28'h6D6

Balance Status Register: Set up balance see Table 63:

Cells 1, 4, 7, and 10 on 1st cycle.
Cells 3, 6, 9, and 12 on 2nd cycle.
Cells 2, 5, 8, and 11 on 3rd cycle

Table 63. Balance Status Register Setup (Auto Balance)

	Cell											
BPS [3:0]	1	2	3	4	5	6	7	8	9	10	11	12
0000	Reserved for Manual Balance mode and Timed Balance mode											
0001	1	0	0	1	0	0	1	0	0	1	0	0
0010	0	0	1	0	0	1	0	0	1	0	0	1
0011	0	1	0	0	1	0	0	1	0	0	1	0
0100	0	0	0	0	0	0	0	0	0	0	0	0

Table 63. Balance Status Register Setup (Auto Balance) (Continued)

BPS [3:0]	Cell											
	1	2	3	4	5	6	7	8	9	10	11	12
0101 - 1111	Not needed											

1. Write Balance Value registers

Table 64. Setup Balance Value Registers (For Cell1) - Value 28'h406A (Auto Balance)

Address		Register Bit													
		13	12	11	10	9	8	7	6	5	4	3	2	1	0
6'20	Bit	B0113	B0112	B1011	B0110	B0109	B0108	B0107	B0106	B0105	B0104	B0103	B0102	B0101	B0100
	Value	0	0	0	0	0	0	0	1	1	0	1	0	1	0
6'21	Bit	B0127	B0126	B0125	B0124	B0123	B0122	B0121	B0120	B0119	B0118	B0117	B0116	B0115	B0114
	Value	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 65. Write Balance Value Register (Auto Balance)

For Cell Number	Write Value Register Command					
	Device Address	$\overline{R}$/W	Page	Address	Data (Hex)	CRC
1	AAAA	1	010	100000	14'h006A	CCCC
	AAAA	1	010	100001	14'h0001	CCCC
2	AAAA	1	010	100010	14'h3E4D	CCCC
	AAAA	1	010	100011	14'h0000	CCCC
3	AAAA	1	010	100100	14'h0000	CCCC
	AAAA	1	010	100101	14'h0000	CCCC
4	AAAA	1	010	100110	14'h292F	CCCC
	AAAA	1	010	100111	14'h0000	CCCC
5	AAAA	1	010	101000	14'h3E00	CCCC
	AAAA	1	010	101001	14'h0000	CCCC
6	AAAA	1	010	101010	14'h0000	CCCC
	AAAA	1	010	101011	14'h0000	CCCC
7	AAAA	1	010	101100	14'h2903	CCCC
	AAAA	1	010	101101	14'h0000	CCCC
8	AAAA	1	010	101110	14'h3D06	CCCC
	AAAA	1	010	101111	14'h0000	CCCC
9	AAAA	1	010	110000	14'h0000	CCCC
	AAAA	1	010	110001	14'h0000	CCCC
10	AAAA	1	010	110010	14'h151E	CCCC
	AAAA	1	010	110011	14'h0000	CCCC
11	AAAA	1	010	110100	14'h0502	CCCC
	AAAA	1	010	110101	14'h0000	CCCC
12	AAAA	1	010	110110	14'h06D6	CCCC
	AAAA	1	010	110111	14'h0000	CCCC

AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

2. Write BDDS bit in Device Setup register (turn balancing functions off during measurement)

   BDDS = 1

Table 66. Write Device Setup Register (Auto Balance)

Device Address	R/W	Page	Address	Data	CRC
AAAA	1	010	011001	XX XXXX 1XXX XXXX	CCCC

X = Do not care.
AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

3. Write balance timeout setting to the Watchdog/Balance Time register: Balance timeout code = 0000001 (20 seconds)

   BTM6:0 = 000 0001

Table 67. Write Balance Timeout Register (Auto Balance)

Device Address	R/W	Page	Address	Data	CRC
AAAA	1	010	010101	00 0000 1XXX XXXX	CCCC

X = The lower bits are the watchdog timeout value and should be set to a time longer than the balance time. (111 1111) is suggested.
AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

4. Setup Balance Status register (from Table 63 on page 113)

This operation is a repetitive process that consists of writing to the Balance Setup Register to set a pointer to a location in the Balance Status Register, then writing the Balance Status Register. Since the Balance Status Register needs to write four locations, this operation is repeated four times.

The following bits are set as part of the procedure. They can be set on the last step or re-written each time. In this example, the bits are re-written in each step.

BMD = 11 (Auto Balance mode)
BWT = 100 (8 seconds)
BEN = 0 (Balancing disabled

This operation starts by setting the Balance Status Pointer to 1.

BSP = 0001 (Balance status pointer = 1)

a. Write Balance Setup register: Set Auto Balance mode, set 8 second Balance wait time, and set balance off:

Table 68. Write Balance Setup Register (Auto Balance - Pointer = 1)

Device Address	R/W	Page	Address	Data	CRC
AAAA	1	010	010011	XX XX00 0011 0011	CCCC

X = Do not care.
AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

b. Write Balance Status register: Set Bits 1, 4, 7, and 10

BAL12:1 = 0010 0100 1001

Table 69. Write Balance Status Register (Auto Balance - Pointer = 1)

Device Address	R/W	Page	Address	Data	CRC
AAAA	1	010	010100	XX 0010 0100 1001	CCCC

X = Do not care.
AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

c. Write Balance Setup register: Set Balance Status Pointer = 2

BSP = 0010 (Balance status pointer = 2)

Table 70. Write Balance Setup Register (Auto Balance - Pointer = 2)

Device Address	R/W	Page	Address	Data	CRC
AAAA	1	010	010011	XX XX00 0101 0011	CCCC

X = Do not care.
AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

d. Write Balance Status register: Set Bits 3, 6, 9, and 12

BAL12:1 = 1001 0010 0100

Table 71. Write Balance Status Register (Auto Balance - Pointer = 2)

Device Address	R/W	Page	Address	Data	CRC
AAAA	1	010	010100	XX 1001 0010 0100	CCCC

X = Do not care.
AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

e. Write Balance Setup register: Set Balance Status Pointer = 3

BSP = 0011 (Balance status pointer = 3)

Table 72. Write Balance Setup Register (Auto Balance - Pointer = 3)

Device Address	R/W	Page	Address	Data	CRC
AAAA	1	010	010011	XX XX00 0111 0011	CCCC

X = Do not care.
AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

f. Write Balance Status register: Set Bits 2, 5, 8, and 11

BAL12:1 = 0100 1001 0010

Table 73. Write Balance Status Register (Auto Balance - Pointer = 3)

Device Address	R/W	Page	Address	Data	CRC
AAAA	1	010	010100	XX 0100 1001 0010	CCCC

X = Do not care.
AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

g. Write Balance Setup register: Set Balance Status Pointer = 4

BSP = 0100 (Balance status pointer = 4)

Table 74. Write Balance Setup Register (Auto Balance - Pointer = 4)

Device Address	R/W	Page	Address	Data	CRC
AAAA	1	010	010011	XX XX00 1001 0011	CCCC

X = Do not care.
AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

h. Write Balance Status register: Set bits to all zero to set the end point for the instances.

BAL12:1 = 0000 0000 0000

Table 75. Write Balance Status Register (Auto Balance - Pointer = 4)

Device Address	R/W	Page	Address	Data	CRC
AAAA	1	010	010100	XX 0000 0000 0000	CCCC

X = Do not care.
AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

5. Enable balancing using Balance Enable command

Table 76. Send “Balance Enable” Command (Auto Balance)

DEVICE ADDRESS	R/W	PAGE	ADDRESS	DATA	CRC
AAAA	0	011	010000	00 0000	CCCC

AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

or enable balancing by setting BEN directly in the Balance Setup register:

BEN = 1

Table 77. Write Balance Setup Register (Auto Balance)

DEVICE ADDRESS	R/W	PAGE	ADDRESS	DATA	CRC
AAAA	1	010	010011	XX XX1X XXXX XXXX	CCCC

X = Do not care.
AAAA = Device Address in Daisy Chain. Not needed in Stand-Alone
CCCC = CRC value in Daisy Chain. Not needed in Stand-Alone

The balance FETs cycle through each instance of the Balance Status register in a loop, interposing the balance wait time between each instance. The measured voltage of each cell being balanced is subtracted from the balance value for that cell at the end of each Balance Status instance. The process continues until the Balance Value register for each cell contains zero.

12. System Registers

System registers contain 14-bits each. All register locations are memory mapped using a 9-bit address. The MSBs of the address form a 3-bit page address. Page 1 (3'b001) registers are the measurement result registers for cell voltages and temperatures. Page 3 (3'b011) is used for commands. Pages 1 and 3 are not subject to the checksum calculations. Page addresses 4 and 5 (3'b100 and 3b'101), with the exception of the EEPROM checksum registers, are reserved for internal functions.

All Page 2 registers (device configuration registers) and EEPROM checksum registers are subject to a checksum calculation. The checksum is calculated in response to the CRC command using a Multiple Input Shift Register (MISR) error detection technique. The checksum is tested in response to a Check Register Checksum command. The occurrence of a checksum error sets the PAR bit in the Fault Status register and causes a Fault response accordingly. The normal response to a PAR error is for the host microcontroller to rewrite the Page 2 register contents. A PAR fault also causes the device to cease any scanning or cell balancing activity.

A description of each register is included in Register Descriptions and includes a depiction of the register with bit names and initialization values at power up or when the device receives a Reset command. Bits which reflect the state of external pins are notated "Pin" in the initialization space. Bits which reflect the state of nonvolatile memory bits (EEPROM) are notated "NV" in the initialization space. Initialization values are shown below each bit name.

Reserved bits (indicated by gray areas) should be ignored when reading and should be set to "0" when writing to them.

12.1 Register Descriptions

Register locations identified as "N/A" are not available and reserved for future use.

12.1.1 Cell Voltage Data

Base Address (Page)	Access	Address Range	Description
3'b001	Read Only	6'h00 - 6'h0C and 6'h0F	**Measured cell voltage and pack voltage values** Address 001111 accesses all cell and Pack Voltage data with one read operation. See Figure 88 on page 84. Cell values are output as 13-bit signed integers with the 14th bit (MSB) denoting the sign, (for example, positive full scale is 14'h1FFF, 8191 decimal, negative full scale is 14'h2000, 8192 decimal). V_{BAT} is a 14-bit unsigned integer.

Access	Page Address	Register Address		Description
Read Only	3'b001	6'h00	VBAT Voltage	$VCx = \frac{(HEXvalue_{10} - 16384) \times 2 \times 2.5}{8192}$ if…$HEXvalue_{10} \geq 8191$ $VCx = \frac{HEXvalue_{10} \times 2 \times 2.5}{8192}$ if…$HEXvalue_{10} < 8191$ $V_{BAT} = \frac{HEXvalue_{10} \times 15.9350784 \times 2.5}{8192}$ $HEXvalue_{10}$ = Hex to Decimal conversion of the register contents.
		6'h01	Cell 1 Voltage	
		6'h02	Cell 2 Voltage	
		6'h03	Cell 3 Voltage	
		6'h04	Cell 4 Voltage	
		6'h05	Cell 5 Voltage	
		6'h06	Cell 6 Voltage	
		6'h07	Cell 7 Voltage	
		6'h08	Cell 8 Voltage	
		6'h09	Cell 9 Voltage	
		6'h0A	Cell 10 Voltage	
		6'h0B	Cell 11 Voltage	
		6'h0C	Cell 12 Voltage	
		6'h0F	Read all cell voltages	

12.2 Temperature Data, Secondary Voltage Reference Data, Scan Count

Base Address (Page)	Access	Address Range	Description
3'b001	See individual register	6'h10 - 6'h16 and 6'h1F	**Measured temperature, Secondary reference, Scan Count** Address 011111 accesses all these data in a continuous read (see Figure 88 on page 84.) Temperature and reference values are output as 14-bit unsigned integers, (such as, full scale is 14'h3FFF (16383 decimal)).

Access	Page Address	Register Address		Description
Read Only	3'b001	6'h10	Internal temperature reading.	$T_{INTERNAL}(°C) = \frac{HEXvalue_{10} - 9180}{31.9} + 25$ $HEXvalue_{10}$ = Hex to Decimal conversion of the register contents.
		6'h11	External temperature Input 1 reading.	$V_{TEMP} = \frac{HEXvalue_{10} \times 2.5}{16384}$ $T_{EXTERNAL}(°C) = V_{TEMP} \times R_{DIVIDER}$ $R_{DIVIDER}$ depends on the external resistor divider circuit that includes an NTC thermistor (see Figure 50 on page 39 for an example external circuit.)
		6'h12	External temperature Input 2 reading.	
		6'h13	External temperature Input 3 reading.	
		6'h14	External temperature Input 4 reading.	
		6'h15	Reference voltage (raw ADC) value. Use to calculate corrected reference value using reference coefficient data. See Page 2 data, address 6'h38 – 6'h3A.	

<table>
<tr><th>Access</th><th>Page Address</th><th>Register Address</th><th>Description (Continued)</th></tr>
<tr><td>Read/ Write</td><td>3’h001</td><td>6’h16</td><td>Scan Count
Current scan instruction count. Count is incremented each time a scan command is received and wraps to zero when overflowed. Register can be compared to previous value to confirm scan command receipt.
Bit Designations:
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="10">N/A</td><td>SCN 3</td><td>SCN 2</td><td>SCN 1</td><td>SCN 0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>Read Only</td><td>3’h001</td><td>6’h1F</td><td>Read all: Temperature Data, Secondary Voltage Reference Data, Scan Count (locations 6’h10 - 6’h16)</td></tr>
</table>

12.3 Fault Registers

Base Address (Page)	Access	Address Range	Description
3'h010	Read/ Write	6'h00 - 6'h05 and 6'h0F	**Fault registers** Fault setup and status information. Address 6'h0F accesses all fault data in a continuous read (daisy chain configuration only). See Figure 88 on page 84.

Access	Page Address	Register Address	Description
Read/ Write	3'h010	6'h00	**Overvoltage Fault** Overvoltage fault on cells 12 to 1 correspond with bits OF12 to OF1, respectively. Default values are all zero. Bits are set to 1 when faults are detected. The contents of this register can be reset through a register write (14'h0000).

13	12	11	10	9	8	7	6	5	4	3	2	1	0
N/A		OF12	OF11	OF10	OF9	OF8	OF7	OF6	OF5	OF4	OF3	OF2	OF1
0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access	Page Address	Register Address	Description
Read/ Write	3'h010	6'h01	**Undervoltage Fault** Undervoltage fault on cells 12 to 1 correspond with bits UF12 to UF1, respectively. Default values are all zero. Bits are set to 1 when faults are detected. The contents of this register can be reset through a register write (14'h0000).

13	12	11	10	9	8	7	6	5	4	3	2	1	0
N/A		UF12	UF11	UF10	UF9	UF8	UF7	UF6	UF5	UF4	UF3	UF2	UF1
0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access	Page Address	Register Address	Description
Read/ Write	3'h010	6'h02	**Open-Wire Fault** Open Wire fault on Pins VC12 to VC0 correspond with bits OC12 to OC0, respectively. Default values are all zero. Bits are set to 1 when faults are detected. The contents of this register can be reset through a register write (14'h0000).

13	12	11	10	9	8	7	6	5	4	3	2	1	0
N/A	OC12	OC11	OC10	OC9	OC8	OC7	OC6	OC5	OC4	OC3	OC2	OC1	OC0
0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access	Page Address	Register Address	Description (Continued)
Read/ Write	3'h010	6'h03	**Fault Setup** These bits control various Fault configurations. Default values are shown below, as are descriptions of each bit.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
N/A	TST4	TST3	TST2	TST1	TST0	TOT2	TOT1	TOT0	WSCN	SCN3	SCN2	SCN1	SCN0
0	0	0	0	0	1	0	1	1	0	0	0	0	0

SCN0, SCN1, SCN2, SCN3	Scan interval code. Decoded to provide the scan interval setup for the auto scan function. Initialized to 0000 (16ms scan interval). See Table 16 on page 55.
WSCN	Scan Wires timing control (See Table 16 on page 55.) This bit only affects timing in Scan Continuous mode. When this bit is 0 (default), Scan Wires is performed at the same rate as Scan Voltages, except when the SCN3:0 bits select a scan interval of 512 ms or less. In this case Scan Wires is performed every 512 ms. When this bit is 1, Scan Wires is performed at the same rate as Scan Temperatures.
TOT0, TOT1, TOT2	Fault Totalizer code bits. Decoded to provide the required fault totalization. An unbroken sequence of positive fault results equal to the totalize amount is needed to verify a fault condition. Initialized to 011 (8 sample totalizing.) See Table 47 on page 101. This register must be rewritten following an error detection resulting from totalizer overflow.
TST0	Controls temperature testing of internal IC temperature. Set bit to 1 to enable internal temperature test. Set to 0 to disable (not recommended). Initialized to 1 (on).
TST1 to TST4	Controls temperature testing on the external temperature inputs 1 to 4, respectively. Set bit to 1 to enable the corresponding temperature test. Set to 0 to disable. Allows external inputs to be used for general voltage monitoring without imposing a limit value. TST1 to TST4 are initialized to 0 (off).

Access	Page Address	Register Address	Description (Continued)
Read/ Write	3'h010	6'h04	**Fault Status** The $\overline{FAULT}$ logic output is an OR function of the bits in this register: the output is asserted low if any bits in the Fault Status register are set.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
MUX	REG	REF	PAR	OVSS	OV_{BAT}	OW	UV	OV	OT	WDGF	OSC	N/A	
0	0	0	0	0	0	0	0	0	0	0	0	0	0

OSC	Oscillator fault bit. Bit is set in response to a fault on either the 4MHz or 32kHz oscillators. Note that communications functions can be disrupted by a fault in the 4MHz oscillator.
WDGF	Watchdog timeout fault. Bit is set in response to a watchdog timeout.
OT	Over-temperature fault. 'OR' of over-temperature fault bits: TFLT0 to TFLT4. This bit is latched. The bits in the over-temperature fault register must first be reset before this bit can be reset. Reset by writing 14'h0000 to this register.
OV	Overvoltage fault. 'OR' of overvoltage fault bits: OF1 to OF12. This bit is latched. The bits in the Overvoltage Fault register must be reset before this bit can be reset. Reset by writing 14'h0000 to this register.
UV	Undervoltage fault. 'OR' of undervoltage fault bits: UF1 to UF12. This bit is latched. The bits in the Undervoltage Fault register must be reset before this bit can be reset. Reset by writing 14'h0000 to this register.
OW	Open-wire fault. 'OR' of open-wire fault bits: OC0 to OC12. This bit is latched. The bits in the open-wire fault register must be reset before this bit can be reset. Reset by writing 14'h0000 to this register.
OV_{BAT}	Open-wire fault on VBAT connection. Bit set to 1 when a fault is detected. Can be reset through a register write (14'h0000).
OVSS	Open wire fault on VSS connection. Bit set to 1 when a fault is detected. Can be reset through a register write (14'h0000).
PAR	Register checksum (Parity) error. This bit is set in response to a register checksum error. The checksum is calculated and stored in response to a Calc Register Checksum command and acts on the contents of all Page 2 registers. The Check Register Checksum command, see Table 12.4.3 on page 130, is used to repeat the calculation and compare the results to the stored value. The PAR bit is then set if the two results are not equal. This bit is not set in response to a nonvolatile EEPROM memory checksum error.
REF	Voltage reference fault. This bit is set if the voltage reference value is outside its "power-good" range.
REG	Voltage regulator fault. This bit is set if a voltage regulator value (V3P3, VCC or V2P5) is outside its "power-good" range.
MUX	Temperature multiplexer error. This bit is set if the VCC loopback check returns a fault. The VCC loopback check is performed at the end of each temperature scan.

<table>
<tr><th>Access</th><th>Page Address</th><th>Register Address</th><th>Description (Continued)</th></tr>
<tr><td>Read/ Write</td><td>3’h010</td><td>6’h05</td><td>
Cell Setup
Default values are shown below, as are descriptions of each bit.
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>FFSN</td><td>FFSP</td><td>C12</td><td>C11</td><td>C10</td><td>C9</td><td>C8</td><td>C7</td><td>C6</td><td>C5</td><td>C4</td><td>C3</td><td>C2</td><td>C1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
<table>
<tr><td>C1 to C12</td><td>Enable/disable cell overvoltage, undervoltage and open-wire detection on Cell 1 to 12, respectively. Set to 1 to disable OV/UV and open wire tests. Note: Cell voltage readings for disabled cells are not valid, so should be discarded.</td></tr>
<tr><td>FFSP</td><td>Force ADC input to Full Scale Positive. All cell scan readings forced to 14'h1FFF. All temperature scan readings forced to 14'h3FFF.</td></tr>
<tr><td>FFSN</td><td>Force ADC input to Full Scale Negative. All cell scan readings forced to 14'h2000. All temperature scan readings forced to 14'h0000.</td></tr>
</table>
Note: The ADC input functions normally if both FFSN and FFSP are set to '1' but this setting is not supported.
</td></tr>
<tr><td>Read/ Write</td><td>3’h010</td><td>6’h06</td><td>
Over-temperature Fault
Over-temperature fault on Cells 12 to 1 correspond with bits OF12 to OF1, respectively.
Default values are all zero.
Bits are set to 1 when fault are detected.
The contents of this register can be reset through a register write (14’h0000).
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="9">N/A</td><td>TFLT4</td><td>TFLT3</td><td>TFLT2</td><td>TFLT1</td><td>TFLT0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
<table>
<tr><td>TFLT0</td><td>Internal over-temperature fault. Bit set to 1 when a fault is detected. Can be reset through a register write (14’h0000).</td></tr>
<tr><td>TFLT1 - TFLT4</td><td>External over-temperature inputs 1 to 4 (respectively.) Bit set to 1 when a fault is detected. Can be reset through a register write (14’h0000).</td></tr>
</table>
</td></tr>
<tr><td>Read Only</td><td>3’h010</td><td>6’h0F</td><td>Read all Fault and Cell Setup data from locations: 6’h00 - 6’h06. See Figure 88 on page 84.</td></tr>
</table>

12.3.1 Setup Registers

Base Address (Page)	Access	Address Range	Description
3’b010		6’h10 - 6’h1D and 6’h1F	**Device Setup registers** All device setup data.

<table>
<tr><th>Access</th><th>Page Address</th><th>Register Address</th><th>Description</th></tr>
<tr><td>Read/ Write</td><td>3’b010</td><td>6’h10</td><td>
Overvoltage Limit
Overvoltage Limit Value
Overvoltage limit is compared to the measured values for Cells 1 to 12 to test for an Overvoltage condition at any of the cells.
Bit 0 is the LSB, Bit 12 is the MSB. Bit 13 is not used and must be set to 0.
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>N/A</td><td>OV12</td><td>OV11</td><td>OV10</td><td>OV9</td><td>OV8</td><td>OV7</td><td>OV6</td><td>OV5</td><td>OV4</td><td>OV3</td><td>OV2</td><td>OV1</td><td>OV0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Access</th><th>Page Address</th><th>Register Address</th><th>Description (Continued)</th></tr>
<tr><td>Read/ Write</td><td>3’b010</td><td>6’h11</td><td>
Undervoltage Limit
Undervoltage Limit Value
Undervoltage limit is compared to the measured values for Cells 1 to 12 to test for an undervoltage condition at any of the cells.
Bit 0 is the LSB, Bit 12 is the MSB. Bit 13 is not used and must be set to 0.
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>N/A</td><td>UV12</td><td>UV11</td><td>UV10</td><td>UV9</td><td>UV8</td><td>UV7</td><td>UV6</td><td>UV5</td><td>UV4</td><td>UV3</td><td>UV2</td><td>UV1</td><td>UV0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>Read/ Write</td><td>3’b010</td><td>6’h12</td><td>
External Temperature Limit
Over-temperature Limit Value
Over-temperature limit is compared to the measured values for external temperatures 1 to 4 to test for an over-temperature condition at any input. The temperature limit assumes NTC temperature measurement devices (i.e., an over-temperature condition is indicated by a temperature reading below the limit value).
Bit 0 is the LSB, Bit 13 is the MSB.
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>ETL13</td><td>ETL12</td><td>ETL11</td><td>ETL10</td><td>ETL9</td><td>ETL8</td><td>ETL7</td><td>ETL6</td><td>ETL5</td><td>ETL4</td><td>ETL3</td><td>ETL2</td><td>ETL1</td><td>ETL0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>Read/ Write</td><td>3’b010</td><td>6’h13</td><td>
Balance Setup
Default values are shown below, as are descriptions of each bit.
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">N/A</td><td>BEN</td><td>BSP3</td><td>BSP2</td><td>BSP1</td><td>BSP0</td><td>BWT2</td><td>BWT1</td><td>BWT0</td><td>BMD1</td><td>BMD0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
<table>
<tr><td>BMD0, BMD1</td><td>Balance mode. These bits set balance mode.
<table>
<tr><td>BMD1</td><td>BMD0</td><td>Mode</td></tr>
<tr><td>0</td><td>0</td><td>OFF</td></tr>
<tr><td>0</td><td>1</td><td>Manual</td></tr>
<tr><td>1</td><td>0</td><td>Timed</td></tr>
<tr><td>1</td><td>1</td><td>Auto</td></tr>
</table>
</td></tr>
<tr><td>BWT0, BWT1, BWT2</td><td>Balance wait time. Register contents are decoded to provide the required wait time between device balancing. This is to assist with thermal management and is used with the Auto Balance mode. See Table 21 on page 63.</td></tr>
<tr><td>BSP0, BSP1, BSP2, BSP3</td><td>Balance Status register pointer. Points to one of the 13 incidents of the Balance Status register. Balance Status register 0 is used for Manual Balance mode and Timed Balance mode. Balance status registers 1 to 12 are used for Auto Balance mode. Reads and writes to the Balance Status register are accomplished by first configuring the Balance Status register pointer (such as, to read (write) Balance Status register 5, load 0101 to the Balance Status register pointer, then read (write) to the Balance Status register). See Table 21 on page 63.</td></tr>
<tr><td>BEN</td><td>Balance enable. Set to ‘1’ to enable balancing. ‘0’ inhibits balancing. Setting or clearing this bit does not affect any other register contents. Balance Enable and Balance Inhibit commands are provided to allow control of this function without requiring a register write. These commands have the same effect as setting this bit directly. This bit is cleared automatically when balancing is complete and the EOB bit is set (see “Device Setup” on page 127).</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Access</th><th>Page Address</th><th>Register Address</th><th>Description (Continued)</th></tr>
<tr><td>Read/ Write</td><td>3’b010</td><td>6’h14</td><td>
Balance Status
The Balance Status register is a multiple incidence register controlled by the BSP0-4 bits in the Balance setup register. See Table 21 on page 63.
Bit 0 is the LSB, Bit 11 is the MSB.
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">N/A</td><td>BAL12</td><td>BAL11</td><td>BAL10</td><td>BAL8</td><td>BAL8</td><td>BAL7</td><td>BAL6</td><td>BAL5</td><td>BAL4</td><td>BAL3</td><td>BAL2</td><td>BAL1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
<table>
<tr><td>BAL1 to BAL12</td><td>Cell 1 to Cell 12 balance control, respectively. A bit set to 1 enables balance control (turns FET on) of the corresponding cell. Writing this bit enables balance output for the current incidence of the Balance Status register for the cells corresponding to the particular bits, depending on the condition of BEN in the Balance Setup register. Read this bit to determine the current status of each cell’s balance control.</td></tr>
</table>
</td></tr>
<tr><td>Read/ Write</td><td>3’b010</td><td>6’h15</td><td>
Watchdog/Balance Time
Defaults are shown below:
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>BTM6</td><td>BTM5</td><td>BTM4</td><td>BTM3</td><td>BTM2</td><td>BTM1</td><td>BTM0</td><td>WDG6</td><td>WDG5</td><td>WDG4</td><td>WDG3</td><td>WDG2</td><td>WDG1</td><td>WDG0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>
<table>
<tr><td>WDG0 to WDG6</td><td>Watchdog timeout setting. Decoded to provide the time out value for the watchdog function. See “Watchdog Function” on page 105 for details. The watchdog can only be disabled (set to 7’h00) if the watchdog password is set. The watchdog setting can be changed to a nonzero value without writing to the watchdog password. Initialized to 7’h7F (128 minutes).</td></tr>
<tr><td>BTM0 to BTM6</td><td>Balance timeout setting. Decoded to provide the time out value for Timed Balance mode and Auto Balance mode. Initialized to 7’00 (Disabled). See Table 23 on page 65.</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Access</th><th>Page Address</th><th>Register Address</th><th>Description (Continued)</th></tr>
<tr><td>Read/ Write</td><td>3’b010</td><td>6’h16
6’h17</td><td>User Register
28 bits of register space arranged as 2 x 14 bits available for user data. These registers have no effect on the operation of the ISL78600. These registers are included in the register checksum function.</td></tr>
<tr><td>Read Only</td><td>3’b010</td><td>6’h18</td><td>Comms Setup
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">N/A</td><td>CRAT1</td><td>CRAT0</td><td>CSEL2</td><td>CSEL1</td><td>SIZE3</td><td>SIZE2</td><td>SIZE1</td><td>SIZE0</td><td>ADDR3</td><td>ADDR2</td><td>ADDR1</td><td>ADDR0</td></tr>
<tr><td>0</td><td>0</td><td>COMMS RATE 1 pin</td><td>COMMS RATE 0 pin</td><td>COMMS SEL 2 pin</td><td>COMMS SEL 1 pin</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
<table>
<tr><td>ADDR0-ADDR3</td><td>Device Address. The Device Address (device position in the stack) is determined automatically by the device in response to an “Identify” command. The resulting address is stored in ADDR0-3 and is used internally for communications paring and sequencing. The Device Address can be read by the user but not written to.</td></tr>
<tr><td>SIZE0-SIZE3</td><td>Device stack size (top stack device address). Corresponds to the number of devices in the stack. The stack size is determined automatically by the stack devices in response to an “Identify” command. The resulting number is stored in SIZE0-3 and is used internally for communications paring and sequencing. The stack size can be read by the user but not written to.</td></tr>
<tr><td>CSEL1, CSEL2</td><td>Communications setup bits. These bits reflect the state of the COMMS SELECT 1, 2 pins and determine the operating mode of the communications ports. See Table 7 on page 35.</td></tr>
<tr><td>CRAT0, CRAT1</td><td>Communications rate bits. These bits reflect the state of the COMMS RATE 0,1 pins and determine the bit rate of the daisy chain communications system. Table 8 on page 36.</td></tr>
</table></td></tr>
<tr><td>Read/ Write</td><td>3’b010</td><td>6’h19</td><td>Device Setup
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>WP5</td><td>WP4</td><td>WP3</td><td>WP2</td><td>WP1</td><td>WP0</td><td>BDDS</td><td>N/A</td><td>ISCN</td><td>SCAN</td><td>EOB</td><td>N/A</td><td>PIN37</td><td>PIN39</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Pin</td><td>Pin</td></tr>
</table>
<table>
<tr><td>PIN37, PIN39</td><td>These bits indicate the signal level on pin 37 and pin 39 of the device.</td></tr>
<tr><td>EOB</td><td>End Of Balance. This bit is set by the device when balancing is complete. This function is used in the Timed Balance mode and Auto Balance mode. The BEN bit is cleared as a result of this bit being set. Initialized to 1.</td></tr>
<tr><td>SCAN</td><td>Scan Continuous mode. This bit is set in response to a Scan Continuous command and cleared by a Scan Inhibit command.</td></tr>
<tr><td>ISCN</td><td>Set wire scan current source/sink values. Set to 0 for 150µA. Set to 1 for 1mA.</td></tr>
<tr><td>BDDS</td><td>Balance condition during measurement. Controls the balance condition in Scan Continuous mode and Auto Balance mode. Set to 1 to have balancing functions turned off 10ms prior to and during cell voltage measurement. Set to 0 for normal operation (balancing functions not affected by measurement).</td></tr>
<tr><td>WP5:0</td><td>Watchdog disable password. These bits must be set to 6’h3A (111010) before the watchdog can be disabled. Disable watchdog by writing 7’h00 to the watchdog bits.</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Access</th><th>Page Address</th><th>Register Address</th><th>Description (Continued)</th></tr>
<tr><td rowspan="5">Read Only Value set in EEPROM</td><td rowspan="5">3’b010</td><td rowspan="5">6’h1A</td><td>Internal Temperature Limit
Bit 0 is the LSB, Bit 13 is the MSB.
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>ITL13</td><td>ITL12</td><td>ITL11</td><td>ITL10</td><td>ITL9</td><td>ITL8</td><td>ITL7</td><td>ITL6</td><td>ITL5</td><td>ITL4</td><td>ITL3</td><td>ITL2</td><td>ITL1</td><td>ITL0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>ITL1 to ITL12</td><td>IC over-temperature limit value. Over-temperature limit is compared to the measured values for internal IC temperature to test for an over-temperature condition. The internal temperature limit value is stored in nonvolatile memory during test and loaded to these register bits at power up. The register contents can be read by the user but not written to.</td></tr>
<tr><td>Read Only</td><td>3’b010</td><td>6’h1B
6’h1C</td><td>Serial Number
The 28b serial number programmed in nonvolatile memory during factory test is mirrored to these 2 x 14 bit registers. The serial number can be read at any time but can not be written.</td></tr>
<tr><td rowspan="3">Read Only Value set in EEPROM</td><td rowspan="3">3’b010</td><td rowspan="3">6’h1D</td><td>Trim Voltages
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>TV5</td><td>TV4</td><td>TV3</td><td>TV2</td><td>TV1</td><td>TV0</td><td colspan="8">N/A</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td colspan="8">Ignore the contents of these bits</td></tr>
</table></td></tr>
<tr><td>TV5:0</td><td>Trim voltage (VNOM). The nominal cell voltage is programmed to nonvolatile memory during test and loaded to the Trim Voltage register at power up. The VNOM value is a 6-bit representation of the 0V to 5V cell voltage input range with 50_{10} (6’h32) representing 5V. By default the trim value is 6’h21, which translates to 33 decimal, or 3.3V. The parts are additionally marked with the trim voltage by the addition of a two digit code to the part number such as, 3.3V is denoted by the code 33.</td></tr>
<tr><td>Read Only</td><td>3’h010</td><td>6’h1F</td><td colspan="2">Read all Setup data from locations: 6’h10 - 6’h1D. See Figure 88 on page 84.</td></tr>
</table>

12.3.2 Cell Balance Registers

Base Address (Page)	Access	Address Range	Description
3’b010	Read/ Write	6’h20 - 6’h37	**Cell balance registers** These registers are loaded with data related to change in SOC desired for each cell. This data is then used during Auto Balance mode. The data value is decremented with each successive ADC sample until a zero value is reached. The register space is arranged as 2 x 14-bit per cell for 24 x 14-bit total. The registers are cleared at device power up or by a Reset command. See “Auto Balance Mode” on page 65.

Access	Page Address	Register Address	Description
Read/ Write	3’b010	6’h20	Cell 1 balance value Bits 0 to 13.
		6’h21	Cell 1 balance value Bits 14 to 27.
		~	
		6’h36	Cell 12 balance value Bits 0 to 13.
		6’h37	Cell 12 balance value Bits 14 to 27.

12.4 Reference Coefficient Registers

12.4.1

Base Address (Page)	Access	Address Range	Description
3'b010	Read Only	6'h38 - 6'h3A	**Reference Coefficients** Bit 13 is the MSB, Bit 0 is the LSB

Access	Page Address	Register Address	Description
Read Only Value set in EEPROM	3'b010	6'h38	**Reference Coefficient C** Reference calibration coefficient C LSB. Use with coefficients A and B and the measured reference value to obtain the compensated reference measurement. This result can be compared to limits given in parameter "V_{RACC}" in the "Voltage Reference/Oscillator Check Specifications" on page 16 to check that the reference is within limits. The register contents can be read by the user but not written to.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RCC13	RCC12	RCC11	RCC10	RCC9	RCC8	RCC7	RCC6	RCC5	RCC4	RCC3	RCC2	RCC1	RCC0
NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV

Access	Page Address	Register Address	Description
Read Only	3'b010	6'h39	**Reference Coefficient B** Reference calibration coefficient B LSB. Use with coefficients A and C and the measured reference value to obtain the compensated reference measurement. This result can be compared to limits given in parameter "V_{RACC}" in the "Voltage Reference/Oscillator Check Specifications" on page 16 to check that the reference is within limits. The register contents can be read by the user but not written to.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RCB13	RCB12	RCB11	RCB10	RCB9	RCB8	RCB7	RCB6	RCB5	RCB4	RCB3	RCB2	RCB1	RCB0
NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV

Access	Page Address	Register Address	Description
Read Only	3'b010	6'h3A	**Reference Coefficient A** Reference calibration coefficient A LSB. Use with coefficients B and C and the measured reference value to obtain the compensated reference measurement. This result can be compared to limits given in parameter "V_{RACC}" in the "Voltage Reference/Oscillator Check Specifications" on page 16 to check that the reference is within limits. The register contents can be read by the user but not written to.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RCA8	RCA7	RCA6	RCA5	RCA4	RCA3	RCA2	RCA1	RCA0	N/A				
NV	NV	NV	NV	NV	NV	NV	NV	NV	Ignore the content of these bits				

12.4.2 Cells In Balance Register

Base Address (Page)	Access	Address Range	Description
3'b010	Read Only	6'h3B	**Cells In Balance**

Access	Page Address	Register Address	Description
Read Only	3'b010	6'h3B	**Cells Balance Enabled (Valid for non-daisy chain configuration only)** This register reports the current condition of the cell balance outputs. Bit 0 is the LSB, Bit 11 is the MSB.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
N/A		CBEN12	CBEN11	CBEN10	CBEN8	CBEN8	CBEN7	CBEN6	CBEN5	CBEN4	CBEN3	CBEN2	CBEN1
0	0	0	0	0	0	0	0	0	0	0	0	0	0

CBEN1 to CBEN12	Indicates the current balancing status of Cell 1 to Cell 12 (respectively). "1" indicates balancing is enabled for this cell. "0" indicates that balancing is turned off.

12.4.3 Device Commands

Base Address (Page)	Access	Address Range	Description
3'b011	Read Only	6'h01 - 6'h14	**Device commands.** Actions and communications administration. Not physical registers but memory mapped device commands. Commands from host and device responses are all configured as reads (BASE ADDR MSB = 0). Write operations breaks the communication rules and produce NAK from the target device.

Page Address	Register Address	Description
3'b011	6'h01	**Scan Voltages.** Device responds by scanning V_{BAT} and all 12 cell voltages and storing the results in local memory.
	6'h02	**Scan Temperatures.** Device responds by scanning external temperature inputs, internal temperature, and the secondary voltage reference, and storing the results in local memory.
	6'h03	**Scan Mixed.** Device responds by scanning V_{BAT}, cell and ExT1 voltages and storing the results in local memory. The ExT1 measurement is performed in the middle of the cell voltage scans to minimize measurement latency between the cell voltages and the voltage on ExT1.
	6'h04	**Scan Wires.** Device responds by scanning for pin connection faults and stores the results in local memory.
	6'h05	**Scan All.** Device responds by performing the functions of the Scan Voltages, Scan Temperatures, and Scan Wires commands in sequence. Results are stored in local memory.
	6'h06	**Scan Continuous.** Places the device in Scan Continuous mode by setting the Device Setup register SCAN bit.
	6'h07	**Scan Inhibit.** Stops Scan Continuous mode by clearing the Device Setup register SCAN bit.
	6'h08	**Measure.** Device responds by measuring a targeted single parameter (cell voltage/V_{BAT}/external or internal temperatures or secondary voltage reference).
	6'h09	**Identify.** Special mode function used to determine device stack position and address. Devices record their own Device Address and the total number of devices in the stack. See "Identify Command" on page 69 for details.
	6'h0A	**Sleep.** Places the part in Sleep mode (wakeup through daisy comms). See "Communication Timing" on page 84.

Page Address	Register Address	Description
	6'h0B	**NAK.** Device response if communications is not recognized. The device responds NAK down the daisy chain to the host microcontroller. The host microcontroller typically retransmits on receiving a NAK.
	6'h0C	**ACK.** Used by host microcontroller to verify communications without changing anything. Devices respond with ACK.
	6'h0E	**Communications Failure.** Used in daisy chain implementations to communicate Communications Failure. If a communication is not acknowledged by a stack device, the last stack device that did receive the communication responds with Communications Failure. This is part of the communications integrity checking. Devices downstream of a communications fault are alerted to the fault condition by the watchdog function.
	6'h0F	**Wakeup.** Used in daisy chain implementations to wake up a sleeping stack of devices. The Wakeup command is sent to the Bottom stack device (Master device) through SPI. The Master device then wakes up the rest of the stack by transmitting a low frequency clock. The Top stack device responds ACK when it is awake. See "Wakeup Command" on page 60.
	6'h10	**Balance Enable.** Enables cell balancing by setting BEN. Can be used to enable cell balancing on all devices simultaneously using the "Address All" address 1111.
	6'h11	**Balance Inhibit.** Disables cell balancing by clearing BEN. Can be used to disable cell balancing on all devices simultaneously using the "Address All" address 1111.
	6'h12	**Reset.** Resets all digital registers to its power-up state (i.e., reloads the factory programmed configuration data from non-volatile memory. Stops all scan and balancing activity. Daisy chain devices must be reset in sequence starting with the Top stack device and proceeding down the stack to the Bottom (Master) device. The Reset command must be followed by an Identify command (daisy chain configuration) before volatile registers can be re-written.
	6'h13	**Calculate register checksum.** Calculates the checksum value for the current Page 2 register contents (registers with base address 0010). See "System Hardware Connection" on page 29.
	6'h14	**Check register checksum.** Verifies the register contents are correct for the current checksum. An incorrect result sets the PAR bit in the Fault status register which starts a standard fault response. See "System Hardware Connection" on page 29.

12.5 Nonvolatile Memory (EEPROM) Checksum

A checksum is provided to verify the contents of EEPROM memory. Two registers are provided. The MISR register (below) contains the correct checksum value, which is calculated during factory testing. The MISR Shadow register contains the checksum value that is calculated each time the nonvolatile memory is loaded to shadow registers, either after a power cycle or after a device receives a Reset command. See "Fault Diagnostics" on page 107.

Base Address (Page)	Access	Address Range	Description
100	Read Only	6'h3F	Nonvolatile memory Multiple Input Shift Register (MISR) register. This checksum value for the nonvolatile memory contents. It is programmed during factory testing.
101	Read Only	6'h00	MISR shadow register checksum value. This value is calculated when shadow registers are loaded from nonvolatile memory either after a power cycle or a software reset.

13. Register Map

R/W + Page		Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	Write					Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0001		000000	V_{BAT} Voltage	VB7	VB6	VB5	VB4	VB3	VB2	VB1	VB0
						VB13	VB12	VB11	VB10	VB9	VB8
0001		000001	Cell 1 Voltage	C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
						C1V13	C1V12	C1V11	C1V10	C1V9	C1V8
0001		000010	Cell 2 Voltage	C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
						C2V13	C2V12	C2V11	C2V10	C2V9	C2V8
0001		000011	Cell 3 Voltage	C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
						C3V13	C3V12	C3V11	C3V10	C3V9	C3V8
0001		000100	Cell 4 Voltage	C4V7	C4V6	C4V5	C4V4	C4V3	C4V2	C4V1	C4V0
						C4V13	C4V12	C4V11	C4V10	C4V9	C4V8
0001		000101	Cell 5 Voltage	C5V7	C5V6	C5V5	C5V4	C5V3	C5V2	C5V1	C5V0
						C5V13	C5V12	C5V11	C5V10	C5V9	C5V8
0001		000110	Cell 6 Voltage	C6V7	C6V6	C6V5	C6V4	C6V3	C6V2	C6V1	C6V0
						C6V13	C6V12	C6V11	C6V10	C6V9	C6V8
0001		000111	Cell 7 Voltage	C7V7	C7V6	C7V5	C7V4	C7V3	C7V2	C7V1	C7V0
						C7V13	C7V12	C7V11	C7V10	C7V9	C7V8
0001		001000	Cell 8 Voltage	C8V7	C8V6	C8V5	C8V4	C8V3	C8V2	C8V1	C8V0
						C8V13	C8V12	C8V11	C8V10	C8V9	C8V8
0001		001001	Cell 9 Voltage	C9V7	C9V6	C9V5	C9V4	C9V3	C9V2	C9V1	C9V0
						C9V13	C9V12	C9V11	C9V10	C9V9	C9V8
0001		001010	Cell 10 Voltage	C10V7	C10V6	C10V5	C10V4	C10V3	C10V2	C10V1	C10V0
						C10V13	C10V12	C10V11	C10V10	C10V9	C10V8
0001		001011	Cell 11 Voltage	C11V7	C11V6	C11V5	C11V4	C11V3	C11V2	C11V1	C11V0
						C11V13	C11V12	C11V11	C11V10	C11V9	C11V8
0001		001100	Cell 12 Voltage	C12V7	C12V6	C12V5	C12V4	C12V3	C12V2	C12V1	C12V0
						C12V13	C12V12	C12V11	C12V10	C12V9	C12V8
0001		001111	All Cell Voltage Data	Daisy chain configuration only. This command returns all Page 1 data from address 6'h00 through 6'h0C in a single data stream. See ""Response Timing Tables" on page 96 and "System Out of Limit Detection" on page 94. See example in Figure 88 on page 84.							
0001		010000	IC Temperature	ICT7	ICT6	ICT5	ICT4	ICT3	ICT2	ICT1	ICT0
						ICT13	ICT12	ICT11	ICT10	ICT9	ICT8
0001		010001	External Temperature 1 Input Voltage (ExT1 pin)	ET1V7	ET1V6	ET1V5	ET1V4	ET1V3	ET1V2	ET1V1	ET1V0
						ET1V13	ET1V12	ET1V11	ET1V10	ET1V9	ET1V8
0001		010010	External Temperature 2 Input Voltage (ExT2 pin)	ET2V7	ET2V6	ET2V5	ET2V4	ET2V3	ET2V2	ET2V1	ET2V0
						ET2V13	ET2V12	ET2V11	ET2V10	ET2V9	ET2V8
0001		010011	External Temperature 3 Input Voltage (ExT3 pin)	ET3V7	ET3V6	ET3V5	ET3V4	ET3V3	ET3V2	ET3V1	ET3V0
						ET3V13	ET3V12	ET3V11	ET3V10	ET3V9	ET3V8
0001		010100	External Temperature 4 Input Voltage (ExT4 pin)	ET4V7	ET4V6	ET4V5	ET4V4	ET4V3	ET4V2	ET4V1	ET4V0
						ET4V13	ET4V12	ET4V11	ET4V10	ET4V9	ET4V8

R/W + Page		Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	Write					Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0001		010101	Secondary Reference Voltage	RV7	RV6	RV5	RV4	RV3	RV2	RV1	RV0
						RV13	RV12	RV11	RV10	RV9	RV8
0001		010110	Scan Count					SCN3	SCN2	SCN1	SCN0
0001		011111	All Temperature Data	Daisy chain configuration only. This command returns all Page 1 data from address 6'h10 through 6'h16 in a single data stream. See ""Response Timing Tables" on page 96 and "System Out of Limit Detection" on page 94. See example in Figure 88 on page 84.							
0010	1010	000000	Overvoltage Fault	OF8	OF7	OF6	OF5	OF4	OF3	OF2	OF1
								OF12	OF11	OF10	OF9
0010	1010	000001	Undervoltage Fault	UF8	UF7	UF6	UF5	UF4	UF3	UF2	UF1
								UF12	UF11	UF10	UF9
0010	1010	000010	Open-Wire Fault	OC7	OC6	OC5	OC4	OC3	OC2	OC1	OC0
							OC12	OC11	OC10	OC9	OC8
0010	1010	000011	Fault Setup	TOT2	TOT1	TOT0	WSCN	SCN3	SCN2	SCN1	SCN0
							TTST4	TTST3	TTST2	TTST1	TTST0
0010	1010	000100	Fault Status	OW	UV	OV	OT	WDGF	OSC	0	0
						MUX	REG	REF	PAR	OVSS	OV_{BAT}
0010	1010	000101	Cell Setup	C8	C7	C6	C5	C4	C3	C2	C1
						FFSN	FFSP	C12	C11	C10	C9
0010	1010	000110	Over-Temperature Fault				TFLT4	TFLT3	TFLT2	TFLT1	TFLT0
0010		001111	All Fault Data	Daisy chain configuration only. This command returns all Page 2 data from address 6'h00 through 6'h06 in a single data stream. See ""Response Timing Tables" on page 96 and "System Out of Limit Detection" on page 94. See example in Figure 88 on page 84.							
0010	1010	010000	Overvoltage Limit	OV7	OV6	OV5	OV4	OV3	OV2	OV1	OV0
						OV13	OV12	OV11	OV10	OV9	OV8
0010	1010	010001	Undervoltage Limit	UV7	UV6	UV5	UV4	UV3	UV2	UV1	UV0
						UV13	UV12	UV11	UV10	UV9	UV8
0010	1010	010010	External Temp Limit	ETL7	ETL6	ETL5	ETL4	ETL3	ETL2	ETL1	ETL0
						ETL13	ETL12	ETL11	ETL10	ETL9	ETL8
0010	1010	010011	Balance Setup	BSP2	BSP1	BSP0	BWT2	BWT1	BWT0	BMD1	BMD0
										BEN	BSP3
0010	1010	010100	Balance Status (Cells to Balance)	BAL8	BAL7	BAL6	BAL5	BAL4	BAL3	BAL2	BAL1
								BAL12	BAL11	BAL10	BAL9
0010	1010	010101	Watchdog/Balance Time	BTM0	WDG6	WDG5	WDG4	WDG3	WDG2	WDG1	WDG0
						BTM6	BTM5	BTM4	BTM3	BTM2	BTM1
0010	1010	010110	User Register	UR7	UR6	UR5	UR4	UR3	UR2	UR1	UR0
						UR13	UR12	UR11	UR10	UR9	UR8
0010	1010	010111	User Register	UR21	UR20	UR19	UR18	UR17	UR16	UR15	UR14
						UR27	UR26	UR25	UR24	UR23	UR22

R/W + Page				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	Write	Address	Register Name			Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0010		011000	Comms Setup	SIZE3	SIZE2	SIZE1	SIZE0	ADDR3	ADDR2	ADDR1	ADDR0
								CRAT1	CRAT0	CSEL2	CSEL1
0010	1010	011001	Device Setup	BDDS	0	ISCN	SCAN	EOB	0	Pin 37	Pin 39
						WP5	WP4	WP3	WP2	WP1	WP0
0010		011010	Internal Temp Limit	ITL7	ITL6	ITL5	ITL4	ITL3	ITL2	ITL1	ITL0
						ITL13	ITL12	ITL11	ITL10	ITL9	ITL8
0010		011011	Serial Number 0	SN7	SN6	SN5	SN4	SN3	SN2	SN1	SN0
						SN13	SN12	SN11	SN10	SN9	SN8
0010		011100	Serial Number 1	SN21	SN20	SN19	SN18	SN17	SN16	SN15	SN14
						SN27	SN26	SN25	SN24	SN23	SN22
0010		011101	Trim Voltage	N/A							
						TV5	TV4	TV3	TV2	TV1	TV0
0010		011111	All Setup Data	Daisy chain configuration only. This command returns all Page 2 data from address 6'h10 through 6'h1D in a single data stream. See ""Response Timing Tables" on page 96 and "System Out of Limit Detection" on page 94. See example in Figure 88 on page 84.							
0010	1010	100000	Cell 1 Balance Value 0	B0107	B0106	B0105	B0104	B0103	B0102	B0101	B0100
						B0113	B0112	B1011	B0110	B0109	B0108
0010	1010	100001	Cell 1 Balance Value 1	B0121	B0120	B0119	B0118	B0117	B0116	B0115	B0114
						B0127	B0126	B0125	B0124	B0123	B0122
0010	1010	100010	Cell 2 Balance Value 0	B0207	B0206	B0205	B0204	B0203	B0202	B0201	B0200
						B0213	B0212	B1011	B0210	B0209	B0208
0010	1010	100011	Cell 2 Balance Value 1	B0221	B0220	B0219	B0218	B0217	B0216	B0215	B0214
						B0227	B0226	B0225	B0224	B0223	B0222
		~	~	~							
0010	1010	110111	Cell 12 Balance Value 1	B1221	B1220	B1219	B1218	B1217	B1216	B1215	B1214
						B1227	B1226	B1225	B1224	B1223	B1222
0010		111000	Reference Coefficient C	RCC7	RCC6	RCC5	RCC4	RCC3	RCC2	RCC1	RCC0
						RCC13	RCC12	RCC11	RCC10	RCC9	RCC8
0010		111001	Reference Coefficient B	RCB7	RCB6	RCB5	RCB4	RCB3	RCB2	RCB1	RCB0
						RCB13	RCB12	RCB11	RCB10	RCB9	RCB8
0010		111010	Reference Coefficient A	RCA2	RCA1	RCA0	N/A				
						RCA8	RCA7	RCA6	RCA5	RCA4	RCA3
0010		111011	Cell Balance Enabled Valid in Stand-Alone Only. Register read responds NAK otherwise.)	CBEN8	CBEN7	CBEN6	CBEN5	CBEN4	CBEN3	BAL2	CBEN1
								CBEN12	CBEN11	CBEN10	CBEN9
0011		000001	Scan Voltages								
0011		000010	Scan Temperatures								
0011		000011	Scan Mixed								
0011		000100	Scan Wires								
0011		000101	Scan All								
0011		000110	Scan Continuous								

R/W + Page		Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	Write					Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0011		000111	Scan Inhibit								
0011		001000	Measure								
0011		001001	Identify								
0011		001010	Sleep								
0011		001011	NAK								
0011		001100	ACK								
0011		001110	Communications Failure								
0011		001111	Wakeup								
0011		010000	Balance Enable								
0011		010001	Balance Inhibit								
0011		010010	Reset								
0011		010011	Calc Register Checksum								
0011		010100	Check Register Checksum								

0100		111111	EEPROM MISR Data Register	14-bit MISR EEPROM checksum value. Programmed during test.
0101		000000	MISR Calculated Checksum	14-bit shadow register MISR checksum value. Calculated when shadow registers are loaded from nonvolatile memory

14. Revision History

Revision	Date	Change
11.00	Jun.12.20	Applied new formatting throughout. Updated minimum and maximum ISL78600 Initial Cell Monitor Voltage Error specification values. Updated Performance Characteristics and Typical Performance Curves sections. Updated Communications Failure table Table 48 on page 103 and description. Clarified use of the term reset to be Software Reset and Hardware reset and updated the response to both actions. Changed description of Identify, adding additional diagrams and text. Changed default values for WSCN, TST0 and TST1 in Register table. Changed the description of the WSCN bit. Updated Table 15 on page 52 and associated text to match device operation. Made minor changes to text in multiple locations to clarify device operation. Removed the capacitor from VDDEXT to Ground in Figure 45 on page 34. Moved 10k (R1) resistor in Figure 50 on page 39 and changed Table 12 on page 39 to match. Updated Long Term Drift chart, Figure 37 on page 26. Updated Figure 95 on page 92 to show more detail and changed text associated with figure. Corrected t1A equation in Figure 91 on page 87 (missing parentheses). Changed t2 equation in Figure 92 on page 88 Corrected definition of t_{CS} in Figure 93 on page 89 and Figure 94 on page 90. Correction to Figure 89 on page 85. Corrected DIN/DOUT references on various figures to always refer to ISL78600 signals. Updated timing values in Table 40 on page 96 through Table 45 on page 99. Table 15 on page 52. Added Note 15 and corrected other note references in table. Section , “Cell Setup,” on page 124: Added the following text to C1 to C12, “Note: Cell voltage readings for disabled cells are not valid, so should be discarded.” Added Daisy Chain Transmit Buffer section. Added Note to Section 5.10, “Scan Inhibit Command,” on page 56.
10.00	Apr.12.18	Updated the Ordering Information table (removed Note 4). Changed the following Abs Max values from 4.1V to 5.5V (BASE, DIN, SCLK, $\overline{CS}$, DOUT, $\overline{DATA\ READY}$, COMMS SELECT n, TEMPREG, REF, V3P3, VCC, $\overline{FAULT}$, COMMS RATE n, EN, VDDEXT). Updated Figure 41 and Figure 42 on page 31, Figure 43 and Figure 44 on page 32, Figure 51 on page 41, Figure 55 on page 45, and Figure 56 on page 46 to reflect new recommended input filter circuits. Added Table 3 on page 31 and Table 4 on page 33 and updated Table 13 on page 48. Added a paragraph in the Daisy Chain Circuits section page 37 that discusses board capacitance effect on capacitor selection and changed Table 10 on page 38 and Table 11 on page 38 to match. Re-arranged the specifications for ΔV_{CELL} to group like voltage ranges. Re-arranged the specifications for VCELL/VBAT board level accuracy Table (page 20). Added Board Level accuracy table for various cell chemistry voltages (page 21) Updated Figure 45 and added Table 6 (No actual changes to content). Updated Figure 48 and Table 10 (No actual changes to content). Updated Figure 49 and Table 11 (No actual changes to content). Updated Figure 50 and Table 12 (No actual changes to content). Removed About Intersil section and updated the disclaimer.
9.00	May.23.17	Added Section “Daisy Chain Receive Buffer” on page 74. Added Figure 75 on page 79 and text to clarify Buffer over-flow. In Figures 70 to 72 and Figure 77, removed a 30us time reference between CS and first SPI clock.
8.00	Feb.10.17	Clarified that “Cells in Balance” register is available only during Stand-Alone operation (page 68, page 130, and page 134). Clarified that Scan Continuous functions during Manual, Timed, and Auto Balance modes (page 54 and page 68). Clarified that the “BDDS” bit function in Timed and Auto Balance modes (page 68). Clarified the calculation of internal and external temperature values (page 118). Updated POD Q64.10x10D from rev 2 to rev 3. Changes: Added land pattern back in (as in rev 1), but removed the exposed pad.

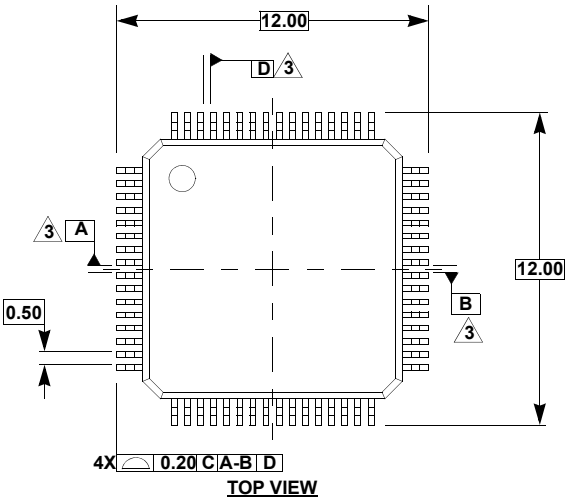
Revision	Date	Change
7.00	Apr.12.16	Added AEC-Q100 to Features on page 1. Updated Ordering Information table on page 7 by adding Tape and Reel option in note and removing evaluation board FG until release. Added Table 1 on page 7. Added table "Performance Characteristics" on page 20. Pages 17-22: Updated Performance Curves. "Absolute Maximum Ratings" on page 10 Updated ESD Ratings testing information from JESD to AEC-Q100 and changed CDM from 500V to 2kV. Changed Thermal Information Tja from "49" to "42" and updated pb-free reflow profile to standard Pages 7-13: Changed selected electrical specifications as follows: Page 7: Changed Abs Max specs for the BASE pin changes from 4.1V to 5.5V. Page 8: Changed I_{VBAT} and $I_{VBATSHDN}$ Typical and Max Current specifications. Page 8: Updated $I_{VBATSHDN}$ Minimum Current specifications. Page 10: Deleted ΔV_{BAT} for 31.2V to 59.4V and changed Min and Max for two other voltage ranges. Page 13: Deleted $t_{DR:ST}$ parameter (not valid in system timing.) Page 13: Changed $t_{DR:SP}$ and $t_{DR:WAIT}$ to typical values (timing is dependent on system variations.) Removed Note 8 which read "Scan and Measurement start times..." from Electrical Spec Table due to not being referenced. Page 15: Removed $t_{DR:ST}$ from Figure 4. Updated graphics (Figures 51 through 57) to Intersil standards. Page 63: Changed the equation for calculating Pack voltage. Changed the heading from "Communication Timing Tables" to "System Timing Tables" on page 91.
6.00	Jan.20.15	Changed ground references in Application Diagram on Page 1. Figure 4B, page 16: Deleted the word "Maximum" from the caption. Page 7 - Capacitive Discharge Model: Changed 750V to 500V. Removed Machine Model specification. "Recommended Operating Conditions" on page 11, changed Recommended Operating Conditions for ExT1, ExT2, ExT3, ExT4 from 3.6V to 2.5V and removed outputs $\overline{FAULT}$, BASE, DOUT, $\overline{DATA\ READY}$, TEMPREG and VREF. Added to "BASE" Pin Description on page 8, "Do not let this pin float." Some changes to Electrical Specifications, pages 9-13. On page 11, "V2P5 Power Good Window", Changed V2PH Min from 2.55 to 2.62 and Max from 2.9 to 2.766V. For the -40°C to 105°C line, change V2PH Min from 2.55 to 2.616 and Max from 2.9 to 2.77. Table 17 on page 57, Changed "Cell0 Voltage" to "VBAT Voltage". "CRC Calculation" on page 80: Added example software CRC calculation code. Added note: "A Reset command should be issued following a "hard reset" in which the EN pin is toggled." to "Reset Command" on page 60. "Fault Diagnostics" on page 107 changed to add the comment, "When a fault is detected, the [TOT2:0] bits should be re-written." Table on page 109, Read checksum value calculated by ISL78600changed "cycling the EN pin or the host issuing a Reset command." to "cycling the EN pin followed by a host initiated Reset command, or simply the host issuing a Reset command." Section, "Register Descriptions," on page 113: Changed "VC0 Voltage" to "VBAT Voltage" and added voltage calculation equations. Changed Section, "System Hardware Connection," on page 27. Changed "when the EN pin is low" to "when the EN pin is toggled and the device receives a Reset Command". "Fault Setup" on page 122 description for TOT bits: Added the comment, "This register must be re-written following an error detection resulting from Totalizer overflow." Added Note to Figure 72 indicating max CS to SCK timing on SPI Read Added to Description in Section, "Power Supplies and Reference," on page 31, "The external pass transistor is required. Do not allow this pin to float." Moved Note 10: "Biasing setup as in Figure 45 on page 34 or equivalent" to Electrical Table heading. Changed all pin name references to all caps.
5.00	Feb.26.14	Changed Note on page 137 From: Initial accuracy does not include drift due to solder or heat effect. To: Stresses may be induced in the ISL78600 during soldering or other high temperature events that affect measurement accuracy. Initial accuracy does not include effects due to this. See Figure 6 for cell reading accuracy obtained after soldering to Intersil evaluation boards. When soldering the ISL78600 to a customized circuit board with a layout or construction significantly differing from the Intersil evaluation board, design verification tests should be applied to determine drift due to soldering and over life time.

Revision	Date	Change
4.00	Oct.25.13	Updated bullet in Features AEC - Q100 Qualified to Qualified for Automotive applications. Updated in Disclaimer Intersil products to Intersil Automotive Qualified Products and ISO9000 to TS16949. Page 18 - removed “Note: Boards baked at +105°C for 12 hours to accelerate recovery from soldering” from Figure 4B.
3.00	Sep.26.13	Open Wire Current ISCN bit = 0 on page 16 changed MAX from 0.175 to 0.185 Updated Electrical Spec Table by adding/modifying Note, T_{JA} Spec, and ΔVCELL, VRACC, IVCELL, ICBSD Specs. Added Typical Performance Curve: Maximum Cell Reading Error from 114 Evaluations Boards At 3.3V, +25°C. Histogram Updated Definitions for Shutdown Mode in “Alarm Response” on page 106 and “Reset Command” on page 60. Page 35: Table 10, Updated recommendation for C1 Replaced “Measurement and Communication Timing” Section (pages 51 to 58 of previous document) with new sections “Communication Timing” on page 84 and “System Timing Tables” on page 91 with new figures and tables to offer more clarity and flexibility in communication and measurement timing calculations.
2.00	Nov.30.12	Removed “BASE” from “Recommended Operating Conditions” on page 11. Page 60, Updated Tables 42 and 43. “Setup Registers” on page 124, changed “Enable/disable cell overvoltage and undervoltage detection on cell 1 to 12, respectively. Set to 1 to disable OV/UV test” to “Enable/disable cell overvoltage, undervoltage and open wire detection on cell 1 to 12, respectively. Set to 1 to disable OV/UV and open wire tests”. Page 32- page 38: Modified and simplified typical application circuits to reflect single RC filters for cell inputs and Ext Temp inputs, as well as the BOM list. Figure 47 on page 36: Modified connections for cell balancing pins with 10 cells Page 80 - page 81: Removed information regarding “ISL78600 Supplied through an external regulated 3.3V Supply”. Page 81: Removed comments: regarding an optional zener diode. Table 10 on page 38: modified C2 values Figure 50 on page 39: Simplified and removed RC filters for Ext Temp inputs 1-4, as well as the BOM list in Table 54.
1.00	Sep.27.12	Initial Release.

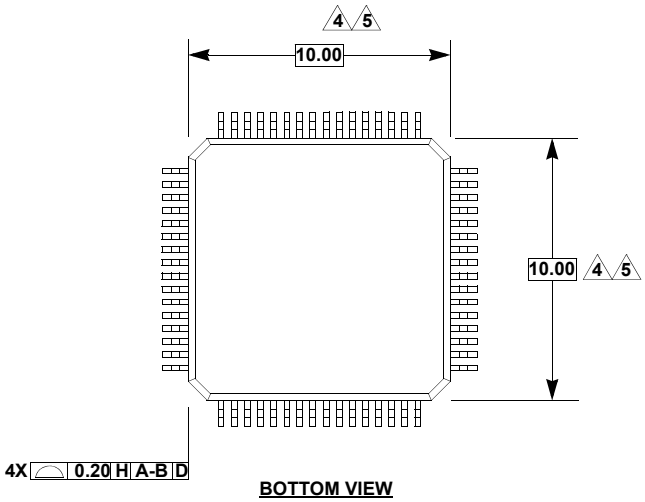
15. Package Outline Drawing

For the most recent package outline drawing, see Q64.10x10D.

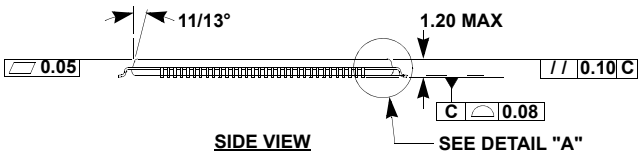
Q64.10x10D
64 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE
Rev 3, 11/16



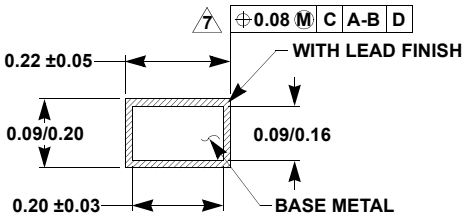
TOP VIEW

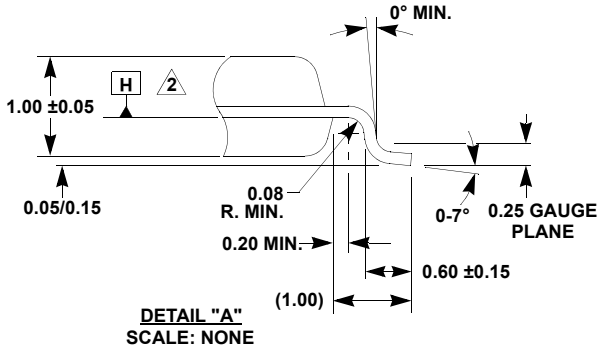


BOTTOM VIEW

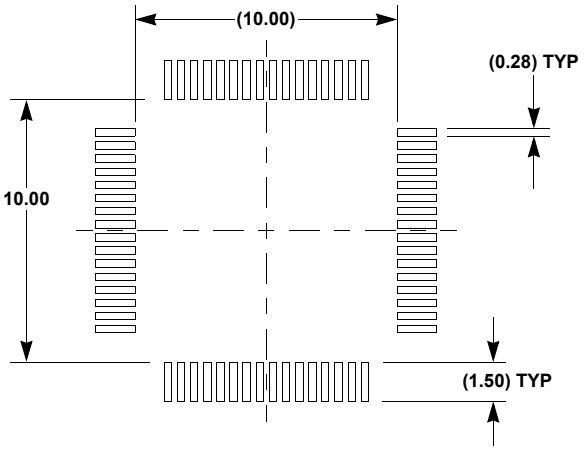


SIDE VIEW





DETAIL "A"
SCALE: NONE



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. All dimensioning and tolerancing conform to ANSI Y14.5-1982.
2. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and D to be determined at centerline between leads where leads exit plastic body at datum plane H.
4. Dimensions do not include mold protrusion. Allowable mold protrusion is 0.254mm.
5. These dimensions to be determined at datum plane H.
6. Package top dimensions are smaller than bottom dimensions and top of package does not overhang bottom of package.
7. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total at maximum material condition. Dambar cannot be located on the lower radius or the foot.
8. Controlling dimension: millimeter.
9. This outline conforms to JEDEC publication 95 registration MS-026, variation ACD.
10. Dimensions in ( ) are for reference only.

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