19-3564; Rev 0; 1/05

EVALUATION KIT AVAILABLE

µPMIC for Microprocessors or DSPs in Portable Equipment

MAX8620Y

General Description

The MAX8620Y micro-power-management integrated circuit (µPMIC) powers low-voltage microprocessors or DSPs in portable devices. The µPMIC includes a high-efficiency step-down DC-DC converter, two low-dropout linear regulators (LDOs), a microprocessor reset output, and power-on/off control logic. This device maintains high efficiency at light loads with a low 115µA supply current, and its miniature TDFN package makes it ideal for portable devices.

The MAX8620Y's step-down DC-DC converter utilizes a proprietary 4MHz hysteretic-PWM control scheme that allows for ultra-small external components. Internal synchronous rectification improves efficiency and eliminates the external Schottky diode that is required in conventional step-down converters. The output voltage is adjustable from 0.6V to 3.3V, with guaranteed output current up to 500mA.

The MAX8620Y's two LDOs offer low 45µV_{RMS} output noise and a low dropout of only 200mV at 200mA. Each LDO delivers at least 300mA of continuous output current. The output voltages are pin selectable from 1.8V to 3.3V for flexibility.

A microprocessor reset output ($\overline{RESET}$) monitors OUT1 and warns the system of impending power loss allowing safe shutdown. $\overline{RESET}$ asserts during power-up, power-down, shutdown, and fault conditions where V_{OUT1} is below its regulation voltage.

Applications

Cellular Handsets

Smart Phones/PDA Phones

PDAs

Wireless LAN

Microprocessor and DSP Solutions including MSM™, XScale™, ARM™, and OMAP™

Pin Configuration appears at end of data sheet.

MSM is a trademark of QUALCOMM, Inc.
XScale is a trademark of Intel Corp.
ARM is a trademark of ARM Limited.
OMAP is a trademark of Texas Instruments, Inc.

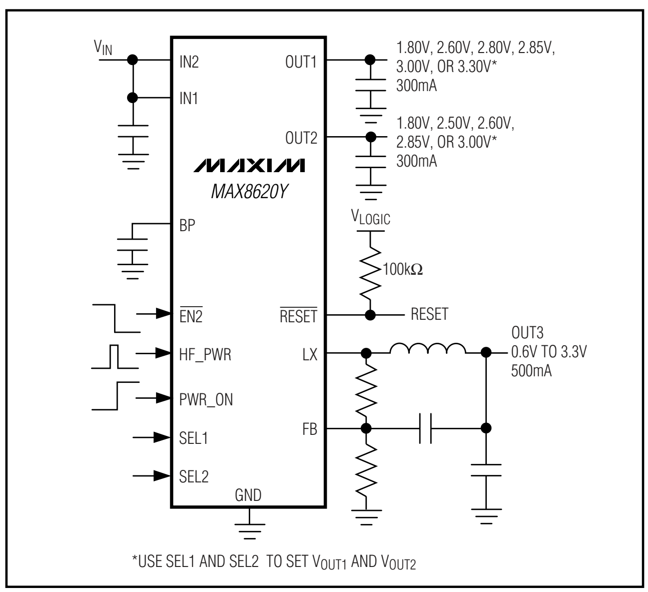
Features

- ♦ **Three Regulators and a Reset in One Package**
- ♦ **High-Efficiency Step-Down Converter**
  - **Up to 4MHz Fixed Switching Frequency**
  - **500mA Guaranteed Output Current**
  - **0.6V to 3.3V Adjustable Output Voltage**
  - **±2% Initial Accuracy**
  - **Fast Voltage-Positioning Transient Response**
  - **Internal Synchronous Rectifier**
- ♦ **Two 300mA LDO Regulators**
  - **200mV Dropout at 200mA Load**
  - **Low 45µV_{RMS} Output Noise**
  - **3% Accuracy over Line, Load, and Temperature**
  - **Overcurrent Protection**
  - **Nine Pin-Selectable Output-Voltage Settings**
- ♦ **30ms (min) $\overline{RESET}$ Output Flag**
- ♦ **2.7V to 5.5V Input**
- ♦ **115µA (typ) Supply Current at No Load**
- ♦ **Thermal-Overload Protection**
- ♦ **Tiny 3mm x 3mm x 0.8mm TDFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX8620YETD	-40°C to +85°C	14 TDFN-EP (T1433-2)	AAB

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

IN1, IN2, PWR_ON, $\overline{RESET}$, $\overline{EN2}$, SEL1, SEL2,
HF_PWR, FB, BP to GND ....-0.3V to +6.0V
OUT1, OUT2 to GND ....-0.3V to (V_{IN1} + 0.3V)
LX Current ....1.5A_{RMS}
Continuous Power Dissipation (T_A = +70°C)
14-Pin TDFN (derate 18.2mW/°C above +70°C) 1454mW

Operating Temperature Range ....-40°C to +85°C
Junction Temperature...+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN1} = V_{IN2} = +3.7V, C_{IN} = 10µF, C_{BP} = 0.01µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN1}		2.7		5.5	V
Shutdown Supply Current	I_{SHDN}	V_{IN1} = V_{IN2} = 4.2V, PWR_ON = HF_PWR = GND		5.5	10	µA
Supply Current	I_{IN1} + I_{IN2}	All outputs enabled, no load		115	140	µA
		V_{OUT1} = V_{OUT3} = 1.8V, I_{OUT1} = I_{OUT3} = 500µA, OUT2 disabled		430		
UNDERVOLTAGE LOCKOUT						
UVLO Threshold	V_{UVLO}	V_{IN1} = V_{IN2} rising	2.70	2.85	3.05	V
		V_{IN1} = V_{IN2} falling		2.35		
THERMAL PROTECTION						
Thermal-Shutdown Threshold		Temperature rising		+160		°C
Thermal-Shutdown Hysteresis				15		°C
REFERENCE (BP)						
Reference Bypass Output Voltage	V_{BP}	0 ≤ I_{BP} ≤ 1µA	1.231	1.250	1.269	V
LOGIC AND CONTROL INPUTS (PWR_ON, HF_PWR, $\overline{EN2}$)						
PWR_ON, HF_PWR, $\overline{EN2}$ Input Low Voltage	V_{IL}	V_{IN1} = V_{IN2} = 2.7V to 4.2V (Note 2)			0.4	V
PWR_ON, HF_PWR, $\overline{EN2}$ Input High Voltage	V_{IH}	V_{IN1} = V_{IN2} = 2.7V to 4.2V (Note 2)	1.44			V
Input Bias Current	I_{INB}	V_{PWR_ON} = V_{HF_PWR} = $V_{\overline{EN2}}$ = 0V or 5.5V	-1		+1	µA
HF_PWR Timer	t_{HF}	From the rising edge of HF_PWR until the one-shot timer expires (Figure 4)	1.05	1.31	1.46	s
LINEAR REGULATORS (OUT1, OUT2)						
OUT1, OUT2 Output-Voltage Accuracy	V_{OUT1}, V_{OUT2}	I_{LOAD} = 1mA, 3.7V ≤ V_{IN} ≤ 5.5V, 0°C to +85°C	-1.3		+1.8	%
		I_{LOAD} = 1mA, 3.7V ≤ V_{IN} ≤ 5.5V, -40°C to +85°C	-1.5		+1.8	
		1mA ≤ I_{LOAD} ≤ 300mA		-1.2		
		I_{LOAD} = 150mA		0		
OUT1, OUT2 Output Current	$I_{OUT\_}$		300			mA
OUT1, OUT2 Output Current Limit	$I_{LIM\_}$	$V_{OUT\_}$ = 0V	310	550	940	mA
OUT1, OUT2 Dropout Voltage	V_{DO}	I_{LOAD} = 200mA, T_A = +85°C (Note 3)		200	380	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = V_{IN2} = +3.7V, C_{IN} = 10μF, C_{BP} = 0.01μF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUT1, OUT2 Power-Supply Rejection Ratio		f = 10Hz to 10kHz, $C_{OUT\_}$ = 4.7μF, $I_{LOAD\_}$ = 30mA			60		dB
Output Noise Voltage		f = 100Hz to 100kHz, $C_{OUT\_}$ = 4.7μF, $I_{LOAD\_}$ = 30mA			45		$μV_{RMS}$
		f = 100Hz to 100kHz, $C_{OUT\_}$ = 4.7μF, $I_{LOAD\_}$ = 30mA, C_{BP} open			100		
STEP-DOWN CONVERTER (OUT3)							
Output Voltage Range	V_{OUT3}			0.6		3.3	V
FB Threshold Voltage	V_{TH}	V_{FB} falling			0.6		V
FB Threshold Line Regulation		V_{IN1} = V_{IN2} = 2.7V to 5.5V (Note 2)			0.08		%/V
FB Threshold Voltage Accuracy (Falling) (% of V_{TH})		I_{OUT3} = 0mA	T_A = +25°C	-2		+2	%
			T_A = -40°C to +85°C	-3		+3	
FB Threshold Voltage Hysteresis (% of V_{TH})	V_{HYS}				2		%
FB Bias Current	I_{FB}	OUT3 disabled			10		μA
		V_{FB} = 0.5V			10		
Current Limit	I_{LIM3P}	pFET switch		675	950	1200	mA
	I_{LIM3N}	nFET rectifier		875	1000	1200	
On-Resistance	R_{ONP}	pFET switch, I_{LX} = -200mA			0.65	1.5	Ω
	R_{ONN}	nFET rectifier, I_{LX} = +200mA			0.35	0.8	
Rectifier-Off Current Threshold	I_{LXOFF}				30	60	mA
Minimum On- and Off-Times	t_{ON}				107		ns
	t_{OFF}				95		
OPEN-DRAIN, ACTIVE-LOW RESET OUTPUT ($\overline{RESET}$)							
$\overline{RESET}$ Output-Voltage Low	V_{OL}	I_{SINK} = 500μA				0.3	V
$\overline{RESET}$ Output Leakage Current		$V_{\overline{RESET}}$ = 5.5V				100	nA
$\overline{RESET}$ Threshold Voltage	V_{THR}	Percent of the OUT1 regulation voltage (Note 4)		84	87	90	%
$\overline{RESET}$ Timeout Period	t_{RP}	Figure 4		30	60		ms
LDO OUTPUT-VOLTAGE SELECT INPUTS (SEL1, SEL2)							
SEL_ Input Low Threshold						1	V
SEL_ Input High Threshold				$V_{IN\_}$ - 0.2V			V
SEL_ Input Bias Current		V_{IN1} = V_{IN2} = 4.2V, V_{SEL1} = 0V or V_{IN1}, V_{SEL2} = 0V or V_{IN1}			±0.1		μA

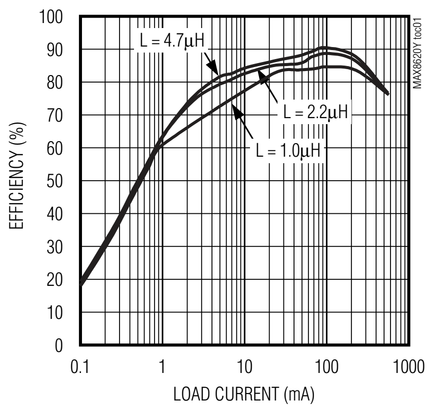
Note 1: Specifications are 100% production tested at T_A = +25°C. Maximum and minimum limits over temperature are guaranteed by design and characterization.
Note 2: After startup.
Note 3: Guaranteed by design.
Note 4: $\overline{RESET}$ asserts low when V_{OUT1} drops below the specified percent of the OUT1 regulation voltage.

µPMIC for Microprocessors or DSPs in Portable Equipment

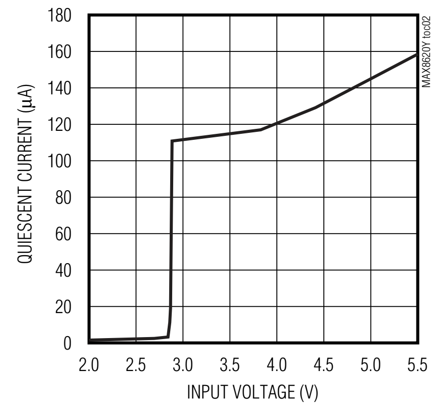
Typical Operating Characteristics

(V_{IN1} = V_{IN2} = 3.7V, PWR_ON = IN1, L = 2.2µH (LQH31CN2R2M53), C_{FF} = 150pF, V_{OUT1} = V_{OUT2} = 2.6V, V_{OUT3} = 1.867V (R1 = 150kΩ, R2 = 75kΩ), C_{IN} = 10µF, C_{BP} = 0.01µF, C_{OUT1} = C_{OUT2} = 4.7µF, C_{OUT3} = 2.2µF, $\overline{RESET}$ pulled up with 100kΩ to OUT1, T_A = +25°C, unless otherwise noted.)

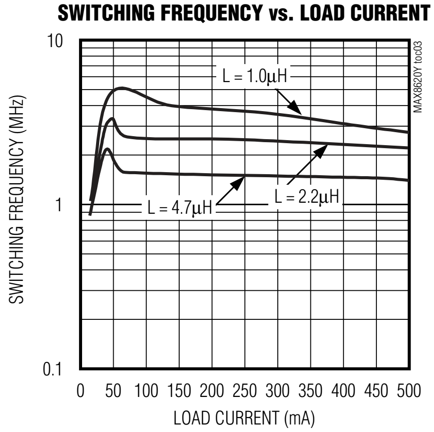
EFFICIENCY vs. LOAD CURRENT



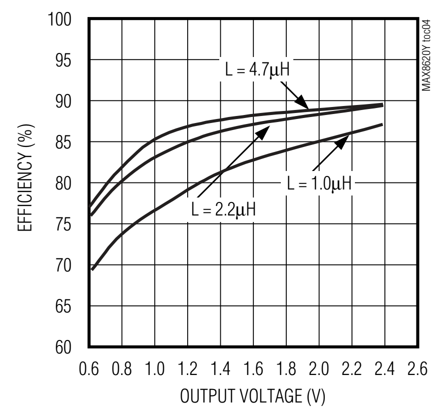
INPUT QUIESCENT CURRENT vs. INPUT VOLTAGE



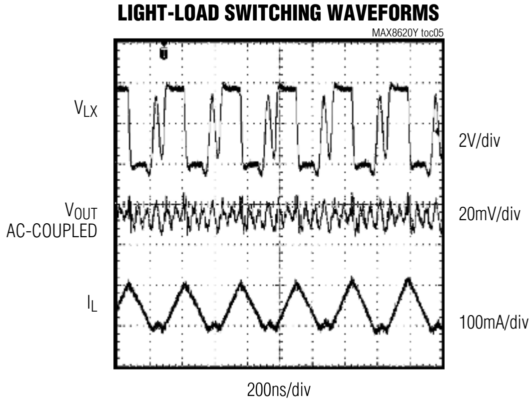
SWITCHING FREQUENCY vs. LOAD CURRENT



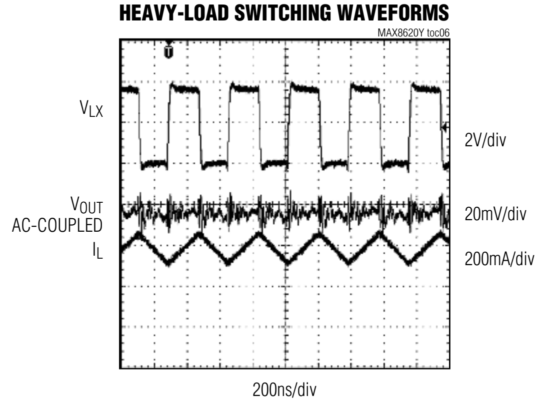
EFFICIENCY vs. OUTPUT VOLTAGE



LIGHT-LOAD SWITCHING WAVEFORMS



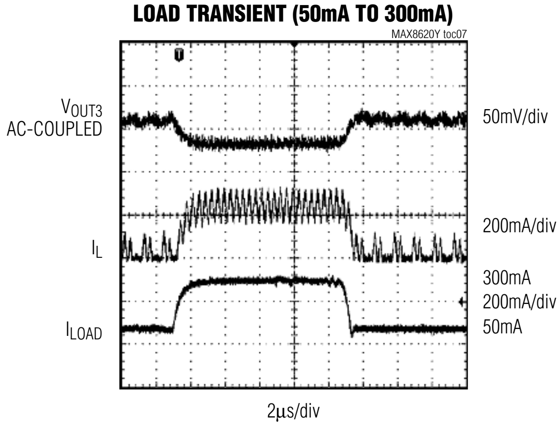
HEAVY-LOAD SWITCHING WAVEFORMS



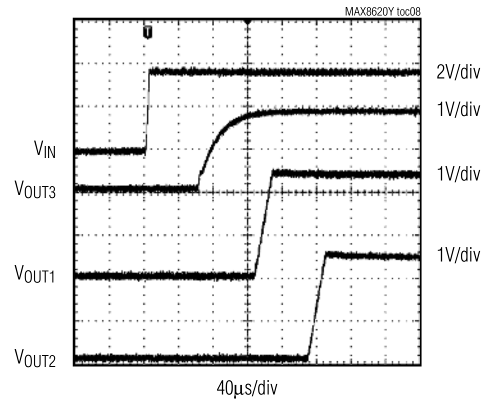
Typical Operating Characteristics (continued)

(V_{IN1} = V_{IN2} = 3.7V, PWR_ON = IN1, L = 2.2µH (LQH31CN2R2M53), C_{FF} = 150pF, V_{OUT1} = V_{OUT2} = 2.6V, V_{OUT3} = 1.867V (R1 = 150kΩ, R2 = 75kΩ), C_{IN} = 10µF, C_{BP} = 0.01µF, C_{OUT1} = C_{OUT2} = 4.7µF, C_{OUT3} = 2.2µF, $\overline{RESET}$ pulled up with 100kΩ to OUT1, T_A = +25°C, unless otherwise noted.)

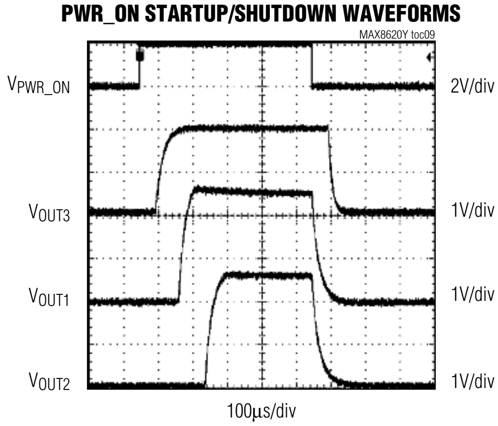
LOAD TRANSIENT (50mA TO 300mA)



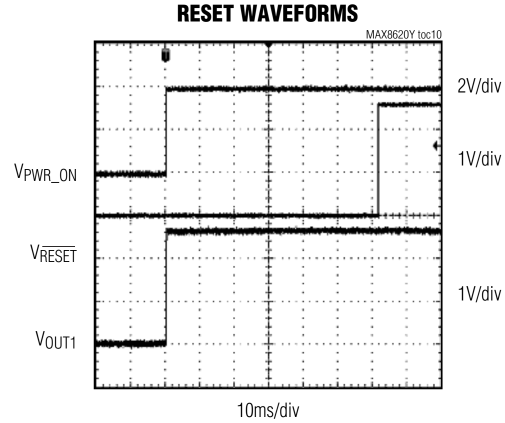
POWER-UP WAVEFORMS



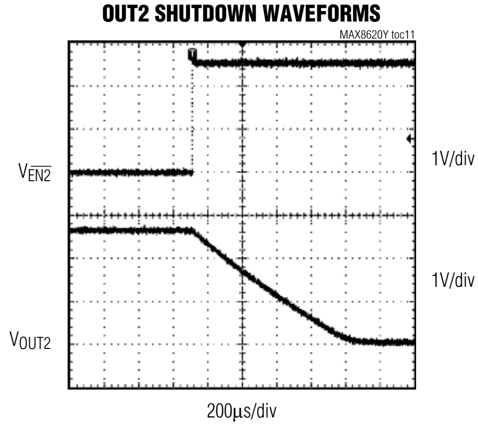
PWR_ON STARTUP/SHUTDOWN WAVEFORMS



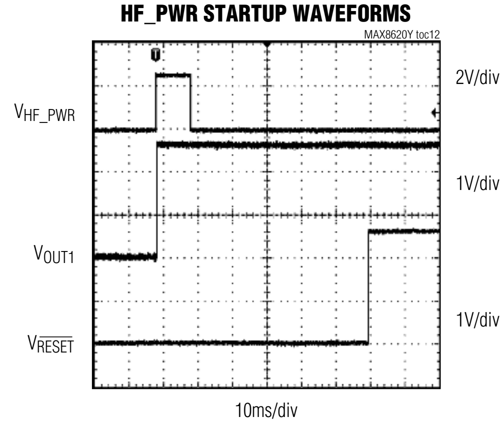
RESET WAVEFORMS



OUT2 SHUTDOWN WAVEFORMS



HF_PWR STARTUP WAVEFORMS

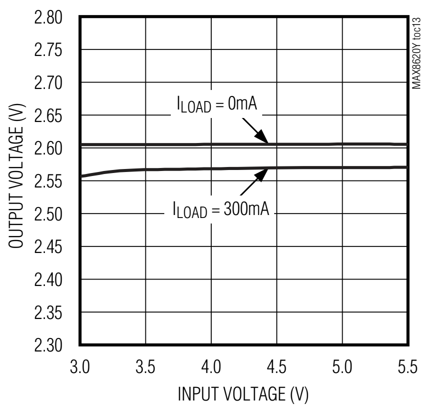


µPMIC for Microprocessors or DSPs in Portable Equipment

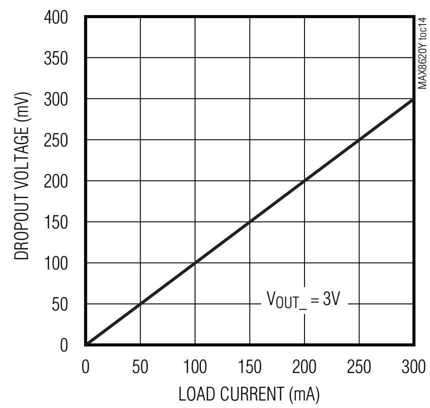
Typical Operating Characteristics (continued)

(V_{IN1} = V_{IN2} = 3.7V, PWR_ON = IN1, L = 2.2µH (LQH31CN2R2M53), C_{FF} = 150pF, V_{OUT1} = V_{OUT2} = 2.6V, V_{OUT3} = 1.867V (R1 = 150kΩ, R2 = 75kΩ), C_{IN} = 10µF, C_{BP} = 0.01µF, C_{OUT1} = C_{OUT2} = 4.7µF, C_{OUT3} = 2.2µF, $\overline{RESET}$ pulled up with 100kΩ to OUT1, T_A = +25°C, unless otherwise noted.)

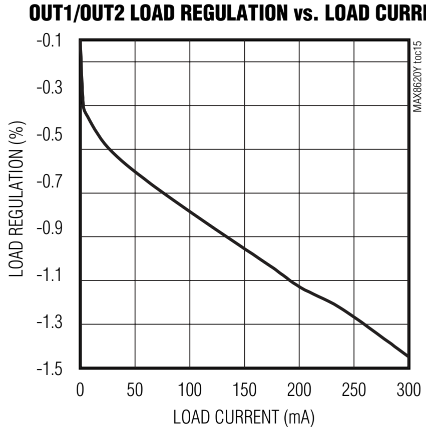
OUT1/OUT2 VOLTAGE vs. INPUT VOLTAGE



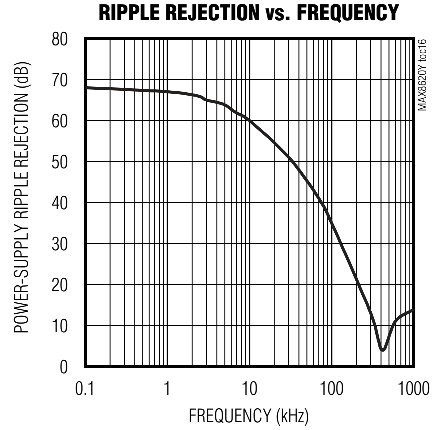
DROPOUT VOLTAGE vs. LOAD CURRENT



OUT1/OUT2 LOAD REGULATION vs. LOAD CURRENT



OUT1/OUT2 POWER-SUPPLY RIPPLE REJECTION vs. FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	SEL1	LDO Output-Voltage Select Input 1. SEL1 and SEL2 set the OUT1 and OUT2 voltages to one of nine combinations (Table 1).
2	SEL2	LDO Output-Voltage Select Input 2. SEL1 and SEL2 set the OUT1 and OUT2 voltages to one of nine combinations (Table 1).
3	$\overline{EN2}$	OUT2 Enable Input. Drive $\overline{EN2}$ low to enable OUT2. Drive $\overline{EN2}$ high to disable OUT2. If the MAX8620Y is placed into shutdown (PWR_ON = HF_PWR = low), OUT2 does not power regardless of the status of $\overline{EN2}$ (Table 2, Figure 4).
4	$\overline{RESET}$	Open-Drain, Active-Low Reset Output. $\overline{RESET}$ asserts low when V_{OUT1} drops below 87% (typ) of regulation. $\overline{RESET}$ remains asserted for t_{RP} after V_{OUT1} rises above 87% (typ) of regulation. $\overline{RESET}$ also asserts when OUT1 is disabled (Figure 4). $\overline{RESET}$ deasserts if OUT1 is enabled and V_{OUT1} is above 87% of regulation after t_{RP}.
5	BP	Reference Bypass Capacitor Node. Bypass BP with a 0.01µF capacitor to GND. BP is high impedance when the MAX8620Y is disabled (PWR_ON = HF_PWR = low).
6	HF_PWR	Hands-Free Enable Input. Drive HF_PWR high or apply a pulse to enable the MAX8620Y. Power is enabled for 1.31s (typ) following a rising edge at HF_PWR (Table 2, Figure 4).
7	PWR_ON	Power-Enable Input. Drive PWR_ON high to enable the MAX8620Y (Table 2, Figure 4). Drive PWR_ON low to enter shutdown mode. In shutdown, the LX node is high impedance and both LDOs are disabled (depending on the state of HF_PWR).
8	FB	Step-Down Converter Output-Voltage Feedback Input. V_{FB} regulates to 0.6V (typ). Connect FB to the center of an external resistor-divider between LX and GND to set V_{OUT3} between 0.6V and 3.3V (see the *Setting the Step-Down Output Voltage (OUT3)* section).
9	GND	Ground. Connect GND to the exposed pad.
10	LX	Inductor Connection. LX is internally connected to the drain of the internal p-channel power MOSFET and the drain of the n-channel synchronous rectifier. LX is high impedance when OUT3 is disabled.
11	IN2	Power Input 2. Connect IN2 to IN1 as close to the device as possible.
12	IN1	Power Input 1. Connect IN1 to IN2 as close to the device as possible. Bypass IN1 to GND with a 10µF ceramic capacitor, as close to the device as possible.
13	OUT1	300mA LDO Output 1. Bypass OUT1 to GND with a 4.7µF ceramic capacitor for 300mA applications, or a 2.2µF ceramic capacitor for 150mA applications. OUT1 is high impedance when disabled.
14	OUT2	300mA LDO Output 2. Bypass OUT2 to GND with a 4.7µF ceramic capacitor for 300mA applications, or a 2.2µF ceramic capacitor for 150mA applications. OUT2 is high impedance when disabled.
EP	EP	Exposed Pad. Connect EP to GND.

Detailed Description

The MAX8620Y μPMIC is designed to power low-core-voltage microprocessors or DSPs in portable devices. The μPMIC contains a fixed-frequency, high-efficiency step-down converter; two low-dropout regulators (LDOs); a 30ms (min) reset timer; and power-on/off control logic (Figure 1).

Step-Down DC-DC Control Scheme

The MAX8620Y step-down converter is optimized for high-efficiency voltage conversion over a wide load range while maintaining excellent transient response, minimizing external component size, and minimizing output voltage ripple. The DC-DC converter (OUT3) also features an optimized on-resistance internal MOSFET switch and synchronous rectifier to maximize efficiency. The MAX8620Y utilizes a proprietary hysteretic-PWM control scheme that switches with nearly fixed frequency up to 4MHz, allowing for ultra-small external components. The step-down converter output current is guaranteed up to 500mA.

When the step-down converter output voltage falls below the regulation threshold, the error comparator begins a switching cycle by turning the high-side pFET switch on. This switch remains on until the minimum on-time (t_{ON}) expires and the output voltage is in regulation or the current-limit threshold (I_{LIM3P}) is exceeded. Once off, the high-side switch remains off until the minimum off-time (t_{OFF}) expires and the output voltage again falls below the regulation threshold. During this off period, the low-side synchronous rectifier turns on and remains on until either the high-side switch turns on or the inductor current reduces to the rectifier-off current threshold (I_{LXOFF} = 30mA (typ)). The internal synchronous rectifier eliminates the need for an external Schottky diode.

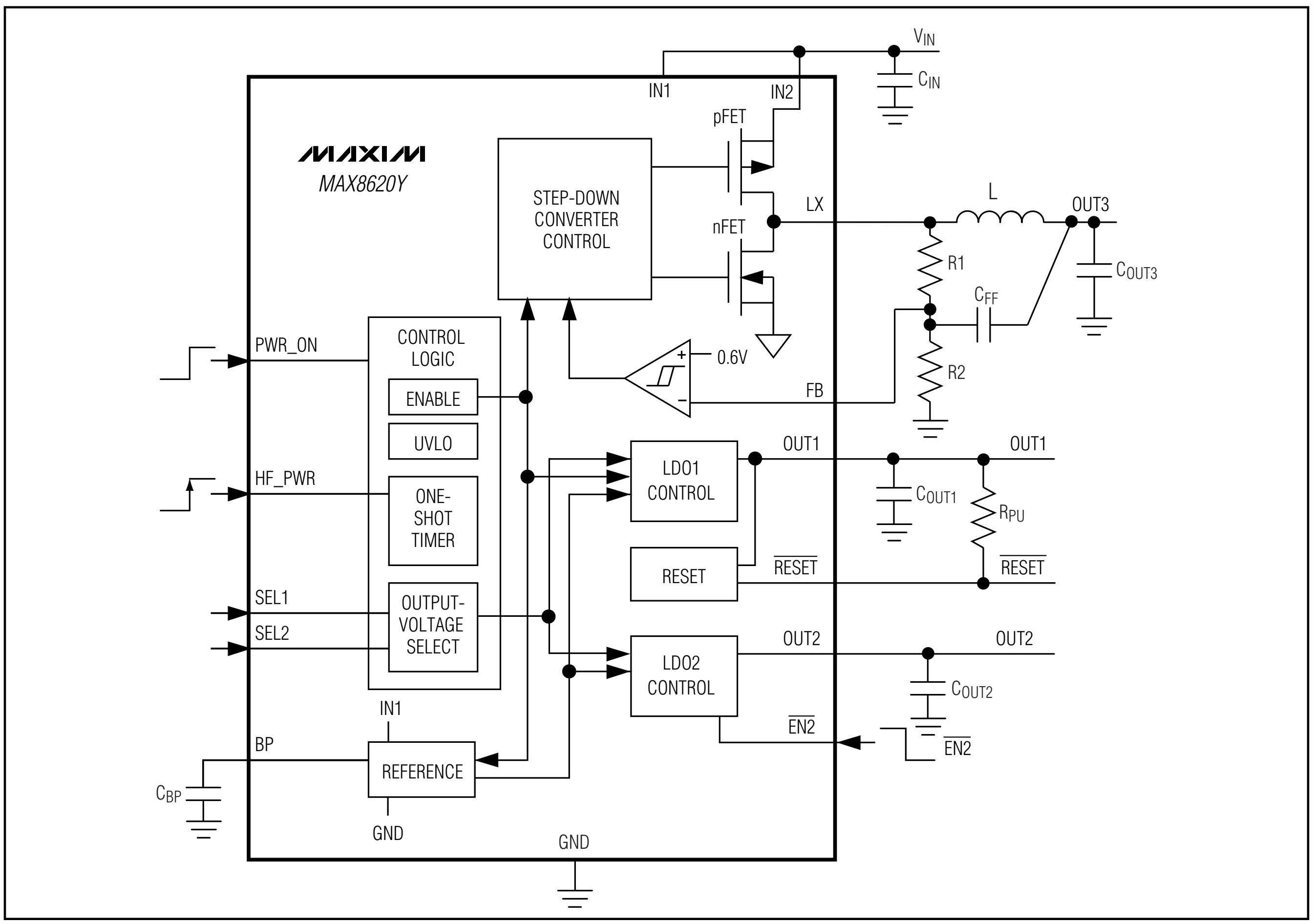


Figure 1. Functional Diagram

Voltage-Positioning Load Regulation

As seen in Figure 2, the MAX8620Y uses a unique step-down converter feedback network. By taking feedback from the LX node through R1, the usual phase lag due to the output capacitor is removed, making the loop exceedingly stable and allowing the use of a very small ceramic output capacitor. This configuration causes the output voltage to shift by the inductor series resistance multiplied by the load current. This output-voltage shift is known as voltage-positioning load regulation. Voltage-positioning load regulation greatly reduces overshoot during load transients, which effectively halves the peak-to-peak output-voltage excursions compared to traditional step-down converters. See the Load-Transient Response graph in the *Typical Operating Characteristics* section.

Two low-dropout, low-quiescent-current, high-accuracy linear regulators supply loads up to 300mA each. The LDO output voltages are set using SEL1 and SEL2 (see Table 1). As shown in Figure 3, the LDOs include an internal reference, error amplifiers, p-channel pass transistors, internal-programmable voltage-dividers, and an OUT1 power-good comparator. Each error amplifier compares the reference voltage to a feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled lower, allowing more current to pass to the outputs and increasing the output voltage. If the feedback voltage is too high, the pass-transistor gate is pulled up, allowing less current to pass to the output.

Table 1. MAX8620Y Output-Voltage Selection

SEL1	SEL2	OUT1	OUT2
IN1	IN1	3.00V	2.50V
IN1	OPEN	2.85V	2.85V
IN1	GND	3.00V	3.00V
OPEN	IN1	3.30V	2.50V
OPEN	OPEN	2.80V	2.60V
OPEN	GND	3.30V	1.80V
GND	IN1	2.85V	2.60V
GND	OPEN	2.60V	2.60V
GND	GND	1.80V	2.60V

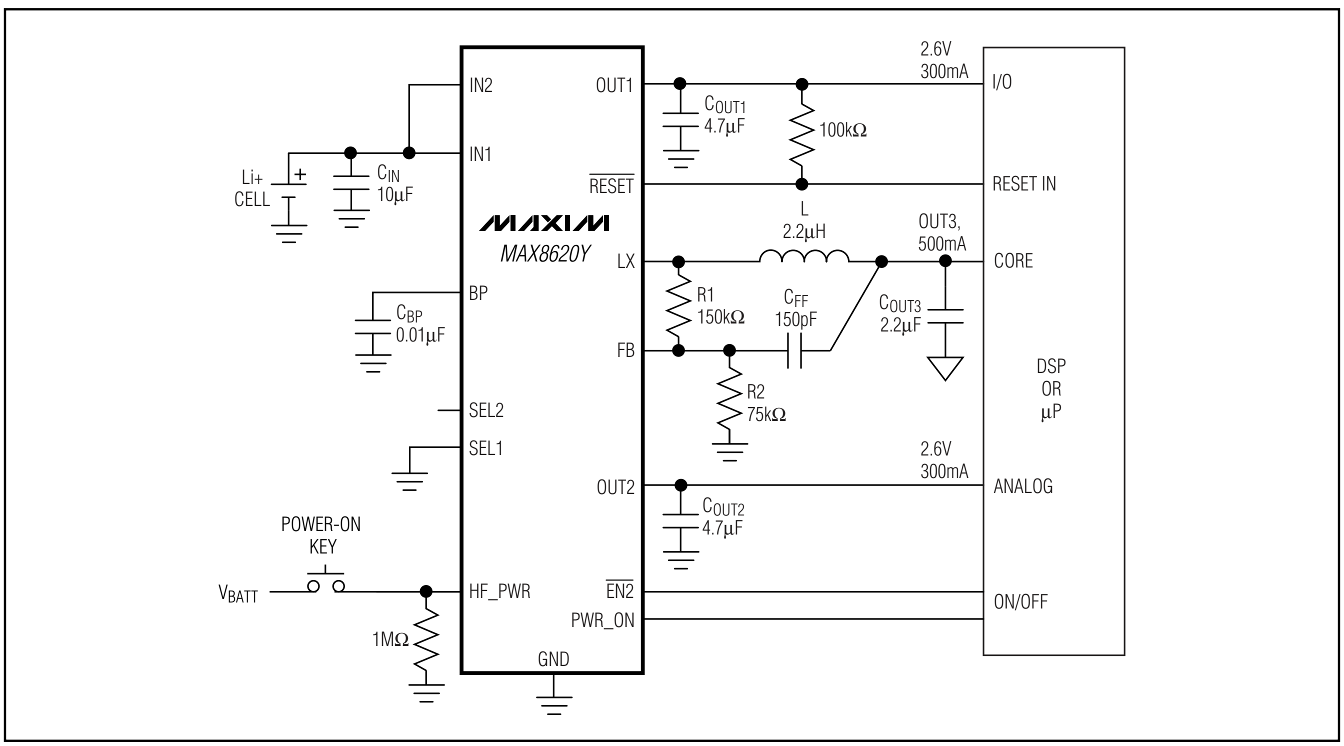


Figure 2. Typical MAX8620Y DSP or µP Application

µPMIC for Microprocessors or DSPs in Portable Equipment

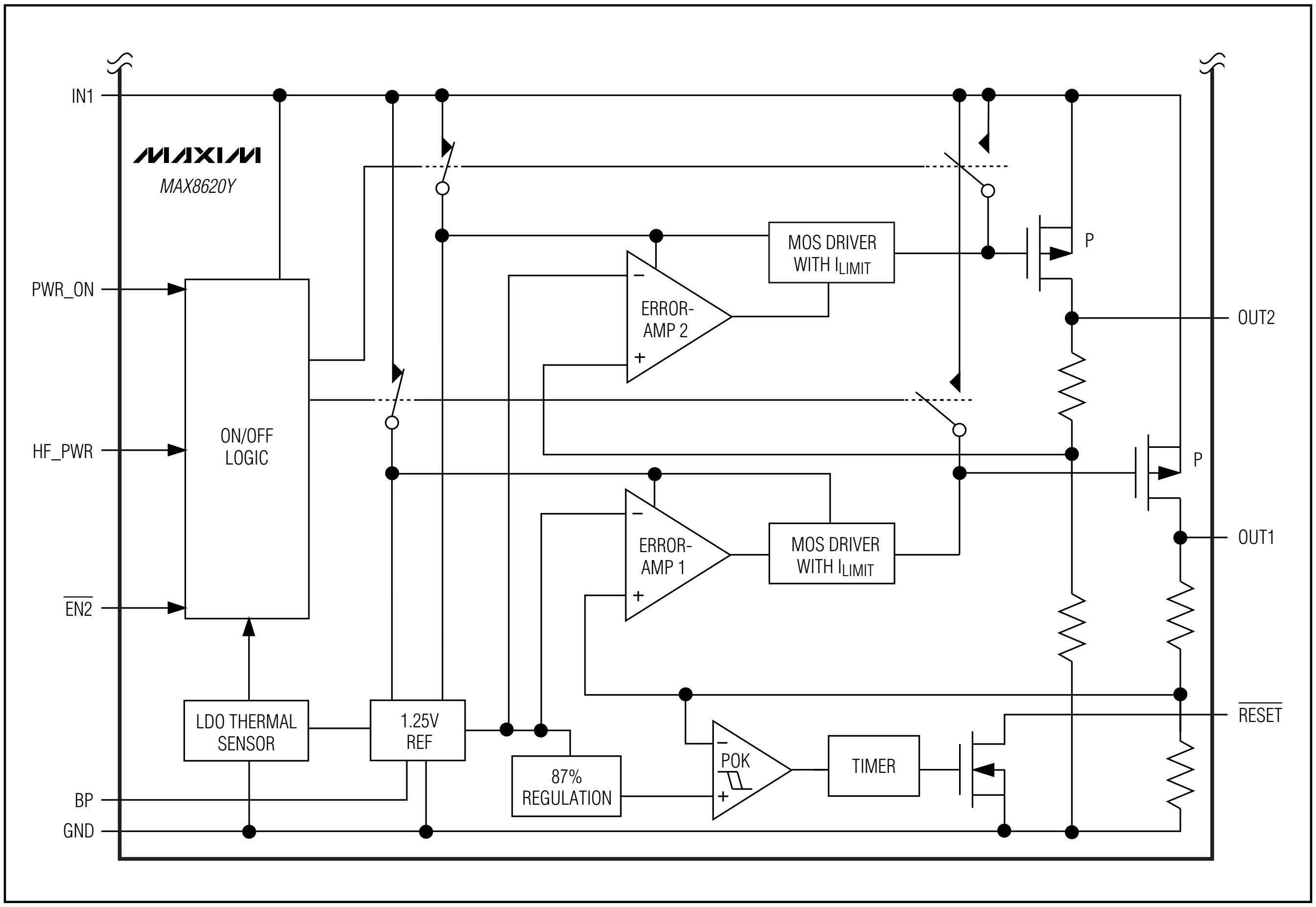


Figure 3. Linear-Regulator Functional Diagram

LDO Output-Voltage Selection (SEL1, SEL2)

As shown in Table 1, the LDO output voltages, OUT1 and OUT2, are set according to the logic states of SEL1 and SEL2. SEL1 and SEL2 are trilevel inputs: IN1, open, and GND. The input voltage, V_{IN1}, must be a dropout voltage (V_{DO}) greater than the selected OUT1 and OUT2 voltages.

Power-Enable Input (PWR_ON)

Drive PWR_ON low to place the MAX8620Y in power-down mode and reduce supply current to 5.5µA (typ). Connect PWR_ON to IN1 = IN2 or logic-high to enable the MAX8620Y. $\overline{EN2}$ enables and disables OUT2 when PWR_ON is high (Table 2). OUT1, OUT2, and OUT3 are all disabled when PWR_ON is low. HF_PWR can temporarily bring the MAX8620 out of power-down mode when PWR_ON is low (see the *HF_PWR* section). In power-down, the control circuitry, internal-switching p-channel MOSFET, and the internal synchronous rectifier (n-channel MOSFET) turn off, and LX becomes high impedance. In addition, both LDOs are disabled.

OUT2 Enable ($\overline{EN2}$)

Drive $\overline{EN2}$ low to enable OUT2. Drive $\overline{EN2}$ high to disable OUT2. If the MAX8620Y is placed into power-down using PWR_ON (PWR_ON = low), OUT2 does not power regardless of the status of $\overline{EN2}$ (Table 2).

Table 2. MAX8620Y Power Modes

PWR_ON	HF_PWR*	$\overline{EN2}$	OUT1 AND OUT3	OUT2
1	X	1	Enabled	Disabled
1	X	0	Enabled	Enabled
0	1	1	Enabled	Disabled
0	1	0	Enabled	Enabled
0	0	X	Disabled	Disabled

**A rising edge at HF_PWR initiates a 1.31s one-shot timer. The status of HF_PWR shown in Table 2 indicates whether the one-shot period has expired as follows:*

1 = During t_{HP}

0 = t_{HP} has expired

Hands-Free Enable Input (HF_PWR)

A rising edge at HF_PWR generates an internal one-shot pulse that enables the MAX8620Y for 1.31s (t_{HF}). If HF_PWR remains high after t_{HF} expires, the MAX8620Y reenters shutdown. During t_{HF}, OUT3 and OUT1 are enabled so the microprocessor (µP) can initialize and assert a logic-high at PWR_ON. OUT2 enables during t_{HF} if $\overline{EN2}$ is low. Once PWR_ON is high, the status of HF_PWR is ignored. If PWR_ON remains low after t_{HF} expires, the MAX8620Y reenters shutdown.

Power-Supply Sequencing

The step-down converter output (OUT3) always powers up first and powers down last (Figure 4). OUT1 powers approximately 70µs after OUT3, and OUT2 powers approximately 50µs after V_{OUT1} reaches 87% (typ) of its regulation voltage. When PWR_ON goes low, OUT1 turns off, then OUT2 turns off, then OUT3 turns off 50µs after PWR_ON goes low.

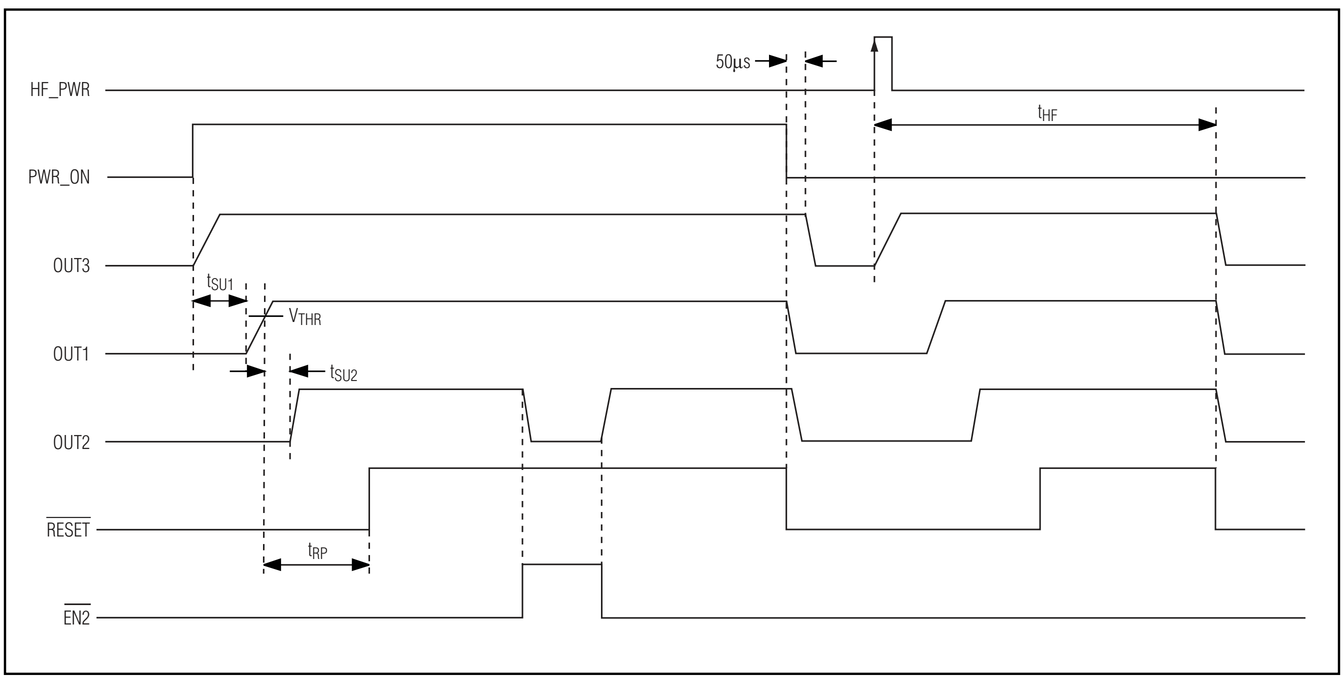


Figure 4. MAX8620Y Power-Supply Sequencing

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Reset Output (RESET)

RESET is an open-drain, active-low output that indicates the status of OUT1. RESET is typically pulled up through a 100kΩ resistor to the system logic voltage. RESET asserts at power-up. The reset timer begins once V_{OUT1} reaches 87% of regulation. RESET deasserts 60ms after V_{OUT1} rises above 87% (typ) of regulation (see the *Typical Operating Characteristics*). RESET also asserts when OUT1 is disabled.

Reference Bypass Capacitor Node (BP)

An optional 0.01µF bypass capacitor at BP creates a lowpass filter for LDO noise reduction. OUT1 and OUT2 exhibit 45µV_{RMS} of output-voltage noise with C_{BP} = 0.01µF and C_{OUT1} = C_{OUT2} = 4.7µF.

Undervoltage Lockout

V_{IN1} = V_{IN2} must exceed the 2.85V typical undervoltage-lockout threshold (V_{UVLO}) before the MAX8620Y enables OUT3 to begin power-supply sequencing (see the *Power-Supply Sequencing* section). The UVLO threshold hysteresis is typically 0.5V.

Current Limiting

The MAX8620Y 300mA LDOs limit their output current to $I_{LIM\_}$ = 550mA (typ). If the LDO output current exceeds $I_{LIM\_}$, the corresponding LDO output voltage drops. The step-down converter limits I_{LIM3P} to 675mA (min).

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX8620Y. Independent thermal-protection circuits monitor the step-down converter and the linear-regulator circuits. When the MAX8620Y junction temperature exceeds T_J = +160°C, the thermal-overload protection circuit disables the corresponding circuitry, allowing the IC to cool. The thermal-overload protection circuitry enables the MAX8620Y after the junction temperature cools by 15°C, resulting in a pulsed output during continuous thermal-overload conditions. Thermal-overload protection safeguards the MAX8620Y in the event of fault conditions. For continuous operation, do not exceed the absolute-maximum junction-temperature rating of T_J = +150°C.

Applications Information

Power-On Closed-Loop System

When the MAX8620Y is used in conjunction with a microcontroller, HF_PWR and PWR_ON can implement a short-key power-on closed-loop system (Figure 5). The MAX8620Y detects a rising edge at HF_PWR and generates an internal 1.31s (typ) one-shot pulse that begins power sequencing and temporarily enables OUT1, OUT2, and OUT3 (depending on the state of EN2). The 1.31s of power provides time for the processor to initialize and assert a logic-high at PWR_ON. Once PWR_ON is driven high, OUT3, OUT1, and OUT2 (depending on the state of EN2) remain enabled. If the microcontroller does not drive PWR_ON high during t_{HF}, the MAX8620Y disables OUT1, OUT2, and OUT3, and reenters shutdown.

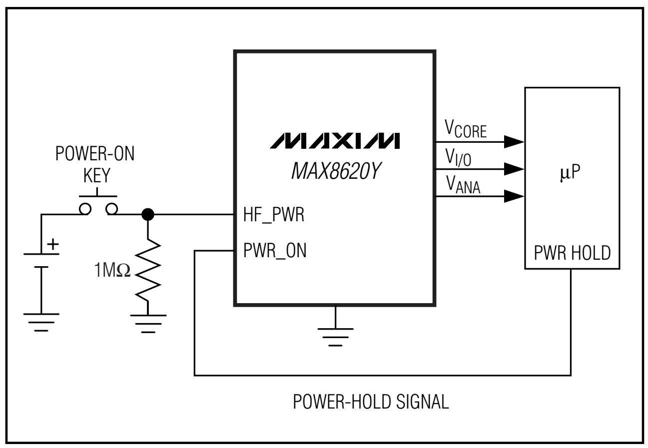

Figure 5. Short-Key Power-On Closed-Loop System

If a long-key press is preferred, see Figure 6. PWR_ON must remain high until a microprocessor asserts a logic-high signal when using this circuit. If a system includes multiple power-on sources, use a diode OR configuration, as shown in Figure 7.

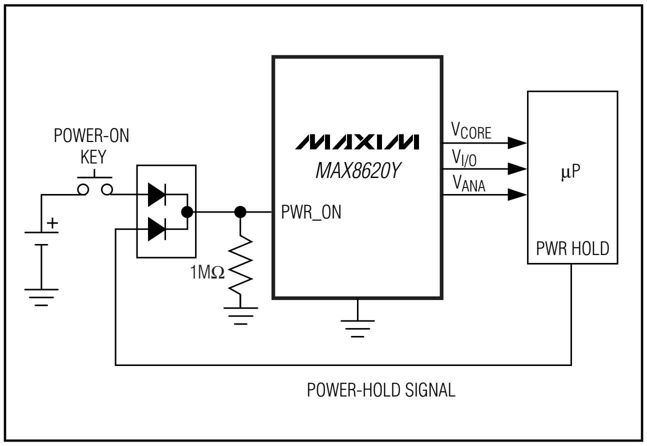

Figure 6. Long-Key Power-On Closed Loop

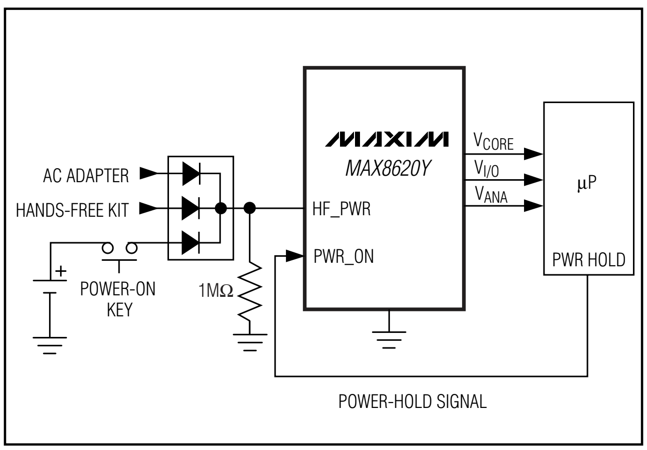

Figure 7. Multiple Power-On Inputs

Setting the Step-Down Output Voltage (OUT3)

Select a step-down converter output voltage between 0.6V and 3.3V by connecting a resistor voltage-divider between LX, FB, and GND (see Figure 2*)*. The FB bias current, I_{FB}, is typically 10nA. Select R2 so the resistor-divider bias current dominates I_{FB} by a factor of 10. A wide range of resistor values is acceptable, but a good starting point is to choose R2 = 100kΩ. R1 is given by:

$$R1 = R2\left(\frac{V_{OUT3}}{V_{FB}} - 1\right)$$

where V_{FB} = 0.6V.

V_{OUT3} can be set between 0.6V and 3.3V, but the step-down converter dropout voltage and inductor voltage drop impact how close V_{OUT3} can be to V_{IN2}. Total dropout voltage is a function of the pFET on-resistance, the DCR of the inductor, and the load as follows:

$$V_{OUT3(DO)} = I_{OUT3} \times (R_{ONP} + DCR_{INDUCTOR})$$

For example, with 300mA load:

$$V_{OUT3(DO)} = 300mA \times (0.65\Omega + 50m\Omega) = 210mV$$

As a result, V_{IN1} = V_{IN2} must exceed the desired V_{OUT3} by 210mV to maintain regulation.

Inductor Selection

The MAX8620Y step-down converter operates with inductors between 1µH and 4.7µH. Low inductance values are physically smaller but require faster switching, which results in some efficiency loss. See the *Typical Operating Characteristics* section for efficiency and switching frequency versus inductor value plots. The inductor's DC current rating needs to be only 100mA greater than the application's maximum load current because the MAX8620Y step-down converter features zero-current overshoot during startup and load transients.

For output voltages above 2.0V, when light-load efficiency is important, the minimum recommended inductor is 2.2µH. For optimum voltage-positioning load transients, choose an inductor with DC series resistance in the 50mΩ to 150mΩ range (Table 3). For higher efficiency at heavy loads (above 200mA) or minimal load regulation (but some transient overshoot), the resistance should be kept below 100mΩ. For light-load applications up to 200mA, much higher resistance is acceptable with very little impact on performance.

Table 3. Suggested Inductors

MANUFACTURER	SERIES	INDUCTANCE (µH)	ESR (Ω)	CURRENT RATING (mA)	DIMENSIONS (mm)
Taiyo Yuden	LB2012	1.0 2.2	0.15 0.23	300 240	2.0 x 1.25 x 1.25 = 3.1mm^3
	LB2016	1.0 1.5 2.2 3.3	0.09 0.11 0.13 0.20	455 350 315 280	2.0 x 1.6 x 1.8 = 5.8mm^3
	LB2518	1.0 1.5 2.2 3.3	0.06 0.07 0.09 0.11	500 400 340 270	2.5 x 1.8 x 2.0 = 9mm^3
	LBC2518	1.0 1.5 2.2 3.3 4.7	0.08 0.11 0.13 0.16 0.20	775 660 600 500 430	2.5 x 1.8 x 2.0 = 9mm^3
	CB2012	2.2 4.7	0.23 0.40	410 300	2.0 x 1.25 x 1.25 = 3.1mm^3
	CB2016	2.2 4.7	0.13 0.25	510 340	2.0 x 1.6 x 1.8 = 5.8mm^3
	CB2518	2.2 4.7	0.09 0.13	510 340	2.5 x 1.8 x 2.0 = 9mm^3
Murata	LQH32C_53	1.0 2.2 4.7	0.06 0.10 0.15	1000 790 650	3.2 x 2.5 x 1.7 = 14mm^3
	LQM43FN	2.2 4.7	0.10 0.17	400 300	4.5 x 3.2 x 0.9 = 13mm^3
TOKO	D310F	1.5 2.2 3.3	0.13 0.17 0.19	1230 1080 1010	3.6 x 3.6 x 1.0 = 13mm^3
	D312C	1.5 2.2 2.7 3.3	0.10 0.12 0.15 0.17	1290 1140 980 900	3.6 x 3.6 x 1.2 = 16mm^3
Sumida	CDRH2D11	1.5 2.2 3.3 4.7	0.05 0.08 0.10 0.14	900 780 600 500	3.2 x 3.2 x 1.2 = 12mm^3

Capacitor Selection

Step-Down Converter Output Capacitor

The output capacitor, C_{OUT3}, is required to keep the output voltage ripple small and to ensure regulation loop stability. C_{OUT3} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the unique feedback network, the output capacitance can be very low. For most applications, a 2.2µF capacitor is sufficient. For optimum load-transient performance and very low output ripple, the output capacitor value in µFs should be equal to or larger than the inductor value in µHs.

Input Capacitor

The input capacitor, C_{IN}, reduces the current peaks drawn from the battery or input power source and reduces switching noise in the IC. The impedance of C_{IN} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. Use a 10µF ceramic capacitor or equivalent amount of multiple capacitors in parallel between IN1 and GND. Connect C_{IN} as close as possible to the MAX8620Y to minimize the impact of PC board trace inductance.

Feed-Forward Capacitor

The feed-forward capacitor, C_{FF}, sets the feedback loop response, controls the switching frequency, and is critical in obtaining the best efficiency possible. Choose a small ceramic C0G (NPO) or X7R capacitor with a value given by:

$$C_{FF} = \frac{L}{R1} \times 10S$$

where R1 is the resistor between LX and FB (Figure 2). Select the closest standard value to C_{FF} as possible.

LDO Output Capacitors

For applications that require greater than 150mA of output current, connect a 4.7µF ceramic capacitor between the LDO output and GND. For applications that require less than 150mA of output current, connect a 2.2µF ceramic capacitor between the LDO output and GND. The LDO output capacitor's ($C_{OUT\_}$) equivalent series resistance (ESR) affects stability and output noise. Use output capacitors with an ESR of 0.1Ω or less to ensure stability and optimum transient response. Surface-mount ceramic capacitors have very low ESR and are commonly available in values up to 10µF. Connect C_{OUT} as close as possible to the MAX8620Y to minimize the impact of PC board trace inductance.

Power Dissipation and Thermal Considerations

The MAX8620Y total power dissipation, P_D, is estimated using the following equations:

$$P_D = P_{LOSS(OUT1)} + P_{LOSS(OUT2)} + P_{LOSS(OUT3)}$$

$$P_{LOSS(OUT1)} = I_{(OUT1)}(V_{IN} - V_{OUT1})$$

$$P_{LOSS(OUT2)} = I_{(OUT2)}(V_{IN} - V_{OUT2})$$

$$P_{LOSS(OUT3)} = P_{IN(OUT3)}\left(1 - \frac{\eta}{100}\right) - I_{(OUT3)}^2 \times R_{DC(INDUCTOR)}$$

where $P_{IN(OUT3)}$ is the input power for OUT3, η is the step-down converter efficiency, and $R_{DC(INDUCTOR)}$ is the inductor's DC resistance.

The die junction temperature can be calculated as follows:

$$T_J = T_A + P_D \times \theta_{JA}$$

where θ_{JA} = 55°C/W at +70°C.

T_J should not exceed +150°C in normal operating conditions.

PC Board Layout and Routing

High switching frequencies and relatively large peak currents make the PC board layout a very important aspect of design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Connect C_{IN} close to IN1 and GND. Connect the inductor and output capacitors (C_{OUT3}) as close to the IC as possible and keep the traces short, direct, and wide.

The traces between C_{OUT3}, C_{FF}, and FB are sensitive to inductor magnetic-field interference. Route these traces between ground planes or keep the traces away from the inductor.

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Connect GND to the ground plane. The external feedback network should be very close to the FB pin, within 0.2in (5mm). Keep noisy traces, such as the LX node, as short as possible. Connect GND to the exposed paddle directly under the IC. Figure 8 and the MAX8620Y evaluation kit illustrate examples of PC board layout and routing schemes.

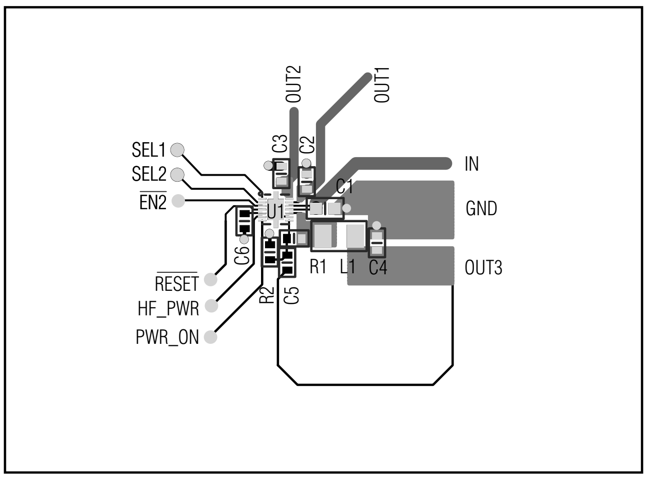
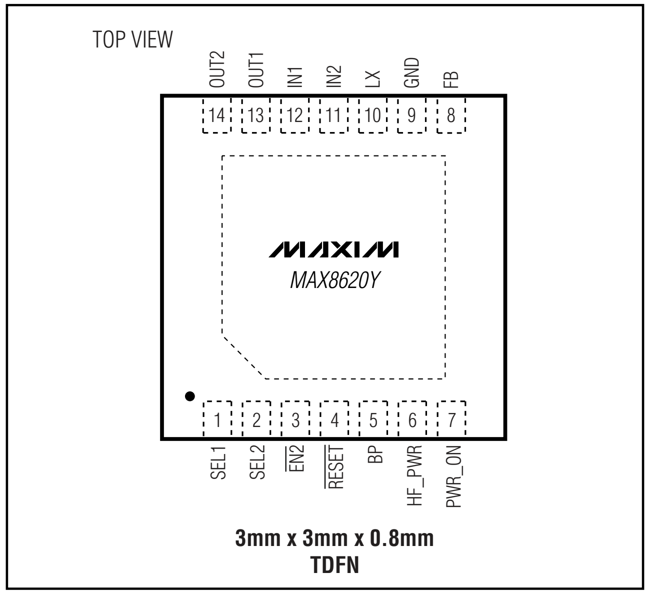


Figure 8. Recommended PC Board Layout

Pin Configuration



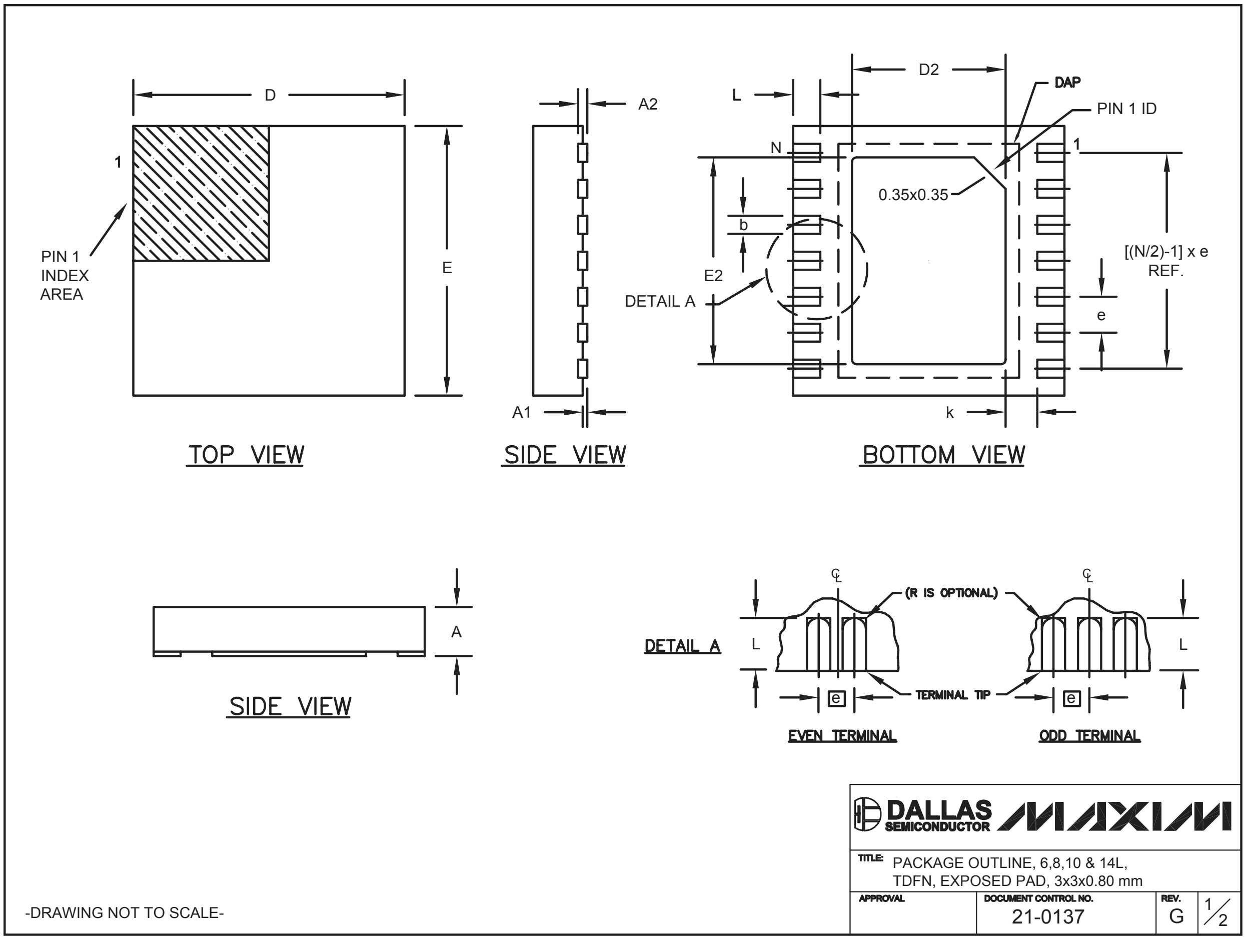
Chip Information

TRANSISTOR COUNT: 4481

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



6, 8, &10L, DFN THIN.EPS

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Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS								
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e	DOWNBONDS ALLOWED
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	YES
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	NO
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF	YES
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF	NO

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

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