Features

- Master and Slave Operation Possible
- Supply Voltage up to 40V
- Operating voltage V_S = 5V to 27V
- Typically 10µA Supply Current During Sleep Mode
- Typically 57µA Supply Current in Silent Mode
- Linear Low-drop Voltage Regulator, 85mA Current Capability:
  - Normal, Fail-safe, and Silent Mode
  - Atmel ATA6622 V_{CC} = 3.3V ±2%
  - Atmel ATA6624 V_{CC} = 5.0V ±2%
  - Atmel ATA6626 V_{CC} = 5.0V ±2%, TXD Time-out Timer Disabled
  - In Sleep Mode V_{CC} is Switched Off
- VCC- Undervoltage Detection (4ms Reset Time) and Watchdog Reset Logical Combined at Open Drain Output NRES
- Negative Trigger Input for Watchdog
- Boosting the Voltage Regulator Possible with an External NPN Transistor
- LIN Physical Layer According to LIN 2.0, 2.1 and SAEJ2602-2
- Wake-up Capability via LIN-bus, Wake Pin, or KI_15 Pin
- INH Output to Control an External Voltage Regulator or to Switch off the Master Pull Up Resistor
- TXD Time-out Timer; Atmel ATA6626: TXD Time-out Timer Is Disabled
- Bus Pin is Overtemperature and Short Circuit Protected versus GND and Battery
- Adjustable Watchdog Time via External Resistor
- Advanced EMC and ESD Performance
- Fulfills the OEM “Hardware Requirements for LIN in automotive Applications Rev.1.0”
- Interference and Damage Protection According ISO7637
- Package: QFN 5mm × 5mm with 20 Pins

LIN Bus Transceiver with 3.3V (5V) Regulator and Watchdog

ATA6622
ATA6624
ATA6626
ATA6622C
ATA6624C
ATA6626C

1. Description

The Atmel® ATA6622 is a fully integrated LIN transceiver, which complies with the LIN 2.0, 2.1 and SAEJ2602-2 specifications. It has a low-drop voltage regulator for 3.3V/85mA output and a window watchdog. The Atmel ATA6624 has the same functionality as the Atmel ATA6622; however, it uses a 5V/85mA regulator. The Atmel ATA6626 has the same functionality as Atmel ATA6624 without a TXD time-out timer. The voltage regulator is able to source 85mA, but the output current can be boosted by using an external NPN transistor. This chip combination makes it possible to develop inexpensive, simple, yet powerful slave and master nodes for LIN-bus systems. Atmel ATA6622/ATA6624/ATA6626 are designed to handle the low-speed data communication in vehicles, e.g., in convenience electronics. Improved slope control at the LIN-driver ensures secure data communication up to 20kBaud. Sleep Mode and Silent Mode guarantee very low current consumption. The Atmel ATA6626 is able to switch the LIN unlimited to dominant level via TXD for low data rates.

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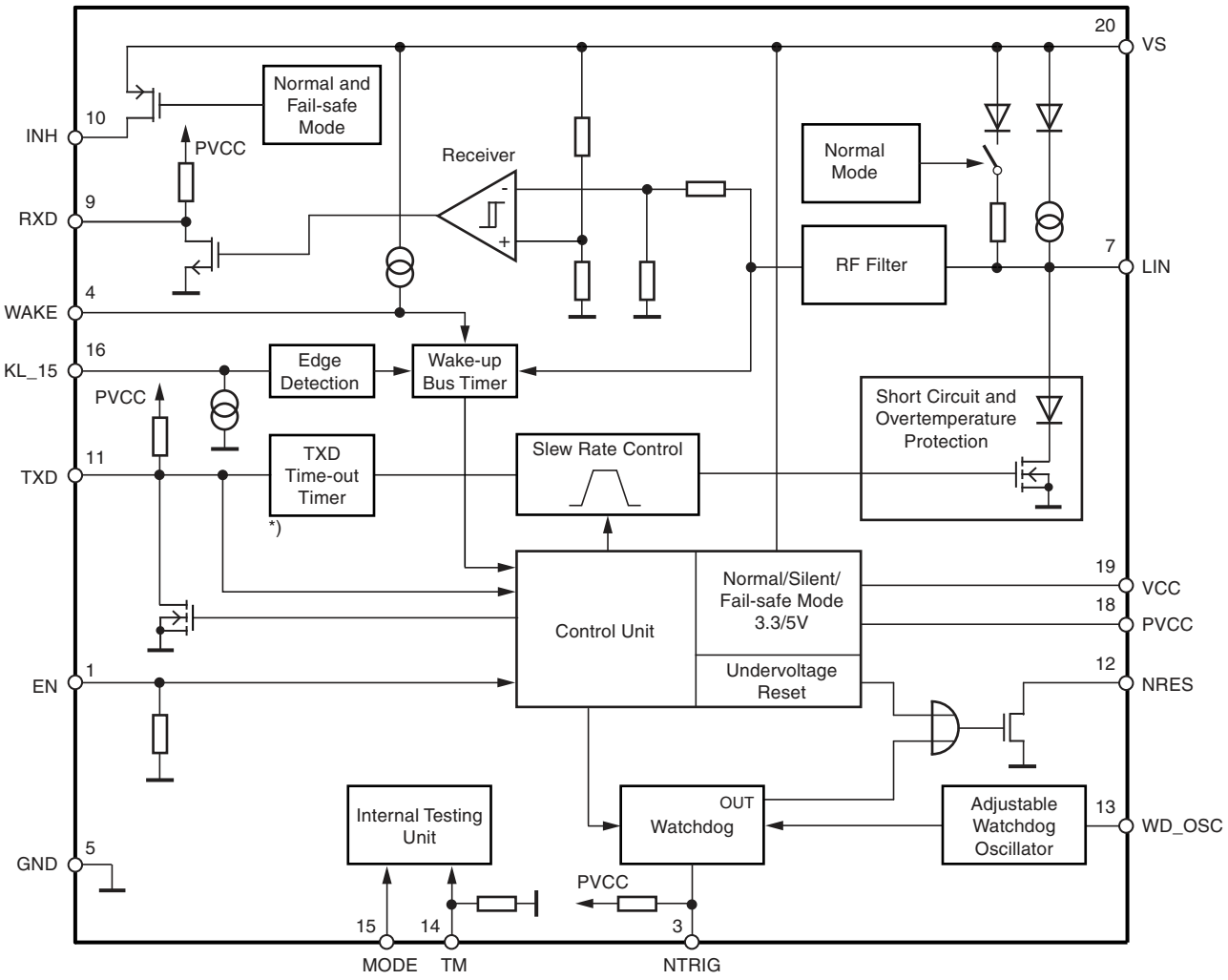
Figure 1-1. Block Diagram



*) Not in ATA6626

2. Pin Configuration

Figure 2-1. Pinning QFN20

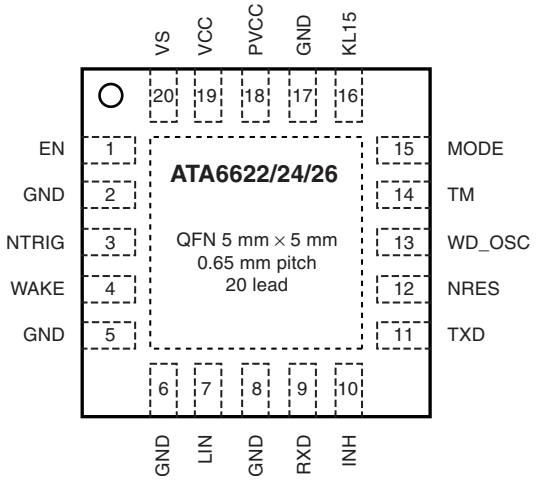


Table 2-1. Pin Description

Pin	Symbol	Function
1	EN	Enables the device in Normal Mode
2	GND	System ground (optional)
3	NTRIG	Low-level watchdog trigger input from microcontroller
4	WAKE	High-voltage input for local wake-up request; if not needed, connect directly to VS
5	GND	System ground (mandatory)
6	GND	System ground (optional)
7	LIN	LIN-bus line input/output
8	GND	System ground (optional)
9	RXD	Receive data output
10	INH	Battery related output for controlling an external voltage regulator
11	TXD	Transmit data input; active low output (strong pull down) after a local wake-up request
12	NRES	Output undervoltage and watchdog reset (open drain)
13	WD_OSC	External resistor for adjustable watchdog timing
14	TM	For factory testing only (tie to ground)
15	MODE	Low, watchdog is on; high, watchdog is off; if not needed, connect to GND
16	KL_15	Ignition detection (edge sensitive)
17	GND	System ground (optional)
18	PVCC	3.3V/5V regulator sense input pin
19	VCC	3.3V/5V regulator output/driver pin
20	VS	Battery supply
Backside		Heat slug is connected to all GND pins

3. Functional Description

3.1 Physical Layer Compatibility

Since the LIN physical layer is independent from higher LIN layers (e.g., the LIN protocol layer), all nodes with a LIN physical layer according to revision 2.x can be mixed with LIN physical layer nodes, which, according to older versions (i.e., LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3), are without any restrictions.

3.2 Supply Pin (VS)

The LIN operating voltage is V_S = 5V to 27V. An undervoltage detection is implemented to disable data transmission if V_S falls below VS_{th} < 4V in order to avoid false bus messages. After switching on VS, the IC starts in Fail-safe Mode, and the voltage regulator is switched on.

The supply current is typically 10µA in Sleep Mode and 57µA in Silent Mode.

3.3 Ground Pin (GND)

The IC does not affect the LIN Bus in the event of GND disconnection. It is able to handle a ground shift up to 11.5% of VS. The mandatory system ground is pin 5.

3.4 Voltage Regulator Output Pin (VCC)

The internal 3.3V/5V voltage regulator is capable of driving loads up to 85mA. It is able to supply the microcontroller and other ICs on the PCB and is protected against overloads by means of current limitation and overtemperature shut-down. Furthermore, the output voltage is monitored and will cause a reset signal at the NRES output pin if it drops below a defined threshold V_{thun}. To boost up the maximum load current, an external NPN transistor may be used, with its base connected to the VCC pin and its emitter connected to PVCC.

3.5 Voltage Regulator Sense Pin (PVCC)

The PVCC is the sense input pin of the 3.3V/5V voltage regulator. For normal applications (i.e., when only using the internal output transistor), this pin is connected to the VCC pin. If an external boosting transistor is used, the PVCC pin must be connected to the output of this transistor, i.e., its emitter terminal.

3.6 Bus Pin (LIN)

A low-side driver with internal current limitation and thermal shutdown and an internal pull-up resistor compliant with the LIN 2.x specification are implemented. The allowed voltage range is between –27V and +40V. Reverse currents from the LIN bus to VS are suppressed, even in the event of GND shifts or battery disconnection. LIN receiver thresholds are compatible with the LIN protocol specification. The fall time from recessive to dominant bus state and the rise time from dominant to recessive bus state are slope controlled.

3.7 Input/Output Pin (TXD)

In Normal Mode the TXD pin is the microcontroller interface used to control the state of the LIN output. TXD must be pulled to ground in order to have a low LIN-bus. If TXD is high or unconnected (internal pull-up resistor), the LIN output transistor is turned off, and the bus is in recessive state. During Fail-safe Mode, this pin is used as output. It is current-limited to < 8mA. and is latched to low if the last wake-up event was from pin WAKE or KL_15.

3.8 TXD Dominant Time-out Function

The TXD input has an internal pull-up resistor. An internal timer prevents the bus line from being driven permanently in dominant state. If TXD is forced to low for longer than t_{DOM} > 6ms, the LIN-bus driver is switched to recessive state.

To reactivate the LIN bus driver, switch TXD to high (> 10µs).

The time-out function is disabled in the ATA6626. Switching to dominant level on the LIN bus occurs without any time limitations.

3.9 Output Pin (RXD)

This output pin reports the state of the LIN-bus to the microcontroller. LIN high (recessive state) is reported by a high level at RXD; LIN low (dominant state) is reported by a low level at RXD. The output has an internal pull-up resistor with typically 5kΩ to VCC. The AC characteristics can be defined with an external load capacitor of 20pF.

The output is short-circuit protected. RXD is switched off in Unpowered Mode (i.e., V_S = 0V).

3.10 Enable Input Pin (EN)

The Enable Input pin controls the operation mode of the device. If EN is high, the circuit is in Normal Mode, with transmission paths from TXD to LIN and from LIN to RXD both active. The VCC voltage regulator operates with 3.3V/5V/85mA output capability.

If EN is switched to low while TXD is still high, the device is forced to Silent Mode. No data transmission is then possible, and the current consumption is reduced to I_{VS} typ. 57µA. The VCC regulator has its full functionality.

If EN is switched to low while TXD is low, the device is forced to Sleep Mode. No data transmission is possible, and the voltage regulator is switched off.

3.11 Wake Input Pin (WAKE)

The Wake Input pin is a high-voltage input used to wake up the device from Sleep Mode or Silent Mode. It is usually connected to an external switch in the application to generate a local wake-up. A pull-up current source, typically 10µA, is implemented.

If a local wake-up is not needed in the application, connect the Wake pin directly to the VS pin.

3.12 Mode Input Pin (MODE)

Connect the MODE pin directly or via an external resistor to GND for normal watchdog operation. To debug the software of the connected microcontroller, connect MODE pin to 3.3V/5V and the watchdog is switched off.

3.13 TM Input Pin

The TM pin is used for final production measurements at Atmel®. In normal application, it has to be always connected to GND.

3.14 KL_15 Pin

The KL_15 pin is a high-voltage input used to wake up the device from Sleep or Silent Mode. It is an edge sensitive pin (low-to-high transition). It is usually connected to ignition to generate a local wake-up in the application when the ignition is switched on. Although KL_15 pin is at high voltage (V_{Batt}), it is possible to switch the IC into Sleep or Silent Mode. Connect the KL_15 pin directly to GND if you do not need it. A debounce timer with a typical Tdb_{KI_15} of 160µs is implemented.

The input voltage threshold can be adjusted by varying the external resistor due to the input current I_{KL_15}. To protect this pin against voltage transients, a serial resistor of 47kΩ and a ceramic capacitor of 100nF are recommended. With this RC combination you can increase the wake-up time Tw_{KL_15} and, therefore, the sensitivity against transients on the ignition KI.15.

You can also increase the wake-up time using external capacitors with higher values.

3.15 INH Output Pin

The INH Output pin is used to switch an external voltage regulator on during Normal or Fail-safe Mode. The INH pin is switched off in Sleep or Silent Mode. It is possible to switch off the external 1kΩ master resistor via the INH pin for master node applications. The INH pin is switched off during VCC undervoltage reset.

3.16 Reset Output Pin (NRES)

The Reset Output pin, an open drain output, switches to low during V_{CC} undervoltage or a watchdog failure.

3.17 WD_OSC Output Pin

The WD_OSC Output pin provides a typical voltage of 1.2V, which supplies an external resistor with values between 34kΩ and 120kΩ to adjust the watchdog oscillator time.

3.18 NTRIG Input Pin

The NTRIG Input pin is the trigger input for the window watchdog. A pull-up resistor is implemented. A negative edge triggers the watchdog. The trigger signal (low) must exceed a minimum time $t_{trigmin}$ to generate a watchdog trigger.

3.19 Wake-up Events from Sleep or Silent Mode

- LIN-bus
- WAKE pin
- EN pin
- KL_15

4. Modes of Operation

Figure 4-1. Modes of Operation

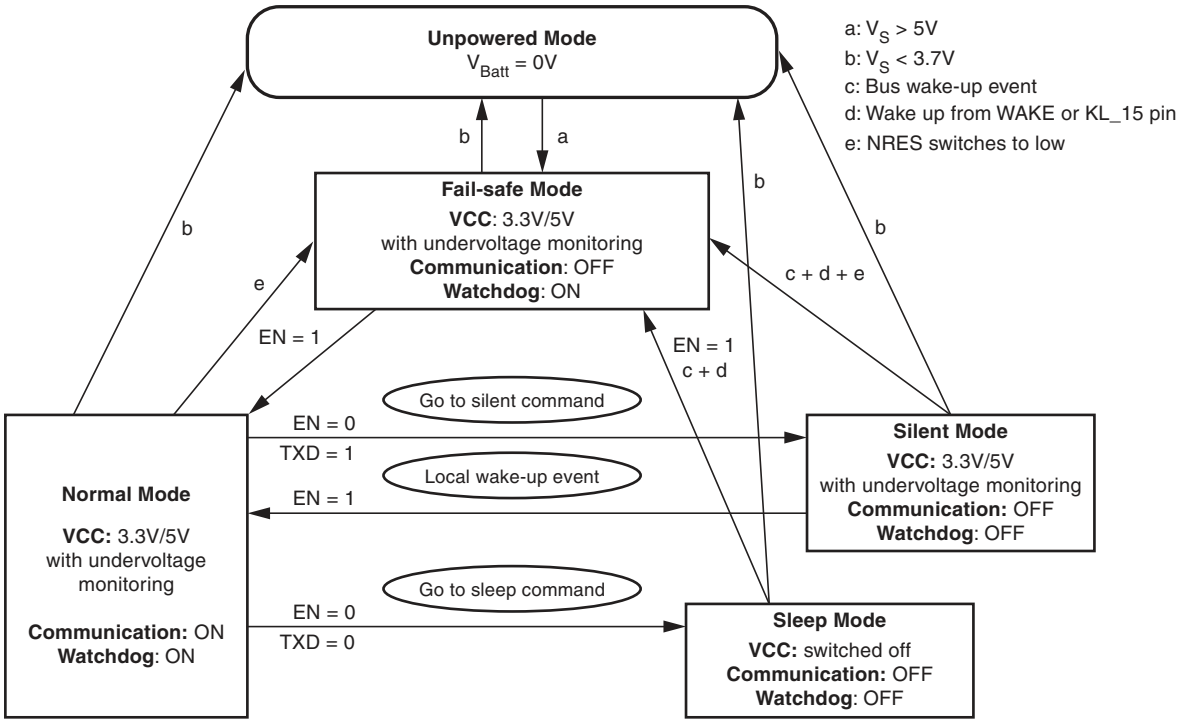


Table 4-1. Table of Modes

Mode of Operation	Transceiver	VCC	Watchdog	WD_OSC	INH	RXD	LIN
Fail-safe	Off	3.3V/5V	On	1.23V	On	High, except after wake-up	Recessive
Normal	On	3.3V/5V	On	1.23V	On	LIN depending	TXD depending
Silent	Off	3.3V/5V	Off	0V	Off	High	Recessive
Sleep	Off	0V	Off	0V	Off	0V	Recessive

4.1 Normal Mode

This is the normal transmitting and receiving mode of the LIN Interface in accordance with the LIN specification LIN 2.x. The voltage regulator is active and can source up to 85mA. The undervoltage detection is activated. The watchdog needs a trigger signal from NTRIG to avoid resets at NRES. If NRES is switched to low, the IC changes its state to Fail-safe Mode.

4.2 Silent Mode

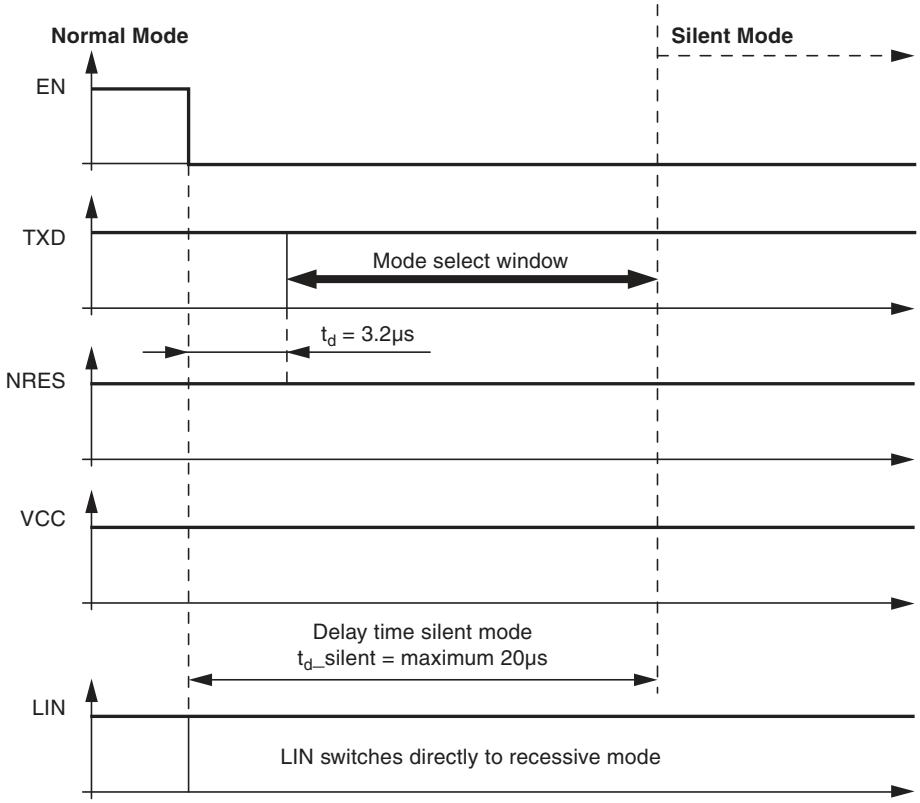
A falling edge at EN when TXD is high switches the IC into Silent Mode. The TXD Signal has to be logic high during the Mode Select window (see Figure 4-2 on page 8). The transmission path is disabled in Silent Mode. The overall supply current from V_{Batt} is a combination of the I_{VSsi} = 57µA plus the VCC regulator output current I_{VCC}.

The internal slave termination between the LIN pin and the VS pin is disabled in Silent Mode, only a weak pull-up current (typically 10µA) between the LIN pin and the VS pin is present. Silent Mode can be activated independently from the actual level on the LIN, WAKE, or KL_15 pins.

If an undervoltage condition occurs, NRES is switched to low, and the IC changes its state to Fail-safe Mode.

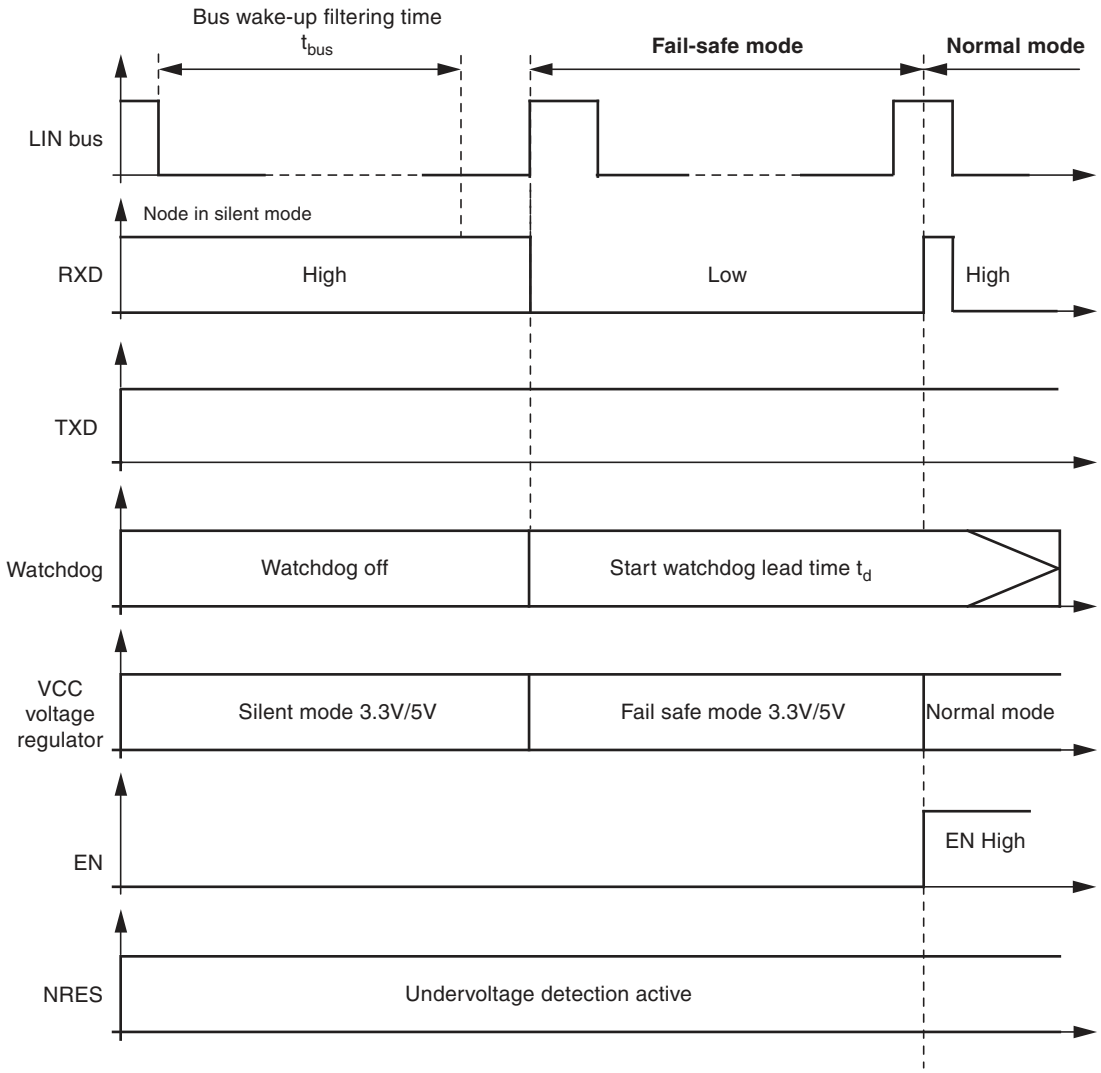
A voltage less than the LIN Pre_Wake detection VLINL at the LIN pin activates the internal LIN receiver and switches on the internal slave termination between the LIN pin and the V_S pin.

Figure 4-2. Switch to Silent Mode



A falling edge at the LIN pin followed by a dominant bus level maintained for a certain time period (> t_{bus}) and the following rising edge at the LIN pin (see Figure 4-3 on page 9) results in a remote wake-up request. The device switches from Silent Mode to Fail-safe Mode. The remote wake-up request is indicated by a low level at the RXD pin to interrupt the microcontroller (see Figure 4-3 on page 9). EN high can be used to switch directly to Normal Mode.

Figure 4-3. LIN Wake Up from Silent Mode



4.3 Sleep Mode

A falling edge at EN when TXD is low switches the IC into Sleep Mode. The TXD Signal has to be logic low during the Mode Select window (Figure 4-4 on page 10). In order to avoid any influence to the LIN-pin during switching into sleep mode it is possible to switch the EN up to 3.2 µs earlier to LOW than the TXD. Therefore, the best and easiest way are two falling edges at TXD and EN at the same time.The transmission path is disabled in Sleep Mode. The supply current $I_{VSsleep}$ from V_{Batt} is typically 10 µA.

The VCC regulator is switched off. NRES and RXD are low. The internal slave termination between the LIN pin and VS pin is disabled, only a weak pull-up current (typically 10µA) between the LIN pin and the VS pin is present. Sleep Mode can be activated independently from the current level on the LIN, WAKE, or KL_15 pin.

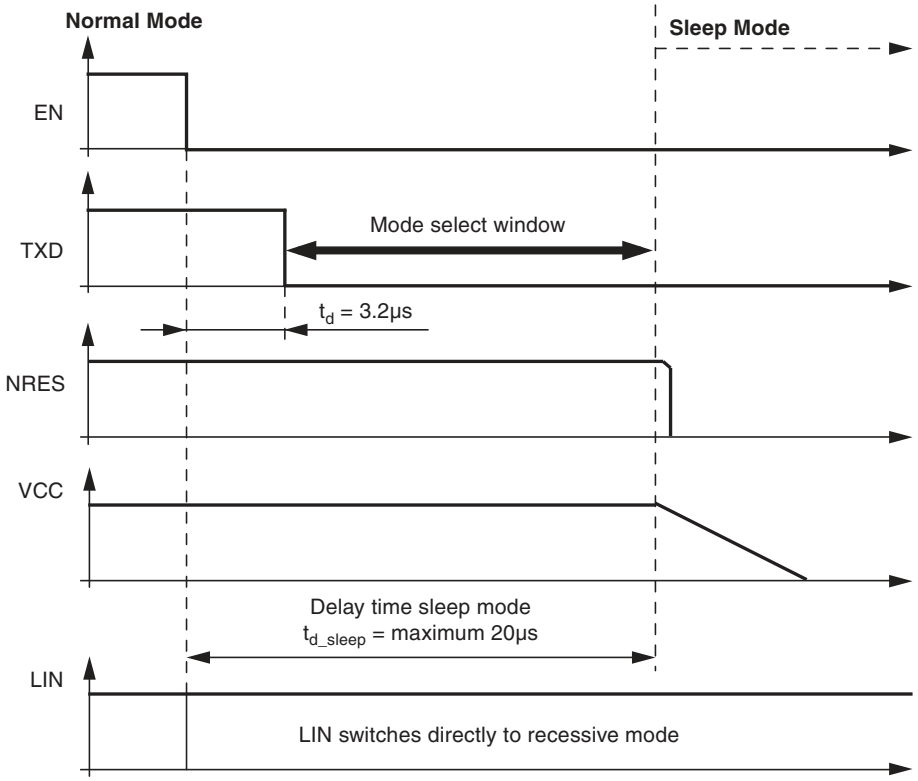
A voltage less than the LIN Pre_Wake detection VLINL at the LIN pin activates the internal LIN receiver and switches on the internal slave termination between the LIN pin and the V_S pin.

A falling edge at the LIN pin followed by a dominant bus level maintained for a certain time period (> t_{bus}) and a following rising edge at pin LIN results in a remote wake-up request. The device switches from Sleep Mode to Fail-safe Mode.

The VCC regulator is activated, and the remote wake-up request is indicated by a low level at the RXD pin to interrupt the microcontroller (see Figure 4-5 on page 11).

EN high can be used to switch directly from Sleep/Silent to Fail-safe Mode. If EN is still high after VCC ramp up and undervoltage reset time, the IC switches to the Normal Mode.

Figure 4-4. Switch to Sleep Mode



4.4 Fail-safe Mode

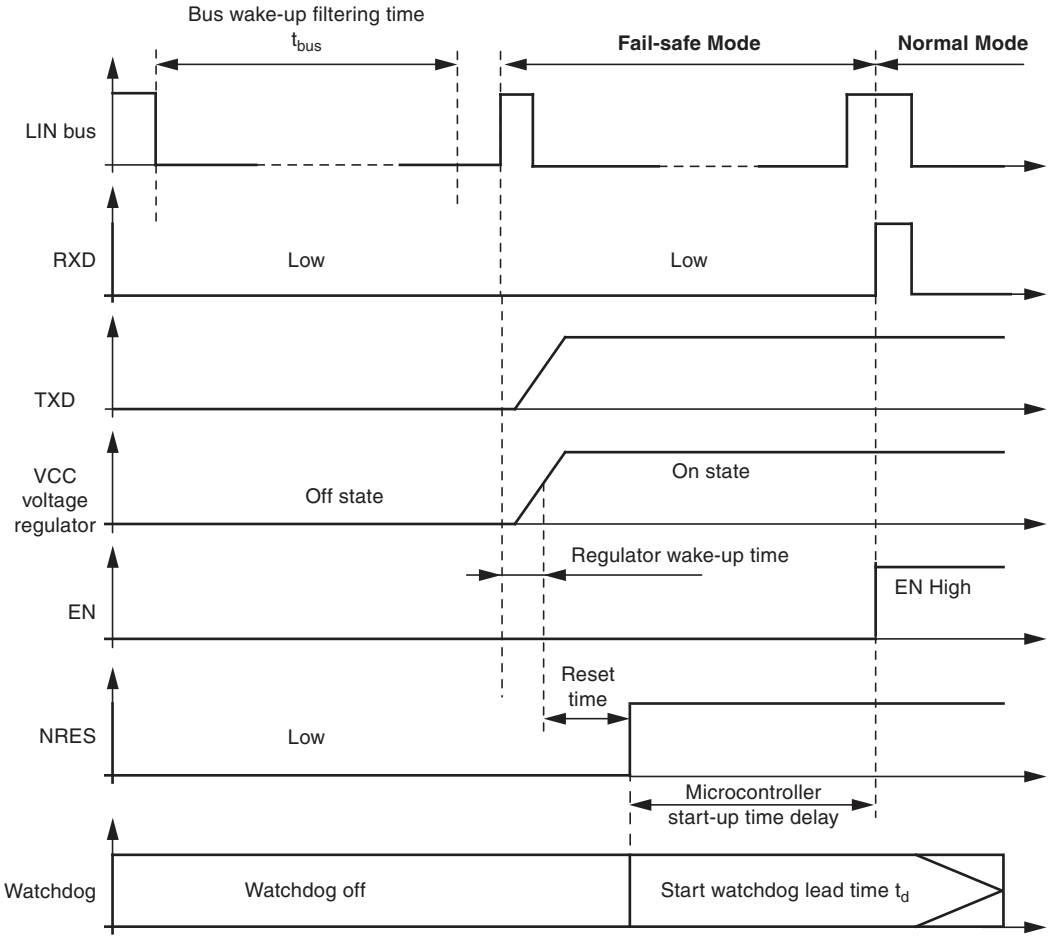
The device automatically switches to Fail-safe Mode at system power-up. The voltage regulator is switched on (see Figure 5-1 on page 14). The NRES output switches to low for t_{res} = 4ms and gives a reset to the microcontroller. LIN communication is switched off. The IC stays in this mode until EN is switched to high. The IC then changes to Normal Mode. A power down of V_{Batt} (V_S < 3.7V) during Silent or Sleep Mode switches the IC into Fail-safe Mode after power up. A low at NRES switches into Fail-safe Mode directly. During Fail-safe Mode the TXD pin is an output and signals the last wake-up source.

4.5 Unpowered Mode

If you connect battery voltage to the application circuit, the voltage at the VS pin increases according to the block capacitor (see Figure 5-1 on page 14). After VS is higher than the VS undervoltage threshold VS_{th}, the IC mode changes from Unpowered Mode to Fail-safe Mode. The VCC output voltage reaches its nominal value after t_{VCC}. This time, t_{VCC}, depends on the VCC capacitor and the load.

The NRES is low for the reset time delay t_{reset}. During this time, t_{reset}, no mode change is possible.

Figure 4-5. LIN Wake Up from Sleep Mode



5. Wake-up Scenarios from Silent or Sleep Mode

5.1 Remote Wake-up via Dominant Bus State

A voltage less than the LIN Pre_Wake detection V_{LINL} at the LIN pin activates the internal LIN receiver.

A falling edge at the LIN pin followed by a dominant bus level V_{BUSdom} maintained for a certain time period (> t_{BUS}) and a rising edge at pin LIN result in a remote wake-up request. The device switches from Silent or Sleep Mode to Fail-safe Mode. The VCC voltage regulator is/remains activated, the INH pin is switched to high, and the remote wake-up request is indicated by a low level at the RXD pin to generate an interrupt for the microcontroller. A low level at the LIN pin in the Normal Mode starts the bus wake-up filtering time, and if the IC is switched to Silent or Sleep Mode, it will receive a wake-up after a positive edge at the LIN pin.

5.2 Local Wake-up via Pin WAKE

A falling edge at the WAKE pin followed by a low level maintained for a certain time period (> t_{WAKE}) results in a local wake-up request. The device switches to Fail-safe Mode. The local wake-up request is indicated by a low level at the RXD pin to generate an interrupt in the microcontroller and a strong pull down at TXD. When the Wake pin is low, it is possible to switch to Silent or Sleep Mode via pin EN. In this case, the wake-up signal has to be switched to high > 10µs before the negative edge at WAKE starts a new local wake-up request.

5.3 Local Wake-up via Pin KL_15

A positive edge at pin KL_15 followed by a high voltage level for a certain time period (> t_{KL_15}) results in a local wake-up request. The device switches into the Fail-safe Mode. The extra long wake-up time ensures that no transients at KL_15 create a wake up. The local wake-up request is indicated by a low level at the RXD pin to generate an interrupt for the microcontroller and a strong pull down at TXD. During high-level voltage at pin KL_15, it is possible to switch to Silent or Sleep Mode via pin EN. In this case, the wake-up signal has to be switched to low > 250µs before the positive edge at KL_15 starts a new local wake-up request. With external RC combination, the time is even longer.

5.4 Wake-up Source Recognition

The device can distinguish between a local wake-up request (Wake or KL_15 pins) and a remote wake-up request (dominant LIN bus state). The wake-up source can be read on the TXD pin in Fail-safe Mode. A high level indicates a remote wake-up request (weak pull up at the TXD pin); a low level indicates a local wake-up request (strong pull down at the TXD pin). The wake-up request flag (signalled on the RXD pin), as well as the wake-up source flag (signalled on the TXD pin), is immediately reset if the microcontroller sets the EN pin to high (see Figure 4-2 on page 8 and Figure 4-3 on page 9) and the IC is in Normal Mode. The last wake-up source flag is stored and signalled in Fail-safe Mode at the TXD pin.

5.5 Fail-safe Features

- During a short-circuit at LIN to $V_{Battery}$, the output limits the output current to I_{BUS_lim}. Due to the power dissipation, the chip temperature exceeds T_{LINoff}, and the LIN output is switched off. The chip cools down and after a hysteresis of T_{hys}, switches the output on again. RXD stays on high because LIN is high. During LIN overtemperature switch-off, the VCC regulator works independently.
- During a short-circuit from LIN to GND the IC can be switched into Sleep or Silent Mode. If the short-circuit disappears, the IC starts with a remote wake-up.
- The reverse current is very low < 2µA at the LIN pin during loss of V_{Batt}. This is optimal behavior for bus systems where some slave nodes are supplied from battery or ignition.
- During a short circuit at VCC, the output limits the output current to I_{VCClim}. Because of undervoltage, NRES switches to low and sends a reset to the microcontroller. The IC switches into Fail-safe Mode. If the chip temperature exceeds the value T_{VCCoff}, the VCC output switches off. The chip cools down and after a hysteresis of T_{hys}, switches the output on again. Because of the Fail-safe Mode, the VCC voltage will switch on again although EN is switched off from the microcontroller. The microcontroller can start with its normal operation.
- EN pin provides a pull-down resistor to force the transceiver into recessive mode if EN is disconnected.
- RXD pin is set floating if V_{Batt} is disconnected.
- TXD pin provides a pull-up resistor to force the transceiver into recessive mode if TXD is disconnected.
- If TXD is short-circuited to GND, it is possible to switch to Sleep Mode via ENABLE after t_{dom} > 20ms (only for Atmel® ATA6622/ATA6624).
- If the WD_OSC pin has a short-circuit to GND and the NTRIG Signal has a period time > 27ms, the watchdog runs with an internal oscillator and guarantees a reset after the second NTRIG signal at the latest.
- If the resistor at WO_OSC pin is disconnected, the watchdog runs with an internal oscillator and guarantees a reseet after the second NTRIG signal at the latest.

5.6 Voltage Regulator

The voltage regulator needs an external capacitor for compensation and for smoothing the disturbances from the microcontroller. It is recommended to use an electrolythic capacitor with C > 1.8µF and a ceramic capacitor with C = 100nF. The values of these capacitors can be varied by the customer, depending on the application.

The main power dissipation of the IC is created from the VCC output current I_{VCC}, which is needed for the application. In Figure 5-2 on page 14 the safe operating area of the Atmel ATA6624/ATA6626 is shown.

Figure 5-1. VCC Voltage Regulator: Ramp-up and Undervoltage Detection

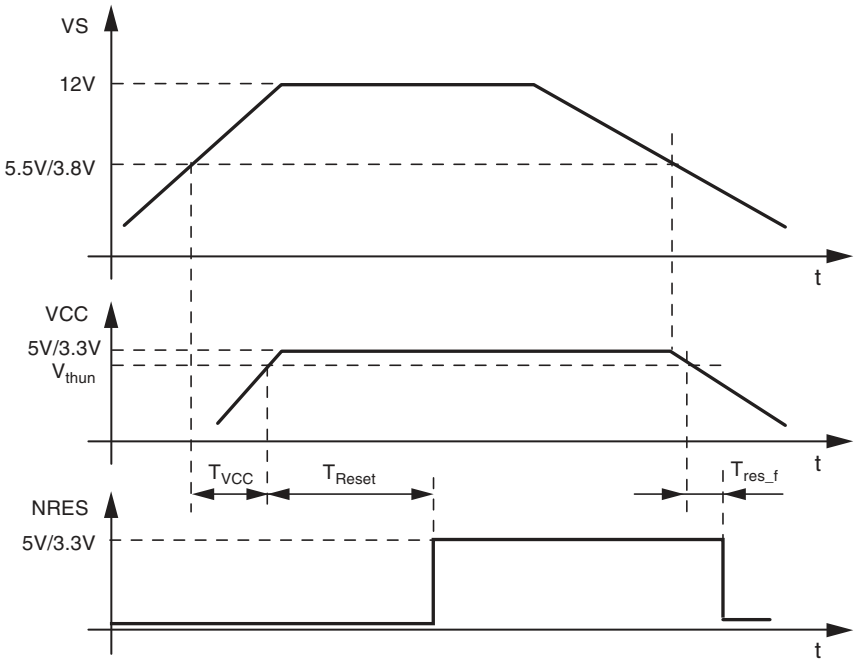
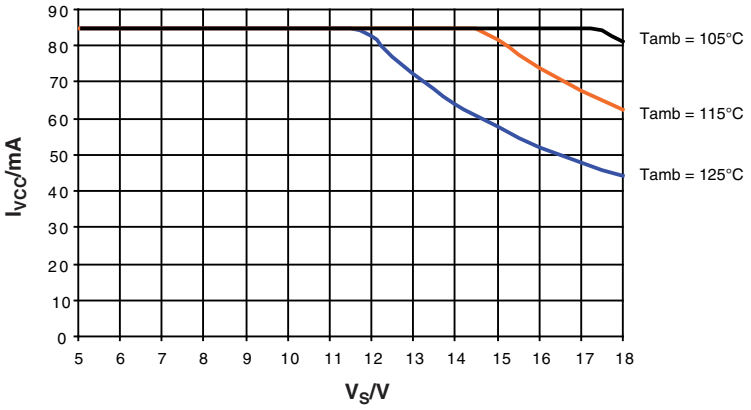


Figure 5-2. Power Dissipation: Safe Operating Area: VCC Output Current versus Supply Voltage V_S at Different Ambient Temperatures Due to R_{thja} = 35K/W



For programming purposes of the microcontroller it is potentially necessary to supply the V_{CC} output via an external power supply while the V_S Pin of the system basis chip is disconnected. This will not affect the system basis chip.

6. Watchdog

The watchdog anticipates a trigger signal from the microcontroller at the NTRIG (negative edge) input within a time window of T_{wd}. The trigger signal must exceed a minimum time $t_{trigmin}$ > 200ns. If a triggering signal is not received, a reset signal will be generated at output NRES. The timing basis of the watchdog is provided by the internal oscillator. Its time period, T_{osc}, is adjustable via the external resistor R_{wd_osc} (34kΩ to 120kΩ).

During Silent or Sleep Mode the watchdog is switched off to reduce current consumption.

The minimum time for the first watchdog pulse is required after the undervoltage reset at NRES disappears. It is defined as lead time t_d. After wake up from Sleep or Silent Mode, the lead time t_d starts with the negative edge of the RXD output.

6.1 Typical Timing Sequence with R_{WD_OSC} = 51kΩ

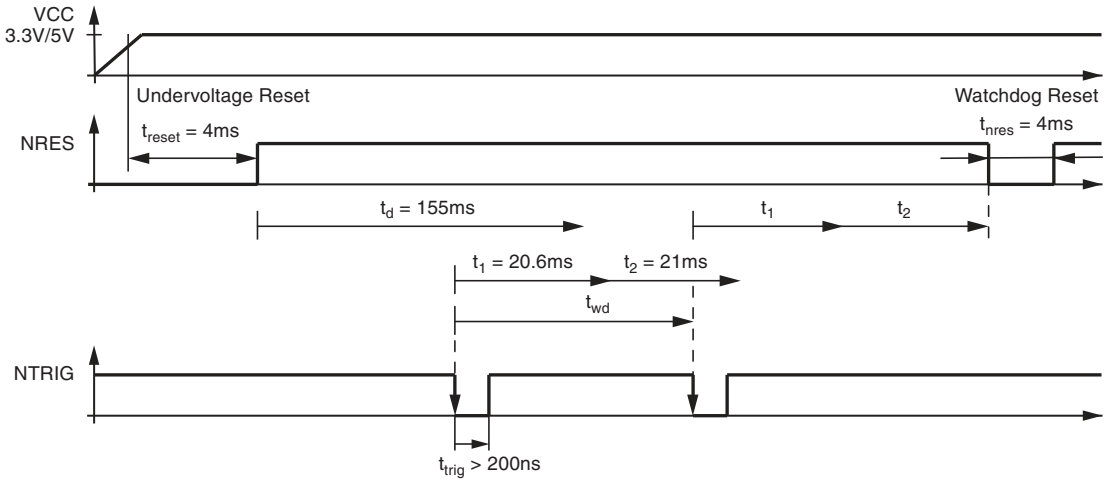
The trigger signal T_{wd} is adjustable between 20ms and 64ms using the external resistor R_{WD_OSC}.

For example, with an external resistor of R_{WD_OSC} = 51kΩ ±1%, the typical parameters of the watchdog are as follows:

$t_{osc} = 0.405 \times R_{WD\_OSC} - 0.0004 \times (R_{WD\_OSC})^2$ (R_{WD_OSC} in kΩ; t_{osc} in µs)
t_{OSC} = 19.6µs due to 51kΩ
$t_d = 7895 \times 19.6\mu s = 155ms$
$t_1 = 1053 \times 19.6\mu s = 20.6ms$
$t_2 = 1105 \times 19.6\mu s = 21.6ms$
t_{nres} = constant = 4ms

After ramping up the battery voltage, the 3.3V/5V regulator is switched on. The reset output NRES stays low for the time t_{reset} (typically 4ms), then it switches to high, and the watchdog waits for the trigger sequence from the microcontroller. The lead time, t_d, follows the reset and is t_d = 155ms. In this time, the first watchdog pulse from the microcontroller is required. If the trigger pulse NTRIG occurs during this time, the time t_1 starts immediately. If no trigger signal occurs during the time t_d, a watchdog reset with t_{NRES} = 4ms will reset the microcontroller after t_d = 155ms. The times t_1 and t_2 have a fixed relationship between each other. A triggering signal from the microcontroller is anticipated within the time frame of t_2 = 21.6ms. To avoid false triggering from glitches, the trigger pulse must be longer than $t_{TRIG,min}$ > 200ns. This slope serves to restart the watchdog sequence. If the triggering signal fails in this open window t_2, the NRES output will be drawn to ground. A triggering signal during the closed window t_1 immediately switches NRES to low.

Figure 6-1. Timing Sequence with R_{WD_OSC} = 51kΩ



6.2 Worst Case Calculation with R_{WD_OSC} = 51kΩ

The internal oscillator has a tolerance of 20%. This means that t_1 and t_2 can also vary by 20%. The worst case calculation for the watchdog period t_{wd} is calculated as follows.

The ideal watchdog time t_{wd} is between the maximum t_1 and the minimum t_1 plus the minimum t_2.

$t_{1,min} = 0.8 \times t_1 = 16.5ms$, $t_{1,max} = 1.2 \times t_1 = 24.8ms$
$t_{2,min} = 0.8 \times t_2 = 17.3ms$, $t_{2,max} = 1.2 \times t_2 = 26ms$

$t_{wdmax} = t_{1min} + t_{2min} = 16.5ms + 17.3ms = 33.8ms$
$t_{wdmin} = t_{1max} = 24.8ms$

$t_{wd} = 29.3ms \pm 4.5ms$ (±15%)

A microcontroller with an oscillator tolerance of ±15% is sufficient to supply the trigger inputs correctly.

Table 6-1. Typical Watchdog Timings

R_{WD_OSC} kΩ	Oscillator Period t_{osc}/µs	Lead Time t_d/ms	Closed Window t_1/ms	Open Window t_2/ms	Trigger Period from Microcontroller t_{wd}/ms	Reset Time t_{nres}/ms
34	13.3	105	14.0	14.7	19.9	4
51	19.61	154.8	20.64	21.67	29.32	4
91	33.54	264.80	35.32	37.06	50.14	4
120	42.84	338.22	45.11	47.34	64.05	4

7. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage V_S	V_S	–0.3		+40	V
Pulse time ≤ 500ms; T_a = 25°C Output current I_{VCC} ≤ 85mA	V_S			+40	V
Pulse time ≤ 2min; T_a = 25°C Output current I_{VCC} ≤ 85mA	V_S			27	V
WAKE (with 33kΩ serial resistor) KL_15 (with 47kΩ/100nF) DC voltage Transient voltage due to ISO7637 (coupling 1nF)		 –1 –150		 +40 +100	 V V
INH - DC voltage		 –0.3		 V_S + 0.3	 V
LIN - DC voltage		 –27		 +40	 V
Logic pins (RxD, TxD, EN, NRES, NTRIG, WD_OSC, MODE, TM)		–0.3		+5.5	V
Output current NRES	I_{NRES}			+2	mA
PVCC DC voltage VCC DC voltage		–0.3 –0.3		+5.5 +6.5	V V
ESD according to IBEE LIN EMC Test Spec. 1.0 following IEC 61000-4-2 - Pin VS, LIN, KL_15 (47kΩ/100nF) to GND - Pin WAKE (33 kΩ serial resistor) to GND		 ±6 ±5			 KV KV
ESD HBM following STM5.1 with 1.5kΩ 100pF - Pin VS, LIN, KL_15, WAKE to GND		±6			KV
HBM ESD ANSI/ESD-STM5.1 JESD22-A114 AEC-Q100 (002)		±3			KV
CDM ESD STM 5.3.1		±750			V
Machine Model ESD AEC-Q100-RevF(003)		±200			V
Junction temperature	T_j	–40		+150	°C
Storage temperature	T_s	–55		+150	°C

8. Thermal Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance junction to heat slug	R_{thjc}			10	K/W
Thermal resistance junction to ambient, where heat slug is soldered to PCB	R_{thja}		35		K/W
Thermal shutdown of VCC regulator		150	165	170	°C
Thermal shutdown of LIN output		150	165	170	°C
Thermal shutdown hysteresis			10		°C

9. Electrical Characteristics

5V < V_S < 27V, -40°C < Tj < 150°C, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**VS Pin**								
1.1	Nominal DC voltage range		VS	V_S	5		27	V	A
1.2	Supply current in Sleep Mode	Sleep Mode $V_{LIN} > V_S - 0.5V$ $V_S < 14V$ ($T_j = 25°C$)	VS	$I_{VSsleep}$	3	10	14	µA	B
		Sleep Mode $V_{LIN} > V_S - 0.5V$ $V_S < 14V$ ($T_j = 125°C$)	VS	$I_{VSsleep}$	5	11	16	µA	A
1.3	Supply current in Silent Mode	Bus recessive $V_S < 14V$ ($T_j = 25°C$) Without load at VCC	VS	I_{VSsi}	47	57	67	µA	B
		Bus recessive $V_S < 14V$ ($T_j = 125°C$) Without load at VCC	VS	I_{VSsi}	56	66	76	µA	A
1.4	Supply current in Normal Mode	Bus recessive $V_S < 14V$ Without load at VCC	VS	I_{VSrec}	0.3		0.8	mA	A
1.5	Supply current in Normal Mode	Bus dominant $V_S < 14V$ V_{CC} load current 50 mA	VS	I_{VSdom}	50		53	mA	A
1.6	Supply current in Fail-safe Mode	Bus recessive $V_S < 14V$ Without load at VCC	VS	I_{VSfail}	250		550	µA	A
1.7	V_S undervoltage threshold		VS	V_{Sth}	3.7	4.4	5	V	A
1.8	VS undervoltage threshold hysteresis		VS	V_{Sth_hys}		0.2		V	A
2	**RXD Output Pin**								
2.1	Low-level output sink current	Normal Mode $V_{LIN} = 0V$ $V_{RXD} = 0.4V$	RXD	I_{RXD}	1.3	2.5	8	mA	A
2.2	Low-level output voltage	I_{RXD} = 1mA	RXD	V_{RXDL}			0.4	V	A
2.3	Internal resistor to V_{CC}		RXD	R_{RXD}	3	5	7	kΩ	A
3	**TXD Input/Output Pin**								
3.1	Low-level voltage input		TXD	V_{TXDL}	–0.3		+0.8	V	A
3.2	High-level voltage input		TXD	V_{TXDH}	2		V_{CC} + 0.3V	V	A
3.3	Pull-up resistor	V_{TXD} = 0V	TXD	R_{TXD}	125	250	400	kΩ	A
3.4	High-level leakage current	V_{TXD} = VCC	TXD	I_{TXD}	–3		+3	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

9. Electrical Characteristics (Continued)

5V < V_S < 27V, -40°C < Tj < 150°C, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3.5	Low-level output sink current at local wake-up request	Fail-safe Mode $V_{LIN} = V_S$ V_{WAKE} = 0V V_{TXD} = 0.4V	TXD	$I_{TXDwake}$	2	2.5	8	mA	A
4	**EN Input Pin**								
4.1	Low-level voltage input		EN	V_{ENL}	–0.3		+0.8	V	A
4.2	High-level voltage input		EN	V_{ENH}	2		V_{CC} + 0.3V	V	A
4.3	Pull-down resistor	$V_{EN} = V_{CC}$	EN	R_{EN}	50	125	200	kΩ	A
4.4	Low-level input current	V_{EN} = 0V	EN	I_{EN}	–3		+3	µA	A
5	**NTRIG Watchdog Input Pin**								
5.1	Low-level voltage input		NTRIG	V_{NTRIGL}	–0.3		+0.8	V	A
5.2	High-level voltage input		NTRIG	V_{NTRIGH}	2		V_{CC} + 0.3V	V	A
5.3	Pull-up resistor	V_{NTRIG} = 0V	NTRIG	R_{NTRIG}	125	250	400	kΩ	A
5.4	High-level leakage current	$V_{NTRIG} = V_{CC}$	NTRIG	I_{NTRIG}	–3		+3	µA	A
6	**Mode Input Pin**								
6.1	Low-level voltage input		MODE	V_{MODEL}	–0.3		+0.8	V	A
6.2	High-level voltage input		MODE	V_{MODEH}	2		V_{CC} + 0.3V	V	A
6.3	Leakage current	$V_{MODE} = V_{CC}$ or V_{MODE} = 0V	MODE	I_{MODE}	–3		+3	µA	A
7	**INH Output Pin**								
7.1	High-level voltage	I_{INH} = –15mA	INH	V_{INHH}	V_S – 0.75		V_S	V	A
7.2	Switch-on resistance between VS and INH		INH	R_{INH}		30	50	Ω	A
7.3	Leakage current	Sleep Mode V_{INH} = 0V/27V, V_S = 27V	INH	I_{INHL}	–3		+3	µA	A
8	**LIN Bus Driver: Bus Load Conditions:** **Load 1 (Small): 1nF, 1kΩ; Load 2 (Large): 10nF, 500Ω; Internal Pull-up R_{RXD} = 5kΩ; C_{RXD} = 20pF** **Load 3 (Medium): 6.8nF, 660Ω, Characterized on Samples** **10.6 and 10.7 Specifies the Timing Parameters for Proper Operation at 20kBit/s and 10.8 and 10.9 at 10.4kBit/s**								
8.1	Driver recessive output voltage	Load1/Load2	LIN	V_{BUSrec}	0.9 × V_S		V_S	V	A
8.2	Driver dominant voltage	V_{VS} = 7V R_{load} = 500Ω	LIN	$V_{\_LoSUP}$			1.2	V	A
8.3	Driver dominant voltage	V_{VS} = 18V R_{load} = 500Ω	LIN	$V_{\_HiSUP}$			2	V	A
8.4	Driver dominant voltage	V_{VS} = 7.0V R_{load} = 1000Ω	LIN	$V_{\_LoSUP\_1k}$	0.6			V	A
8.5	Driver dominant voltage	V_{VS} = 18V R_{load} = 1000Ω	LIN	$V_{\_HiSUP\_1k}$	0.8			V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

9. Electrical Characteristics (Continued)

5V < V_S < 27V, -40°C < Tj < 150°C, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.6	Pull-up resistor to V_S	The serial diode is mandatory	LIN	R_{LIN}	20	30	60	kΩ	A
8.7	Voltage drop at the serial diodes	In pull-up path with R_{slave} $I_{SerDiode}$ = 10mA	LIN	$V_{SerDiode}$	0.4		1.0	V	D
8.8	LIN current limitation $V_{BUS} = V_{Batt\_max}$		LIN	I_{BUS_LIM}	40	120	200	mA	A
8.9	Input leakage current at the receiver including pull-up resistor as specified	Input leakage current Driver off V_{BUS} = 0V V_{Batt} = 12V	LIN	$I_{BUS\_PAS\_dom}$	–1	–0.35		mA	A
8.10	Leakage current LIN recessive	Driver off 8V < V_{Batt} < 18V 8V < V_{BUS} < 18V $V_{BUS} \geq V_{Batt}$	LIN	$I_{BUS\_PAS\_rec}$		10	20	µA	A
8.11	Leakage current when control unit disconnected from ground. Loss of local ground must not affect communication in the residual network.	$GND_{Device} = V_S$ V_{Batt} = 12V 0V < V_{BUS} < 18V	LIN	$I_{BUS\_NO\_gnd}$	–10	+0.5	+10	µA	A
8.12	Leakage current at a disconnected battery. Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition.	V_{Batt} disconnected V_{SUP_Device} = GND 0V < V_{BUS} < 18V	LIN	$I_{BUS\_NO\_bat}$		0.1	2	µA	A
8.13	Capacitance on pin LIN to GND		LIN	C_{LIN}			20	pF	D
9	**LIN Bus Receiver**								
9.1	Center of receiver threshold	V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2	LIN	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	A
9.2	Receiver dominant state	V_{EN} = 5V	LIN	V_{BUSdom}			0.4 × V_S	V	A
9.3	Receiver recessive state	V_{EN} = 5V	LIN	V_{BUSrec}	0.6 × V_S			V	A
9.4	Receiver input hysteresis	$V_{hys} = V_{th\_rec} - V_{th\_dom}$	LIN	V_{BUShys}	0.028 × V_S	0.1 × V_S	0.175 × V_S	V	A
9.5	Pre_Wake detection LIN High-level input voltage		LIN	V_{LINH}	V_S – 2V		V_S + 0.3V	V	A
9.6	Pre_Wake detection LIN Low-level input voltage	Activates the LIN receiver	LIN	V_{LINL}	–27		V_S – 3.3V	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

9. Electrical Characteristics (Continued)

5V < V_S < 27V, -40°C < Tj < 150°C, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10	**Internal Timers**								
10.1	Dominant time for wake-up via LIN bus	V_{LIN} = 0V	LIN	t_{bus}	30	90	150	µs	A
10.2	Time delay for mode change from Fail-safe into Normal Mode via EN pin	V_{EN} = 5V	EN	t_{norm}	5	15	20	µs	A
10.3	Time delay for mode change from Normal Mode to Sleep Mode via EN pin	V_{EN} = 0V	EN	t_{sleep}	2	7	12	µs	A
10.4	TXD dominant time-out time (ATA6626 disabled)	V_{TXD} = 0V	TXD	t_{dom}	6	13	20	ms	A
10.5	Time delay for mode change from Silent Mode into Normal Mode via EN	V_{EN} = 5V	EN	t_{s_n}	5	15	40	µs	A
10.6	Duty cycle 1	$TH_{Rec(max)} = 0.744 \times V_S$ $TH_{Dom(max)} = 0.581 \times V_S$ V_S = 7.0V to 18V t_{Bit} = 50µs $D1 = t_{bus\_rec(min)}/(2 \times t_{Bit})$	LIN	D1	0.396				A
10.7	Duty cycle 2	$TH_{Rec(min)} = 0.422 \times V_S$ $TH_{Dom(min)} = 0.284 \times V_S$ V_S = 7.6V to 18V t_{Bit} = 50µs $D2 = t_{bus\_rec(max)}/(2 \times t_{Bit})$	LIN	D2			0.581		A
10.8	Duty cycle 3	$TH_{Rec(max)} = 0.778 \times V_S$ $TH_{Dom(max)} = 0.616 \times V_S$ V_S = 7.0V to 18V t_{Bit} = 96µs $D3 = t_{bus\_rec(min)}/(2 \times t_{Bit})$	LIN	D3	0.417				A
10.9	Duty cycle 4	$TH_{Rec(min)} = 0.389 \times V_S$ $TH_{Dom(min)} = 0.251 \times V_S$ V_S = 7.6V to 18V t_{Bit} = 96µs $D4 = t_{bus\_rec(max)}/(2 \times t_{Bit})$	LIN	D4			0.590		A
10.10	Slope time falling and rising edge at LIN	V_S = 7.0V to 18V	LIN	t_{SLOPE_fall} t_{SLOPE_rise}	3.5		22.5	µs	A

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9. Electrical Characteristics (Continued)

5V < V_S < 27V, -40°C < Tj < 150°C, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
11	**Receiver Electrical AC Parameters of the LIN Physical Layer LIN Receiver, RXD Load Conditions: C_{RXD} = 20pF**								
11.1	Propagation delay of receiver (Figure 9-1 on page 25)	V_S = 7.0V to 18V $t_{rx\_pd} = max(t_{rx\_pdr}, t_{rx\_pdf})$	RXD	t_{rx_pd}			6	µs	A
11.2	Symmetry of receiver propagation delay rising edge minus falling edge	V_S = 7.0V to 18V $t_{rx\_sym} = t_{rx\_pdr} - t_{rx\_pdf}$	RXD	t_{rx_sym}	–2		+2	µs	A
12	**NRES Open Drain Output Pin**								
12.1	Low-level output voltage	$V_S \geq 5.5V$ I_{NRES} = 1mA	NRES	V_{NRESL}			0.14	V	A
12.2	Low-level output low	10kΩ to 5V V_{CC} = 0V	NRES	V_{NRESLL}			0.14	V	A
12.3	Undervoltage reset time	$V_S \geq 5.5V$ C_{NRES} = 20pF	NRES	t_{reset}	2	4	6	ms	A
12.4	Reset debounce time for falling edge	$V_S \geq 5.5V$ C_{NRES} = 20pF	NRES	t_{res_f}	1.5		10	µs	A
13	**Watchdog Oscillator**								
13.1	Voltage at WD_OSC in Normal Mode	I_{WD_OSC} = –200µA $V_{VS} \geq 4V$	WD_OSC	V_{WD_OSC}	1.13	1.23	1.33	V	A
13.2	Possible values of resistor		WD_OSC	R_{OSC}	34		120	kΩ	A
13.3	Oscillator period	R_{OSC} = 34kΩ		t_{OSC}	10.65	13.3	15.97	µs	A
13.4	Oscillator period	R_{OSC} = 51kΩ		t_{OSC}	15.68	19.6	23.52	µs	A
13.5	Oscillator period	R_{OSC} = 91kΩ		t_{OSC}	26.83	33.5	40.24	µs	A
13.6	Oscillator period	R_{OSC} = 120kΩ		t_{OSC}	34.2	42.8	51.4	µs	A
14	**Watchdog Timing Relative to t_{osc}**								
14.1	Watchdog lead time after Reset			t_d		7895		cycles	A
14.2	Watchdog closed window			t_1		1053		cycles	A
14.3	Watchdog open window			t_2		1105		cycles	A
14.4	Watchdog reset time NRES		NRES	t_{nres}	3.2	4	4.8	ms	A
15	**KL_15 Pin**								
15.1	High-level input voltage R_V = 47kΩ	Positive edge initializes a wake-up	KL_15	V_{KL_15H}	4		V_S + 0.3V	V	A
15.2	Low-level input voltage R_V = 47kΩ		KL_15	V_{KL_15L}	–1		+2	V	A
15.3	KL_15 pull-down current	V_S < 27V V_{KL_15} = 27V	KL_15	I_{KL_15}		50	65	µA	A
15.4	Internal debounce time	Without external capacitor	KL_15	Tdb_{KL_15}	80	160	250	µs	A
15.5	KL_15 wake-up time	R_V = 47kΩ, C = 100nF	KL_15	Tw_{KL_15}	0.4	2	4.5	ms	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

9. Electrical Characteristics (Continued)

5V < V_S < 27V, -40°C < Tj < 150°C, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
16	**WAKE Pin**								
16.1	High-level input voltage		WAKE	V_{WAKEH}	V_S – 1V		V_S + 0.3V	V	A
16.2	Low-level input voltage	Initializes a wake-up signal	WAKE	V_{WAKEL}	–1		V_S – 3.3V	V	A
16.3	WAKE pull-up current	V_S < 27V V_{WAKE} = 0V	WAKE	I_{WAKE}	–30	–10		µA	A
16.4	High-level leakage current	V_S = 27V V_{WAKE} = 27V	WAKE	I_{WAKEL}	–5		+5	µA	A
16.5	Time of low pulse for wake-up via WAKE pin	V_{WAKE} = 0V	WAKE	I_{WAKEL}	30	70	150	µs	A
17	**VCC Voltage Regulator ATA6622, PVCC = VCC**								
17.1	Output voltage VCC	4V < V_S < 18V (0mA to 50mA)	VCC	VCC_{nor}	3.234		3.366	V	A
		4.5V < V_S < 18V (0mA to 85mA)	VCC	VCC_{nor}	3.234		3.366	V	C
17.2	Output voltage VCC at low VS	3V < V_S < 4V	VCC	VCC_{low}	V_S – V_D		3.366	V	A
17.3	Regulator drop voltage	V_S > 3V I_{VCC} = –15mA	VS, VCC	V_{D1}			200	mV	A
17.4	Regulator drop voltage	V_S > 3V I_{VCC} = –50mA	VS, VCC	V_{D2}		500	700	mV	A
17.5	Line regulation	4V < V_S < 18V	VCC	VCC_{line}		0.1	0.2	%	A
17.6	Load regulation	5mA < I_{VCC} < 50mA	VCC	VCC_{load}		0.1	0.5	%	A
17.7	Power supply ripple rejection	10Hz to 100kHz C_{VCC} = 10µF V_S = 14V, I_{VCC} = –15mA	VCC		50			dB	D
17.8	Output current limitation	V_S > 4V	VCC	I_{VCClim}	–240	–160	–85	mA	A
17.9	External load capacity	0.2Ω < ESR < 5Ω at 100kHz for phase margin ≥ 60°	VCC	C_{load}	1.8	10		µF	D
		ESR < 0.2Ω at 100kHz for phase margin ≥ 30°							
17.10	VCC undervoltage threshold	Referred to VCC V_S > 4V	VCC	V_{thunN}	2.8		3.2	V	A
17.11	Hysteresis of undervoltage threshold	Referred to VCC V_S > 4V	VCC	$Vhys_{thun}$		150		mV	A
17.12	Ramp-up time V_S > 4V to V_{CC} = 3.3V	C_{VCC} = 2.2µF I_{load} = –5mA at VCC	VCC	T_{VCC}		100	250	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

9. Electrical Characteristics (Continued)

5V < V_S < 27V, -40°C < Tj < 150°C, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
18	**VCC Voltage Regulator ATA6624/ATA6626, PVCC = VCC**								
18.1	Output voltage VCC	5.5V < V_S < 18V (0mA to 50mA)	VCC	VCC_{nor}	4.9		5.1	V	A
		6V < V_S < 18V (0mA to 85mA)	VCC	VCC_{nor}	4.9		5.1	V	C
18.2	Output voltage VCC at low VS	4V < V_S < 5.5V	VCC	VCC_{low}	$V_S - V_D$		5.1	V	A
18.3	Regulator drop voltage	V_S > 4V I_{VCC} = –20mA	VS, VCC	V_{D1}			250	mV	A
18.4	Regulator drop voltage	V_S > 4V I_{VCC} = –50mA	VS, VCC	V_{D2}		400	600	mV	A
18.5	Regulator drop voltage	V_S > 3.3V I_{VCC} = –15mA	VS, VCC	V_{D3}			200	mV	A
18.6	Line regulation	5.5V < V_S < 18V	VCC	VCC_{line}		0.1	0.2	%	A
18.7	Load regulation	5mA < I_{VCC} < 50mA	VCC	VCC_{load}		0.1	0.5	%	A
18.8	Power supply ripple rejection	10Hz to 100kHz C_{VCC} = 10µF V_S = 14V, I_{VCC} = –15mA	VCC		50			dB	D
18.9	Output current limitation	V_S > 5.5V	VCC	I_{VCClim}	–240	–130	–85	mA	A
18.10	External load capacity	0.2Ω< ESR < 5Ω at 100kHz for phase margin ≥ 60°	VCC	C_{load}	1.8	10		µF	D
		ESR < 0.2Ω at 100kHz for phase margin ≥ 30°							
18.11	VCC undervoltage threshold	Referred to VCC V_S > 5.5V	VCC	V_{thunN}	4.2		4.8	V	A
18.12	Hysteresis of undervoltage threshold	Referred to VCC V_S > 5.5V	VCC	$Vhys_{thun}$		250		mV	A
18.13	Ramp-up time V_S > 5.5V to V_{CC} = 5V	C_{VCC} = 2.2µF I_{load} = –5mA at VCC	VCC	t_{VCC}		130	300	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 9-1. Definition of Bus Timing Characteristics

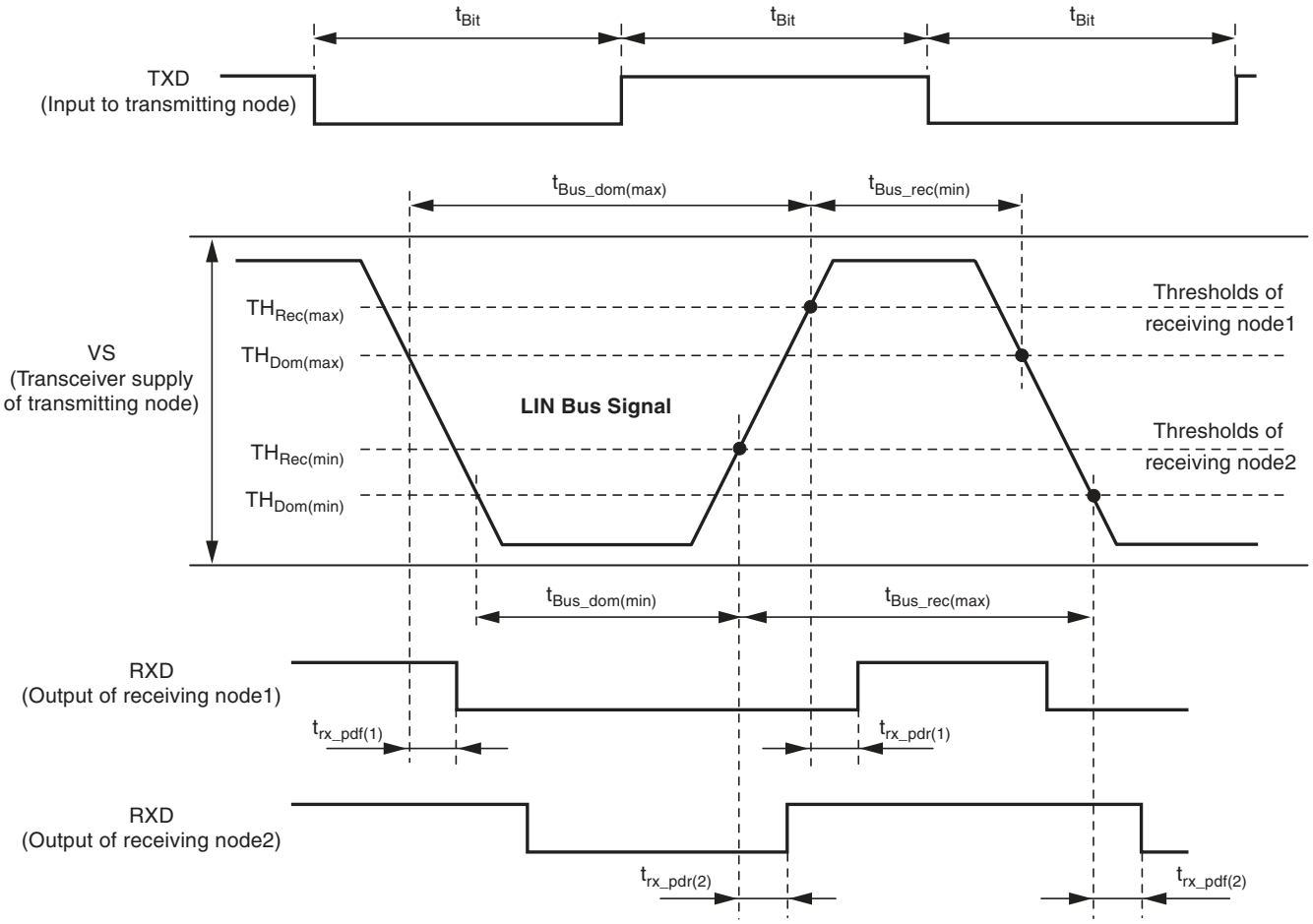


Figure 9-2. Typical Application Circuit

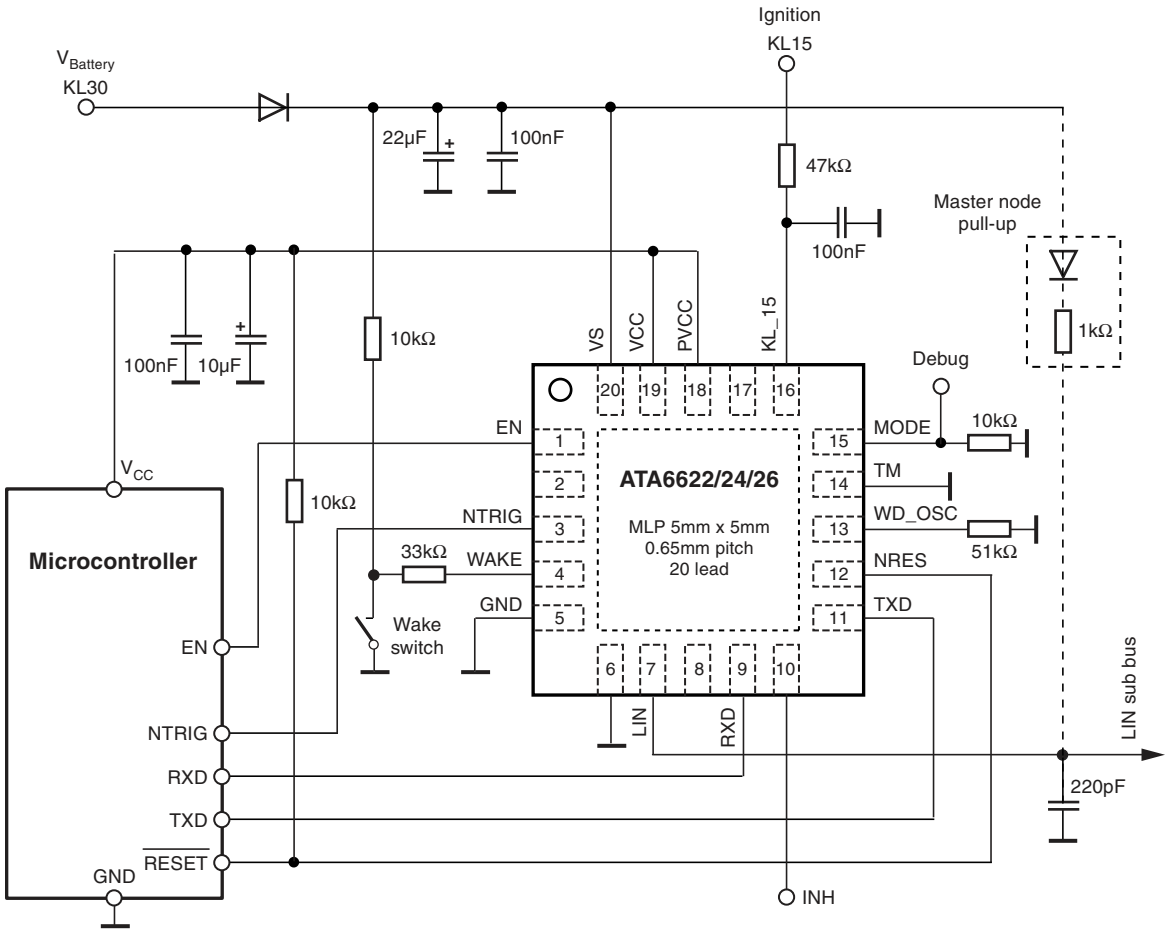
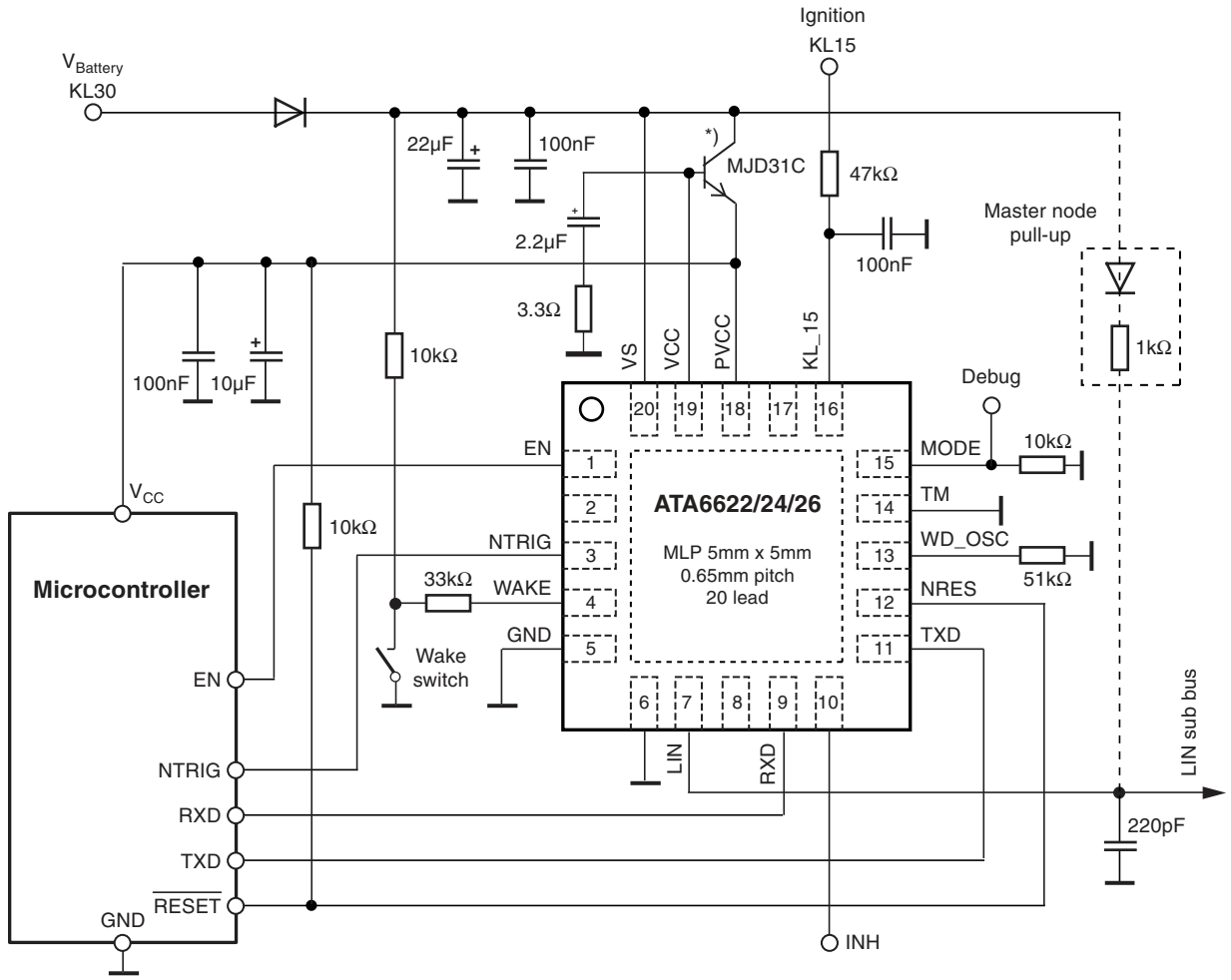
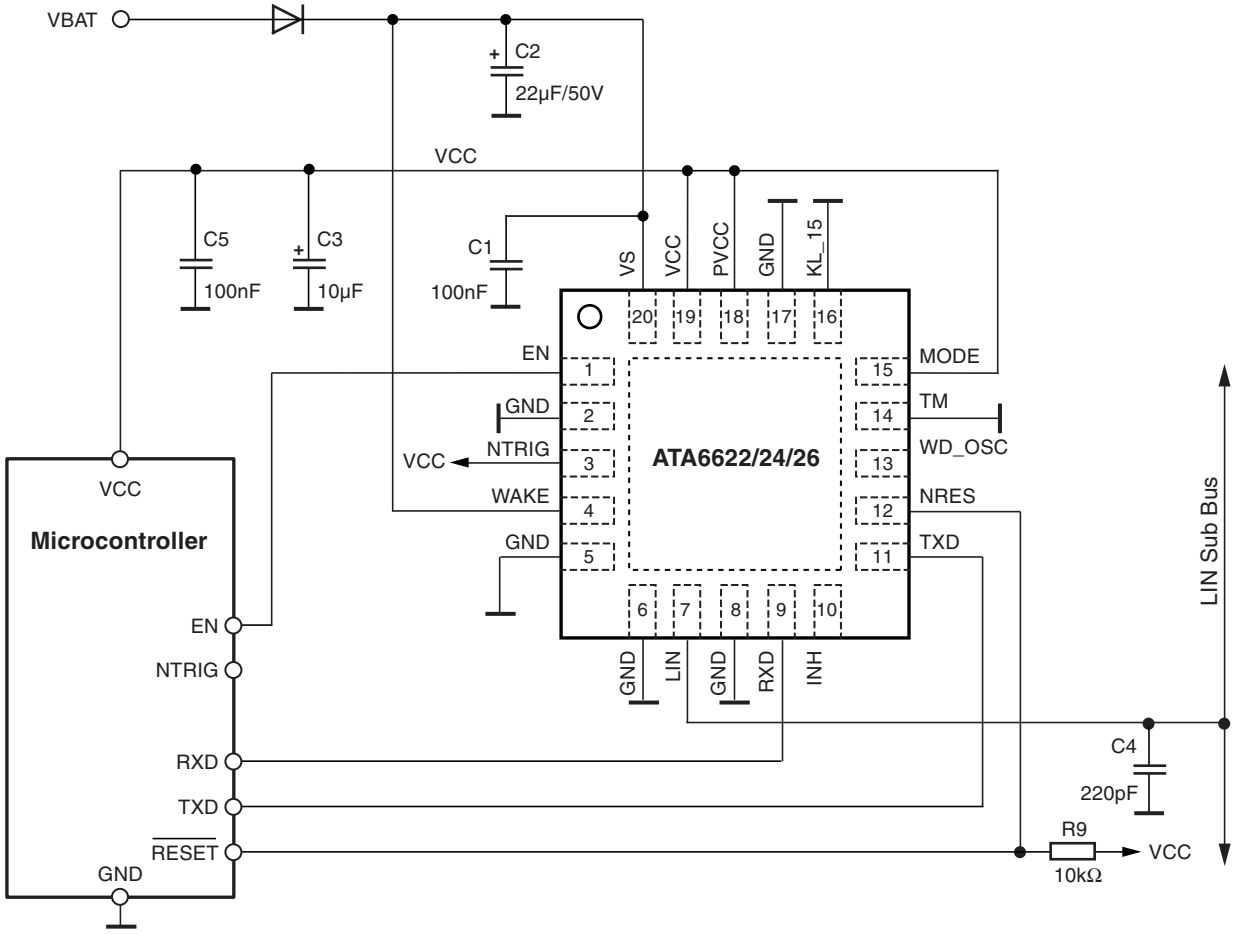


Figure 9-3. Application Circuit with External NPN-Transistor



*) Note that the output voltage PVCC is no longer short-ciruit protected when boosting the output current by an external NPN-transistor.

Figure 9-4. LIN Slave Application with Minimum External Devices



Note: No watchdog, INH output not used, no local wake-up

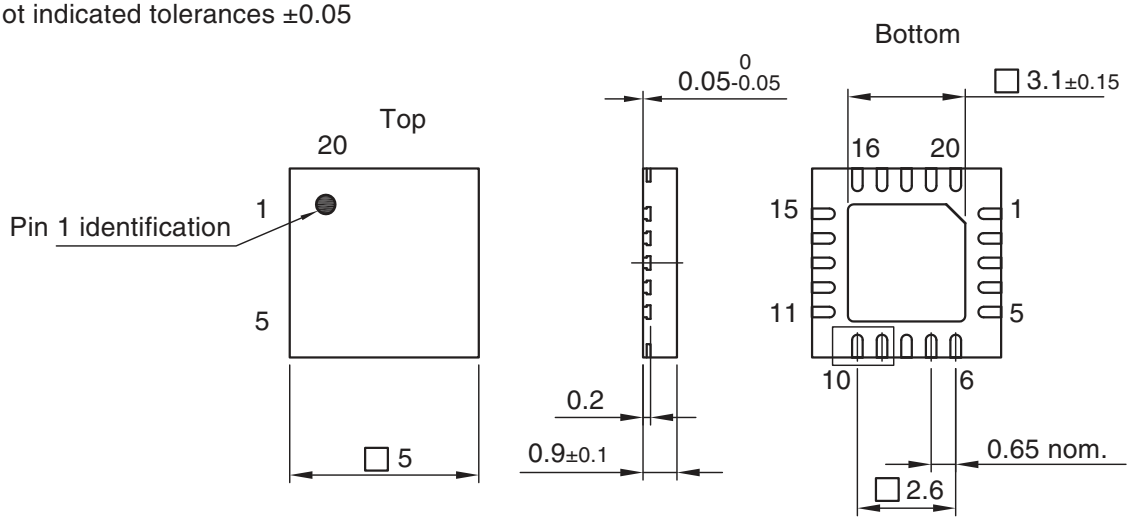
10. Ordering Information

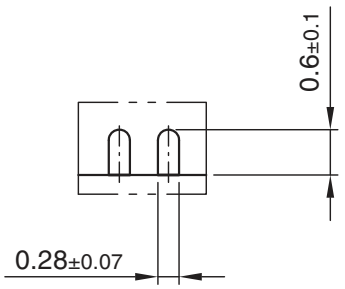
Extended Type Number	Package	Remarks
ATA6622-PGPW	QFN20	3.3V LIN system-basis-chip, Pb-free, 1.5k, taped and reeled
ATA6624-PGPW	QFN20	5V LIN system-basis-chip, Pb-free, 1.5k, taped and reeled
ATA6622-PGQW	QFN20	3.3V LIN system-basis-chip, Pb-free, 6k, taped and reeled
ATA6624-PGQW	QFN20	5V LIN system-basis-chip, Pb-free, 6k, taped and reeled
ATA6626-PGQW	QFN20	5V LIN system-basis-chip, Pb-free, 6k, taped and reeled
ATA6622C-PGPW	QFN20	3.3V LIN system-basis-chip, Pb-free, 1.5k, taped and reeled
ATA6624C-PGPW	QFN20	5V LIN system-basis-chip, Pb-free, 1.5k, taped and reeled
ATA6622C-PGQW	QFN20	3.3V LIN system-basis-chip, Pb-free, 6k, taped and reeled
ATA6624C-PGQW	QFN20	5V LIN system-basis-chip, Pb-free, 6k, taped and reeled
ATA6626C-PGQW	QFN20	5V LIN system-basis-chip, Pb-free, 6k, taped and reeled

11. Package Information

Package: VQFN_5 x 5_20L
Exposed pad 3.1 x 3.1
Dimensions in mm

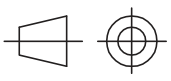
Not indicated tolerances ±0.05





Drawing-No.: 6.543-5129.01-4

Issue: 2; 09.02.07



technical drawings
according to DIN
specifications

12. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4986J-AUTO-03/11	• Features on page 1 changed • Section 1 “Description” on pages 1 to 2 changed • Table 2-1 “Pin Description” on page 3 changed • Section 3 “Functional Description” on pages 4 to 6 changed • Section 4 “Modes of Operation” on pages 7 to 11 changed • Section 5 “Wake-up Scenarios from Silent to Sleep Mode” on pages 12 to 14 changed • Section 7 “Absolute Maximum Ratings” on page 17 changed • Section 9 “Electrical Characteristics” on pages 18 to 26 changed
4986I-AUTO-07/10	• Section 6 “Watchdog” on pages 15 to 16 changed
4986H-AUTO-05/10	• New Part numbers ATA6622C, ATA6624C and ATA6626C added • Features on page 1 changed • Pin Description table: rows Pin 4 and Pin 15 changed • Text under headings 3.3, 3.9, 3.11, 5.5 and 6 changed • Figures 4-5, 6-1 and 9-3 changed • Abs.Max.Rat.Table -> Values in row “ESD HBM following....” changed • El.Char.Table -> rows changed: 7.1, 12.1, 12.2, 17.5, 17.6, 17.7, 17.8, 18.6, 18.7, 18.8, 18.9 • El.Char.Table -> row 8.13 added • Figures 9-2 and 9-3 figure title changed • Figure 9-4 on page 27 added • Ord.Info.Table -> new part numbers added
4986G-AUTO-08/09	• complete datasheet: “LIN 2.0 specification” changed in “LIN 2.1 specification” • Figures changed: 1-1, 4-2, 4-3, 4-4, 4-5, 5-1, 9-2, 9-3 • Sections changed: 3.1, 3.6, 3.8, 3.9, 3.10, 3.14, 4.1, 4.2, 4,3, 5.1, 5.2, 5.3, 5.5, 5.6 • Features and Description changed • Table 4-1 changed • Abs. Max. Ratings table changed • Thermal Characteristics table inserted • El. Characteristics table changed
4986F-AUTO-05/08	• Section 3.15 “INH Output Pin” on page 6 changed • Section 5.5 “Fail-safe Features” on page 13 changed • Section 6.1 “Typical Timing Sequence with R_{WD_OSC} = 51 kΩ” on page 15 changed • Section 8 “Electrical Characteristics” numbers 1.6 to 1.8 on page 18 changed
4986E-AUTO-02/08	• Figure 2-1 on page 3 renamed • Figure 6-1 “Timing Sequence with R_{WD_OSC} = 51 kΩ” on page 16 changed • Figure 8-3 “Application Circuit with External NPN” on page 26 added
4986D-AUTO-10/07	• Section 9 “Ordering Information” on page 26 changed

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