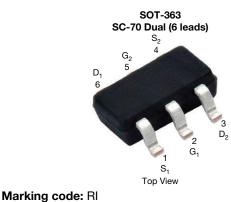
Vishay Siliconix



N- and P-Channel 30 V (D-S) MOSFET



N-CHANNEL

30

0.388

0.525

0.55

0.7

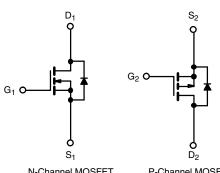
Dual

FEATURES

- TrenchFET[®] power MOSFET
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- DC/DC converter
- · Load switch



N-Channel MOSFET

P-Channel MOSFET

ORDERING INFORMATION

PRODUCT SUMMARY

 $\mathsf{R}_{\text{DS(on)}}\left(\Omega\right)$ at V_{GS} = \pm 10 V

 $R_{DS(on)}(\Omega)$ at $V_{GS} = \pm 4.5 \text{ V}$

V_{DS} (V)

I_D (A) ^a

Q_g typ. (nC)

Configuration

Package	SOT-363
Lead (Pb)-free and halogen-free	Si1539DDL-T1-GE3

P-CHANNEL

-30

1.070

2.590

0.8

-0.46

ABSOLUTE MAXIMUM RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)							
PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT			
Drain-source voltage		V _{DS}	30	-30	v		
Gate-source voltage		V _{GS}	± 20	± 20	v		
	T _C = 25 °C		0.7	-0.46			
Continuous drain surrent $(T_{\rm e} = 150 ^{\circ}{\rm C})$	T _C = 70 °C		0.6	-0.36	A		
Continuous drain current ($T_J = 150 \ ^\circ C$)	T _A = 25 °C	I ID	0.7 ^{b, c}	-0.42 ^{b, c}			
	T _A = 70 °C		0.5 ^{b, c}	-0.33 ^{b, c}			
Source-drain current diode current	T _C = 25 °C		0.3	-0.3			
Source-drain current diode current	T _A = 25 °C	- I _S	0.2 ^{b, c}	-0.2 ^{b, c}	1		
Pulsed drain current (t = 100 µs)		I _{DM}	2	-1			
$T_{\rm C} = 2$			0.34	0.34			
Maximum power dissipation	T _C = 70 °C		0.22	0.22	w		
	T _A = 25 °C	P _D	0.29 ^{b, c}	0.29 ^{b, c}	vv		
	T _A = 70 °C	1	0.18 ^{b, c}	0.18 ^{b, c}			
Operating junction and storage temperature range)	T _J , T _{stg}	-55 tc	+150	°C		

THERMAL RESISTANCE RATINGS								
PARAMETER		SYMBOL	N-CH/	NNEL	P-CHA	NNEL		
PARAMETER		STINDUL	TYP.	MAX.	TYP.	MAX.	UNIT	
Maximum junction-to-ambient b, d	t ≤ 10 s	R _{thJA}	365	438	365	438	°C/W	
Maximum junction-to-foot (drain)	Steady state	R _{thJF}	308	370	308	370	0/10	

Notes

a. Based on $T_C = 25 \ ^{\circ}C$

b. Surface mounted on 1" x 1" FR4 board

c. t = 10 s

d. Maximum under steady state conditions is 486 °C/W (N-Channel) and 486 °C/W (P-Channel)

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RoHS COMPLIANT HALOGEN FREE



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PARAMETER	SYMBOL	herwise noted) TEST CONDITIONS		MIN.	TYP. ^a	MAX.	UNIT	
Static								
		V _{GS} = 0 V, I _D = 250 μA	N-Ch	30	-	-		
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	P-Ch	-30	-	-	V	
		I _D = 250 μA	N-Ch	-	30	-		
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	I _D = -250 μA	P-Ch	-	-25	-	mV/°C	
		I _D = 250 μA	N-Ch	-	-3.6	-		
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = -250 μA	P-Ch	-	3.1	-		
		V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1.2	-	2.5		
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-1.5	-	-3	V	
			N-Ch	-	-	± 100		
Gate-body leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	P-Ch	-	-	± 100	nA	
		V _{DS} = 30 V, V _{GS} = 0 V	N-Ch	-	-	1		
		$V_{DS} = -30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	P-Ch	-	-	-1	1	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch	-	-	10	μA	
		V _{DS} = -30 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch	-	-	-10	1	
		V _{DS} = 5 V, V _{GS} = 10 V	N-Ch	2	-	-	A	
On-state drain current ^b	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -10 V	P-Ch	-1	-	-		
		V _{GS} = 10 V, I _D = 0.6 A	N-Ch	-	0.323	0.388	1	
Drain-source on-state resistance ^b	R _{DS(on)}	V _{GS} = -10 V, I _D = -0.4 A	P-Ch	-	0.890	1.070	Ω	
		V _{GS} = 4.5 V, I _D = 0.1A	N-Ch	-	0.437	0.525		
		V _{GS} = -5 V, I _D = -0.1 A		-	1.850	2.590		
		V _{GS} = -4.35 V, I _D = -0.1 A	P-Ch	-	2.800	-		
		V _{DS} = 15 V, I _D = 0.6 A	N-Ch	-	1.2	-	_	
Forward transconductance ^b g _{fs}		V _{DS} = -15 V, I _D = -0.4 A	P-Ch	-	0.6	-	S	
Dynamic ^a					•		1	
			N-Ch	-	28	-		
Input capacitance	C _{iss}	N-Channel	P-Ch	-	21	-	1	
	_	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	N-Ch	-	10	-	_	
Output capacitance	C _{oss}	P-Channel	P-Ch	-	10	-	- pF -	
		$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, \text{ f} = 1 \text{ MHz}$	N-Ch	-	5	-		
Reverse transfer capacitance	C _{rss}		P-Ch	-	6	-		
	_	$V_{DS} = 15 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 0.6 \text{ A}$	N-Ch	-	1	1.5	-	
		$V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -0.4 \text{ A}$	P-Ch	-	1.5	3		
Total gate charge	Qg		N-Ch	-	0.55	1.1		
		N-Channel	P-Ch	-	0.8	1.2		
	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V} \text{ I}_{D} = 0.6 \text{ A}$	N-Ch	-	0.2	-	nC	
Gate-source charge		P-Channel	P-Ch	-	0.4	-		
Outer during the	_	V_{DS} = -15 V, V_{GS} = -4.5 V, I_D = -0.4 A	N-Ch	-	0.2	-	-	
Gate-drain charge	Q _{gd}		P-Ch	-	0.35	-		
Outo and the se	_		N-Ch	0.7	3.7	7.4	~	
Gate resistance	R _g	f = 1 MHz	P-Ch	0.3	15	30	Ω	

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Si1539DDL

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N-Ch annel N-Ch annel N-Ch - 2 4 Rise time tr N-Ch annel P-Ch - 4 8 Turn-off delay time tr $V_{DD} = 15 V, R_L = 30 \Omega$ N-Ch - 14 21 Turn-off delay time t_d(ort) P-Channel N-Ch - 14 21 P-Ch - 18 30 N-Ch - 11 20 P-Ch - 18 30 N-Ch - 11 20 P-Ch - 18 30 N-Ch - 11 20 P-Ch - 18 30 N-Ch - 18 30 Turn-on delay time tr N-Ch - 18 30 Turn-on delay time t_d(ort) N-Ch annel N-Ch - 22 33 Turn-off delay time t_d(ort) P-Ch annel N-Ch - 28 42 Turn-off delay time t_r P-Ch annel N-Ch - 14 21 N_DD = -15 V, R_L = 30 \Omega I_D = 0.3 A, V_{GEN} = -4.5 V, R_g = 1 \Omega N-Ch - 14 </th <th>SPECIFICATIONS (T_J = 25 °C</th> <th>, unless ot</th> <th>herwise noted)</th> <th></th> <th></th> <th></th> <th></th> <th></th>	SPECIFICATIONS (T _J = 25 °C	, unless ot	herwise noted)					
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP. ^a	MAX.	UNIT
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Dynamic ^a		•					•
$\begin{array}{ c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	Turn-on delay time	t-(()		N-Ch	-	2	4	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		۹(on)	N-Channel	P-Ch	-	4	8	
$ \begin{array}{ c c c c c c } I_{0} = 0.5 \text{ A}, \text{ V}_{0EN} = 10 \text{ V}, \Omega \\ P-\text{Channel} \\ P-\text{Channel} \\ P-\text{Ch} & - & 18 & 30 \\ P-\text{Ch} & - & 11 & 20 \\ P-\text{Ch} & - & 8 & 16 \\ P-\text{Ch} & - & 9 & 18 \\ P-\text{Ch} & - & 18 & 30 \\ P-\text{Ch} & - & 9 & 18 \\ P-\text{Ch} & - & 9 & 18 \\ P-\text{Ch} & - & 18 & 30 \\ P-\text{Ch} & - & 9 & 18 \\ P-\text{Ch} & - & 18 & 30 \\ P-\text{Ch} & - & 9 & 18 \\ P-\text{Ch} & - & 18 & 30 \\ P-\text{Ch} & - & 9 & 18 \\ P-\text{Ch} & - & 22 & 33 \\ P-\text{Ch} & - & 28 & 42 \\ P-\text{Ch} & - & 28 & 42 \\ P-\text{Ch} & - & 14 & 21 \\ P-\text{Ch} & - & 16 & 39 \\ P-\text{Ch} & - & 14 & 21 \\ P-\text{Ch} & - & 14 & 21 \\ P-\text{Ch} & - & 18 & 30 \\ P-\text{Ch} & - & 14 & 21 \\ P-\text{Ch} & - & 14 & 21 \\ P-\text{Ch} & - & 18 & 30 \\ P-\text{Ch} & - & 13 & 20 \\ P-\text{Ch} &$	Rise time	t.	V_{DD} = 15 V, R_L = 30 Ω		-	14	21	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		۲ 	$I_D \cong 0.5 \text{ A}, V_{GEN} = 10 \text{ V}, \text{ R}_g = 1 \Omega$	P-Ch	-	18	30	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Turn-off delay time	t-1/- 40	i onamoi	N-Ch	-	11	20	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		°а(оп)		P-Ch	-	8	16	
$ \begin{array}{ c c c c c } \hline P-Ch & - & 18 & 30 \\ \hline P-Ch & - & 18 & 30 \\ \hline P-Ch & - & 26 & 39 \\ \hline P-Ch & - & 22 & 33 \\ \hline P-Ch & - & 14 & 21 \\ \hline P-Ch & - & 14 & 21 \\ \hline P-Ch & - & 15 & 23 \\ \hline P-Ch & - & 15 & 23 \\ \hline P-Ch & - & 18 & 30 \\ \hline P-Ch & - & 18 & 30 \\ \hline P-Ch & - & 18 & 30 \\ \hline P-Ch & - & 18 & 30 \\ \hline P-Ch & - & - & 0.3 \\ \hline P-Ch & - & - & 0.3 \\ \hline P-Ch & - & - & 0.3 \\ \hline P-Ch & - & - & 0.3 \\ \hline P-Ch & - & - & 0.3 \\ \hline P-Ch & - & - & -0.3 \\ \hline P-Ch & - & - & -0.3 \\ \hline P-Ch & - & - & -0.3 \\ \hline P-Ch & - & - & -0.3 \\ \hline P-Ch & - & - & -1 \\ \hline P-$	Fall time	t,		N-Ch	-	9	18	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		4		P-Ch	-	18	30	20
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Turn-on delay time	talan		N-Ch	-	26	39	110
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		°a(on)	N-Channel	P-Ch	-	22	33	
$\begin{split} & I_{D} \equiv 0.5 \text{ A}, \ V_{GEN} = 4.5 \text{ V}, \ H_{g} = 1 \Omega \\ & I_{D} \equiv 0.5 \text{ A}, \ V_{GEN} = 4.5 \text{ V}, \ H_{g} = 1 \Omega \\ & P-Ch & - & 28 & 42 \\ \hline P-Ch & - & 14 & 21 \\ \hline P-Ch & - & 14 & 21 \\ \hline P-Ch & - & 14 & 21 \\ \hline P-Ch & - & 14 & 21 \\ \hline P-Ch & - & 14 & 21 \\ \hline P-Ch & - & 14 & 8 \\ \hline N-Ch & - & 15 & 23 \\ \hline P-Ch & - & 15 & 23 \\ \hline P-Ch & - & 18 & 30 \\ \hline \\ \hline P-Ch & - & 18 & 30 \\ \hline \\ $	Rise time	t _r	V_{DD} = 15 V, R_L = 30 Ω	N-Ch	-	25	38	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $			$I_D \cong 0.5 \text{ A}, V_{\text{GEN}} = 4.5 \text{ V}, \text{R}_\text{g} = 1 \Omega$	P-Ch	-	28	42	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Turn-off delay time	t _{d(off)}		N-Ch	-	14	21	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$				P-Ch	-	4	8	
$ \begin{array}{ c c c c c c c c } \hline P-Ch & - & 18 & 30 \\ \hline P-Ch & - & 18 & 30 \\ \hline \\ \hline \\ Drain-Source Body Diode Characteristics \\ \hline \\ Continuous source-drain diode current \\ I_S & T_C = 25 ^{\circ}C & \hline \\ \hline P-Ch & - & - & 0.3 \\ \hline P-Ch & - & - & -0.3 \\ \hline \\ P-Ch & - & - & -2 \\ \hline \\ P-Ch & - & - & -1 \\ \hline \\ \hline \\ P-Ch & - & - & -1 \\ \hline \\ P-Ch & - & - & -1 \\ \hline \\ P-Ch & - & - & -1 \\ \hline \\ P-Ch & - & - & -1 \\ \hline \\ P-Ch & - & - & -1 \\ \hline \\ P-Ch & - & - & -1 \\ \hline \\ P-Ch & - & 0.8 & 1.2 \\ \hline \\ P-Ch & - & 0.8 & -1.2 \\ \hline \\ P-Ch & - & 10 & 20 \\ \hline \\ P-Ch & - & 13 & 20 \\ \hline \\ P-Ch & - & 13 & 20 \\ \hline \\ P-Ch & - & 13 & 20 \\ \hline \\ P-Ch & - & 13 & 20 \\ \hline \\ P-Ch & - & 3 & 6 \\ \hline \\ P-Ch & - & 3 & 6 \\ \hline \\ P-Ch & - & 8 & 16 \\ \hline \\ P-Ch & - & 8 & 16 \\ \hline \\ P-Ch & - & 6 & - \\ \hline \\ P-Ch & - & 6 & - \\ \hline \\ P-Ch & - & 7 & - \\ \hline \\ P-Ch & - & 7 & - \\ \hline \\ P-Ch & - & 7 & - \\ \hline \\ P-Ch & - & 7 & - \\ \hline \\ P-Ch & - & 4 & - \\ \hline \\ \hline \\ P-Ch & - & 4 & - \\ \hline \\ \hline \\ P-Ch & - & 7 & - \\ \hline \\ P-Ch & - & 4 & - \\ \hline \\ \hline \\ P-Ch & - & 4 & - \\ \hline \\ \hline \\ P-Ch & - & 4 & - \\ \hline \\ \hline \\ \hline \\ \hline \\ \hline \\ P-Ch & - & 4 & - \\ \hline \\$	Fall Time	+.	10 = 0.07, $10 = 4.00$, $10 = 122$	N-Ch	I	15	23	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		ч		P-Ch	-	18	30	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Drain-Source Body Diode Characteri	stics						
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Continuous source drain diade current	la la	To = 25 °C	N-Ch	I	-	0.3	A
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Continuous source-urain diode current	IS	10 = 23 0	P-Ch	-	-	-0.3	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Pulse diode forward current			N-Ch	-	-	2	
Body diode voltage V_{SD} $I_S = -0.4 \text{ A}$ P-Ch - -0.8 -1.2 V Body diode reverse recovery time t_{rr} t_{rr} $N-Ch$ - 10 20 ns Body diode reverse recovery time t_{rr} $N-Ch$ - 13 20 ns Body diode reverse recovery charge Q_{rr} $I_F = 0.5 \text{ A}$, di/dt = 100 A/µs, $T_J = 25 \text{ °C}$ $N-Ch$ - 3 6 nC Reverse recovery fall time t_a $I_F = -0.5 \text{ A}$, di/dt = -100 A/µs, $T_J = 25 \text{ °C}$ $N-Ch$ - 6 - $P-Ch$ - 7 - $N-Ch$ ns Reverse recovery rise time t_h	(t = 100 μs)	ISM		P-Ch	I	-	-1	
$\frac{1}{18} = -0.4 \text{ A} \qquad \frac{P-Ch}{I} \qquad - \frac{-0.8}{I} \qquad -1.2 \qquad \frac{1}{I} = 0.5 \text{ A} \qquad \frac{P-Ch}{I} \qquad - \frac{-0.8}{I} \qquad -1.2 \qquad \frac{1}{I} = 0.5 \text{ A} \qquad \frac{P-Ch}{I} \qquad - \frac{10}{I} \qquad \frac{20}{I} \qquad \frac{P-Ch}{I} \qquad - \frac{10}{I} \qquad - \frac{10}{I} \qquad \frac{20}{I} \qquad \frac{P-Ch}{I} \qquad - \frac{10}{I} \qquad - $	Body diade voltage	Var	I _S = 0.5 A	N-Ch	-	0.8	1.2	V
Body diode reverse recovery time t_{rr} N-ChannelP-Ch-1320Body diode reverse recovery charge Q_{rr} $I_F = 0.5 A, di/dt = 100 A/\mu s, T_J = 25 °C$ N-Ch-36nCP-Ch-36-P-Ch-816nCReverse recovery fall time t_a $I_F = -0.5 A, di/dt = -100 A/\mu s, T_J = 25 °C$ N-Ch-6Reverse recovery rise time t_b $I_F = -0.5 A, di/dt = -100 A/\mu s, T_J = 25 °C$ N-Ch-7-ns	body diode voltage	v SD	I _S = -0.4 A	P-Ch	-	-0.8	-1.2	
Body diode reverse recovery charge Q_{rr} N-Channel P-Ch - 13 20 N-Channel $I_F = 0.5 \text{ A}, di/dt = 100 \text{ A/}\mu\text{s}, T_J = 25 \text{ °C}$ N-Ch - 3 6 nC Reverse recovery fall time t_a $I_F = -0.5 \text{ A}, di/dt = -100 \text{ A/}\mu\text{s}, T_J = 25 \text{ °C}$ N-Ch - 8 16 nC Reverse recovery fall time t_a $I_F = -0.5 \text{ A}, di/dt = -100 \text{ A/}\mu\text{s}, T_J = 25 \text{ °C}$ N-Ch - 6 - - N-Ch - 7 - N-Ch - 4 - ns	Dedu diede ververe vees verver time	t _{rr}		N-Ch	-	10	20	20
Body diode reverse recovery charge Q_{rr} $I_F = 0.5 \text{ A}, di/dt = 100 \text{ A/}\mu\text{s}, T_J = 25 \text{ °C}$ $P-Channel$ $P-Channel$ $P-Channel$ $N-Ch$ $ 8$ 16 nC Reverse recovery fall time t_a $I_F = -0.5 \text{ A}, di/dt = -100 \text{ A/}\mu\text{s}, T_J = 25 \text{ °C}$ $P-Ch$ $ 8$ 16 nC P-Channel $I_F = -0.5 \text{ A}, di/dt = -100 \text{ A/}\mu\text{s}, T_J = 25 \text{ °C}$ $N-Ch$ $ 6$ $ P-Ch$ $ 0$ N-Ch $ 0$ $Reverse recovery rise timet_h$	Body diode reverse recovery time			P-Ch	-	13	20	115
Image: Problem in the second system is set as a second system in the second system in the second system is set as a second system in the second system in the second system is set as a second system in the second system is set as a second system in the second system is set as a second system in the second system is set as a second system in the second system is set as a second system in the second system is set as a second system in the second system in the second system in the second system is set as a second system in the second system in the second system is set as a second system in the second sys	Rody diada rayaraa raaayary aharaa	Q _{rr}		N-Ch	-	3	6	nC
Reverse recovery fall time t_a $I_F = -0.5 \text{ A}$, di/dt = $-100 \text{ A}/\mu \text{s}$, $T_J = 25 \text{ °C}$ P-Ch - 7 - Reverse recovery rise time t_b t_b N-Ch - 4 -	Body diode reverse recovery charge			P-Ch	-	8	16	
$\frac{P-Ch}{N-Ch} = \frac{7}{4}$ ns Reverse recovery rise time t_h	Poverse receivery fall time	t _a		N-Ch	-	6	-	
Reverse recovery rise time the			$I_F = -0.5 \text{ A}, \text{ di/dt} = -100 \text{ A/}\mu\text{s}, \text{ T}_J = 25 ^\circ\text{C}$	P-Ch	-	7	-	200
P-Ch - 6 -		+]	N-Ch	-	4	-	ns
	neverse recovery rise time	τ _b		P-Ch	-	6	-	

Notes

a. Guaranteed by design, not subject to production testing

b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %

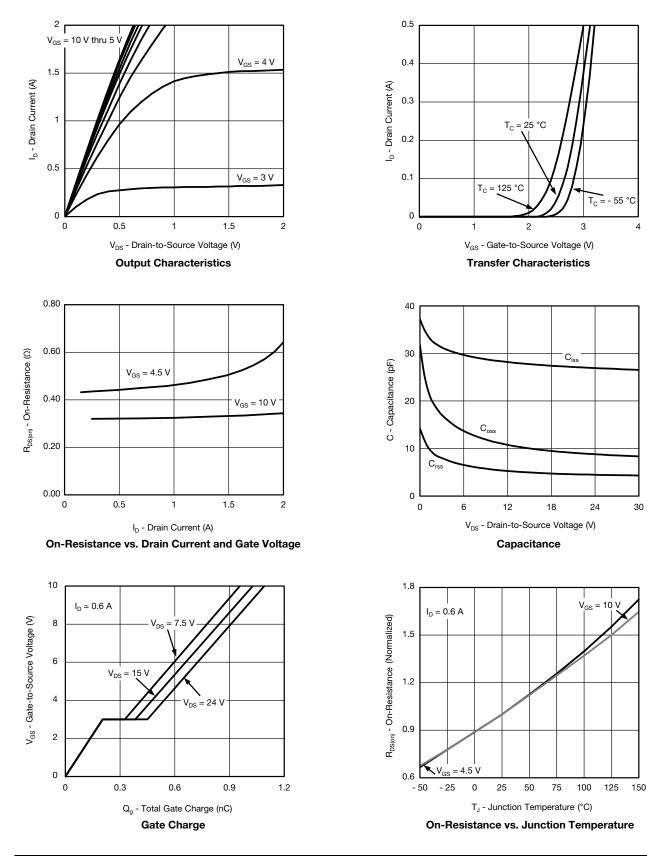
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



4

30

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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4

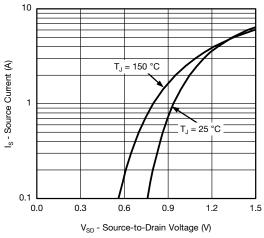
Document Number: 62999

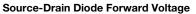
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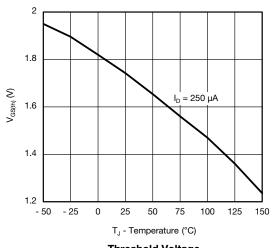


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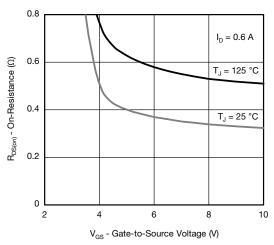
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



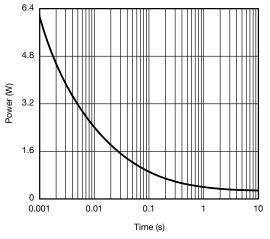




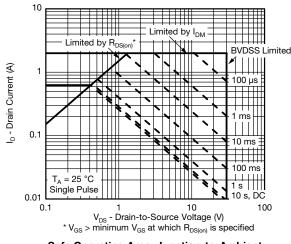




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient

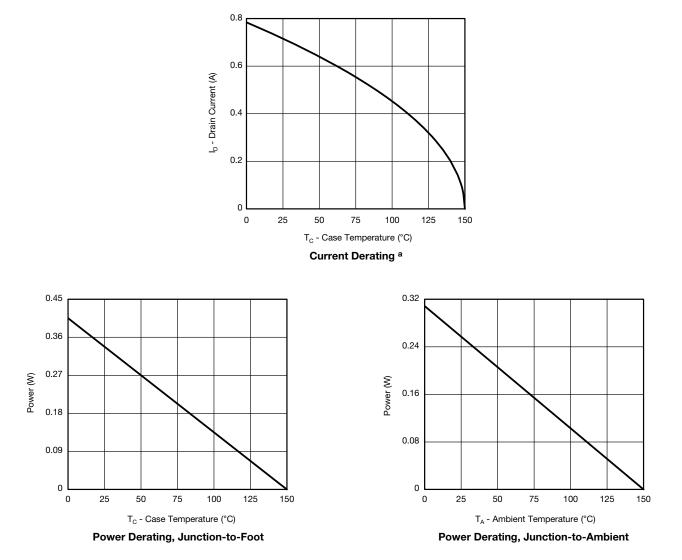
5

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N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

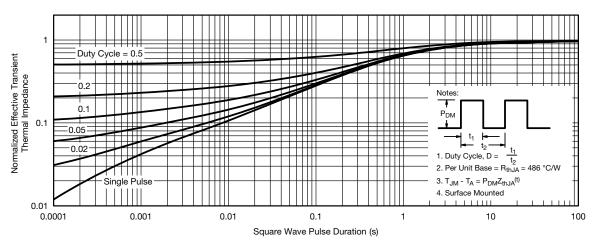


Note

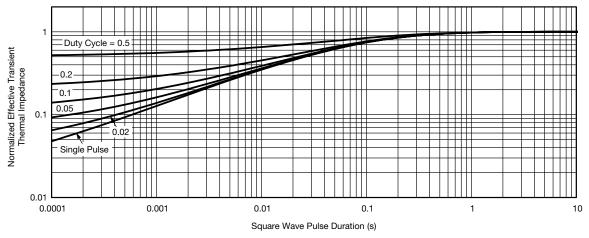
a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



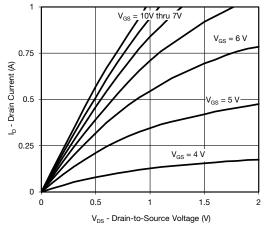
Normalized Thermal Transient Impedance, Junction-to-Ambient



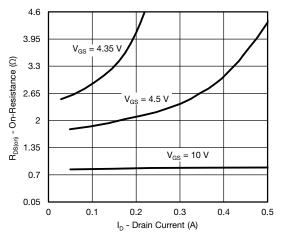
Normalized Thermal Transient Impedance, Junction-to-Foot



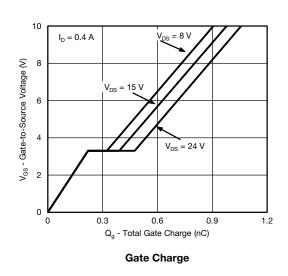
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

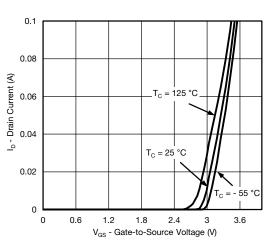


Output Characteristics

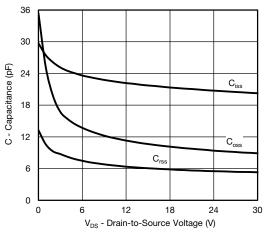


On-Resistance vs. Drain Current and Gate Voltage

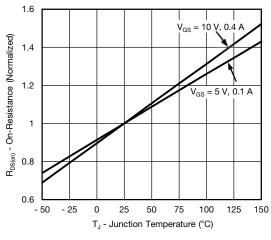




Transfer Characteristics



Capacitance



On-Resistance vs. Junction Temperature

S17-1009-Rev. B, 03-Jul-17

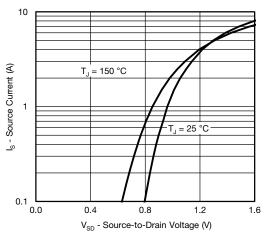
8 stions contact: pmostechsupp Document Number: 62999

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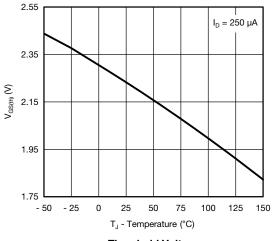




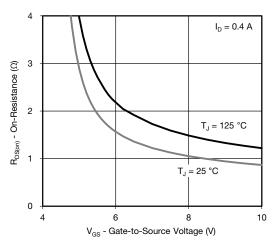
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



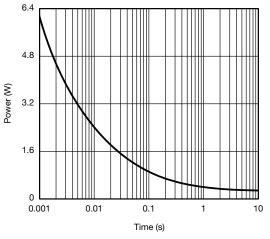
Source-Drain Diode Forward Voltage



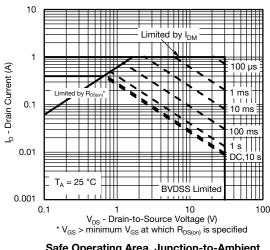
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient

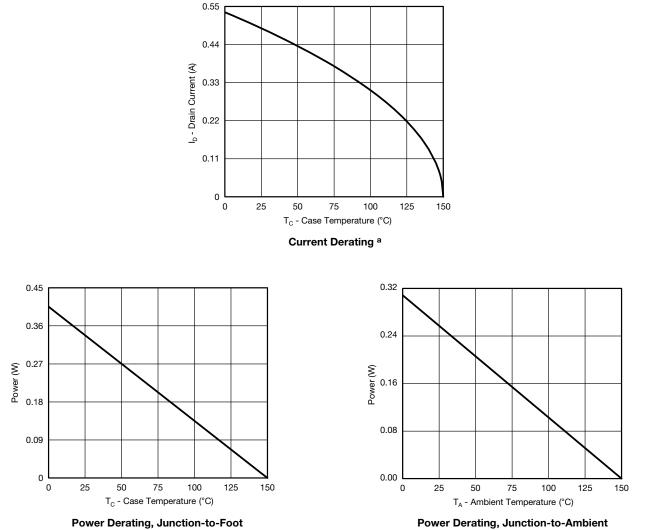
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Vishay Siliconix

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

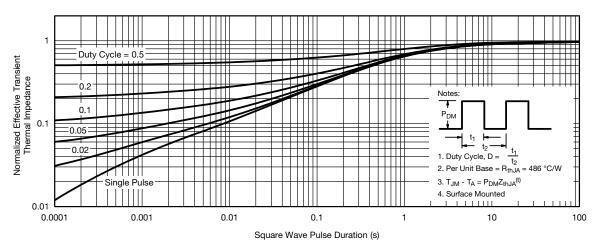


Note

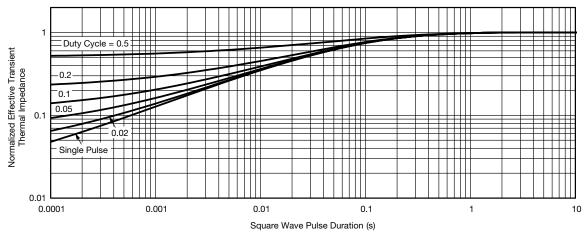
a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



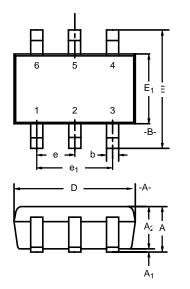
Normalized Thermal Transient Impedance, Junction-to-Foot

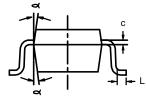
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Package Information Vishay Siliconix

SC-70: 6-LEADS





	MILLIMETERS				INCHES		
Dim	Min	Nom	Max	Min	Nom	Max	
Α	0.90	-	1.10	0.035	-	0.043	
A ₁	-	-	0.10	-	-	0.004	
A ₂	0.80	-	1.00	0.031	-	0.039	
b	0.15	-	0.30	0.006	-	0.012	
С	0.10	-	0.25	0.004	-	0.010	
D	1.80	2.00	2.20	0.071	0.079	0.087	
E	1.80	2.10	2.40	0.071	0.083	0.094	
E ₁	1.15	1.25	1.35	0.045	0.049	0.053	
е		0.65BSC			0.026BSC	;	
e ₁	1.20	1.30	1.40	0.047	0.051	0.055	
L	0.10	0.20	0.30	0.004	0.008	0.012	
م	≺ 7°Nom 7°Nom						
	ECN: S-03946—Rev. B, 09-Jul-01 DWG: 5550						



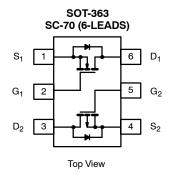
Dual-Channel LITTLE FOOT® SC-70 6-Pin MOSFET Recommended Pad Pattern and Thermal Performance

INTRODUCTION

This technical note discusses the pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for dual-channel LITTLE FOOT power MOSFETs in the SC-70 package. These new Vishay Siliconix devices are intended for small-signal applications where a miniaturized package is needed and low levels of current (around 250 mA) need to be switched, either directly or by using a level shift configuration. Vishay provides these devices with a range of on-resistance specifications in 6-pin versions. The new 6-pin SC-70 package enables improved on-resistance values and enhanced thermal performance.

PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the dual-channel SC-70 device in the 6-pin configuration.





For package dimensions see outline drawing SC-70 (6-Leads) (http://www.vishay.com/doc?71154)

BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFET*s, (http://www.vishay.com/doc?72286) for the 6-pin SC-70. This basic pad pattern is sufficient for the low-power applications for which this package is intended. For the 6-pin device, increasing the pad patterns yields a reduction in thermal resistance on the order of 20% when using a 1-inch square with full copper on both sides of the printed circuit board (PCB).

EVALUATION BOARDS FOR THE DUAL SC70-6

The 6-pin SC-70 evaluation board (EVB) measures 0.6 inches by 0.5 inches. The copper pad traces are the same as described in the previous section, *Basic Pad Patterns*. The board allows interrogation from the outer pins to 6-pin DIP connections permitting test sockets to be used in evaluation testing.

The thermal performance of the dual SC-70 has been measured on the EVB with the results shown below. The minimum recommended footprint on the evaluation board was compared with the industry standard 1-inch square FR4 PCB with copper on both sides of the board.

THERMAL PERFORMANCE

Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the dual SC-70 6-pin package measured as junction-to-foot thermal resistance is 300°C/W typical, 350°C/W maximum. The "foot" is the drain lead of the device as it connects with the body. Note that these numbers are somewhat higher than other LITTLE FOOT devices due to the limited thermal performance of the Alloy 42 lead-frame compared with a standard copper lead-frame.

Junction-to-Ambient Thermal Resistance (dependent on PCB size)

The typical $R\theta_{JA}$ for the dual 6-pin SC-70 is 400°C/W steady state. Maximum ratings are 460°C/W for the dual. All figures based on the 1-inch square FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the dual 6-pin SC-70 package at two different ambient temperatures.



SC-70 (6-PIN)	
Room Ambient 25 °C	Elevated Ambient 60 °C
$P_{D} = \frac{T_{J(max)} - T_{A}}{R\theta_{JA}}$	$P_{D} = \frac{T_{J(max)} - T_{A}}{R\boldsymbol{\theta}_{JA}}$
$P_{\rm D} = \frac{150^{\circ}{\rm C} - 25^{\circ}{\rm C}}{400^{\circ}{\rm C}/{\rm W}}$	$P_{D} = \frac{150^{\circ}C - 60^{\circ}C}{400^{\circ}C/W}$
$P_D = 312 \text{ mW}$	$P_D = 225 \text{ mW}$

NOTE: Although they are intended for low-power applications, devices in the 6-pin SC-70 will handle power dissipation in excess of 0.2 W.

Testing

To aid comparison further, Figure 2 illustrates the dual-channel SC-70 thermal performance on two different board sizes and two different pad patterns. The results display the thermal performance out to steady state. The measured steady state values of $R\theta_{JA}$ for the dual 6-pin SC-70 are as follows:

LITTLE FOOT SC-70 (6-PIN)				
1) Minimum recommended pad pattern (see Figure 2) on the EVB of 0.5 inches x 0.6 inches.	518°C/W			
2) Industry standard 1" square PCB with maximum copper both sides.	413°C/W			

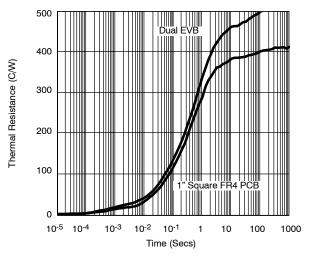


FIGURE 2. Comparison of Dual SC70-6 on EVB and 1" Square FR4 PCB.

The results show that if the board area can be increased and maximum copper traces are added, the thermal resistance reduction is limited to 20%. This fact confirms that the power dissipation is restricted with the package size and the Alloy 42 leadframe.

ASSOCIATED DOCUMENT

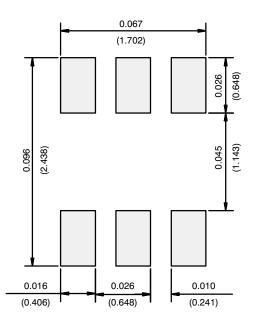
Single-Channel LITTLE FOOT SC-70 6-Pin MOSFET Copper Leadframe Version, REcommended Pad Pattern and Thermal Performance, AN815, (http://www.vishay.com/doc?71334).

Application Note 826

Vishay Siliconix



RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index



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