

MOSFET

950V CoolMOS™ PFD7 SJ Power Device

The latest 950V CoolMOS™ PFD7 series sets a new benchmark in the super junction (SJ) technologies. This technology is designed to address Lighting and Industrial SMPS applications by combining best-in-class performance with state-of-the-art ease of use. Compared to the CoolMOS™ P7 families, the PFD7 offers an integrated ultra-fast body diode enabling usage in resonant topologies with markets lowest reverse recovery charge (Q_{rr}).

Features

- Integrated ultra-fast body diode
- Best-in-class reverse recovery charge Q_{rr}
- Best-in-class FOM $R_{DS(on)} * E_{oss}$, reduced Q_g , C_{iss} , and C_{oss}
- Best-in-class $V_{(GS)th}$ of 3V and smallest $V_{(GS)th}$ variation of $\pm 0.5V$
- Integrated fast body diode
- Best-in-class CoolMOS™ quality and reliability
- Fully optimized portfolio
- Best-in-class $R_{DS(on)}$ in THD and SMD packages
- ESD protection min. Class 2 (HBM)

Benefits

- Excellent hard commutation robustness enabling usage in resonant topologies
- Extra safety margin for designs with increased bus voltage
- Enabling increased power density solutions
- Improved full load efficiency in industrial SMPS applications
- Price competitiveness over previous CoolMOS™ families
- Improved production yield by reducing ESD related failures

Potential applications

- Suitable for hard & soft switching topologies
- Optimized for usage in LLC and ZVS topologies
- PFC & LLC applications in Lighting and Industrial SMPS

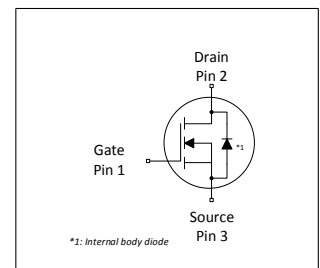
Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_j = 25\text{ °C}$	950	V
$R_{DS(on),max}$	130	mΩ
$Q_{g,typ}$	141	nC
I_D	13.9	A
E_{oss} @ 500V	9.5	μJ
Body diode di_F/dt	1300	A/μs
Q_{oss} @ 500V	0.33	μC

Type / Ordering Code	Package	Marking	Related Links
IPA95R130PFD7	PG-TO220 FullPAK	95R130D7	see Appendix A



RoHS

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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	13.9 8.7	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	150	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	100	mJ	$I_D=3.8\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.77	mJ	$I_D=3.8\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, single pulse	I_{AS}	-	-	3.8	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	33	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	I_S	-	-	10	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	150	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	70	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 10\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di _F /dt	-	-	1300	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 10\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	V_{ISO}	-	-	2500	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$. Maximum Duty Cycle $D = 0.50$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_θ

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.80	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	leaded
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	°C/W	n.a.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	950	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	2.5	3	3.5	V	$V_{DS}=V_{GS}, I_D=1.25mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=950V, V_{GS}=0V, T_j=25^\circ\text{C}$ $V_{DS}=950V, V_{GS}=0V, T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.1 0.27	0.13	Ω	$V_{GS}=10V, I_D=25.1A, T_j=25^\circ\text{C}$ $V_{GS}=10V, I_D=25.1A, T_j=150^\circ\text{C}$
Gate resistance	R_G	-	0.9	-	Ω	$f=250kHz$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	4170	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Output capacitance	C_{oss}	-	53	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	88	-	pF	$V_{GS}=0V, V_{DS}=0...400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	894	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	25	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=25.1A,$ $R_G=5.3\Omega$; see table 9
Rise time	t_r	-	14	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=25.1A,$ $R_G=5.3\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	118	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=25.1A,$ $R_G=5.3\Omega$; see table 9
Fall time	t_f	-	3.6	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=25.1A,$ $R_G=5.3\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	19	-	nC	$V_{DD}=760V, I_D=25.1A, V_{GS}=0$ to 10V
Gate to drain charge	Q_{gd}	-	43	-	nC	$V_{DD}=760V, I_D=25.1A, V_{GS}=0$ to 10V
Gate charge total	Q_g	-	141	-	nC	$V_{DD}=760V, I_D=25.1A, V_{GS}=0$ to 10V
Gate plateau voltage	$V_{plateau}$	-	4.5	-	V	$V_{DD}=760V, I_D=25.1A, V_{GS}=0$ to 10V

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	1.1	-	V	$V_{GS}=0V, I_F=25.1A, T_j=25^{\circ}C$
Reverse recovery time	t_{rr}	-	153	-	ns	$V_R=400V, I_F=25.1A, di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	1.10	-	μC	$V_R=400V, I_F=25.1A, di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	14.0	-	A	$V_R=400V, I_F=25.1A, di_F/dt=100A/\mu s$; see table 8

4 Electrical characteristics diagrams

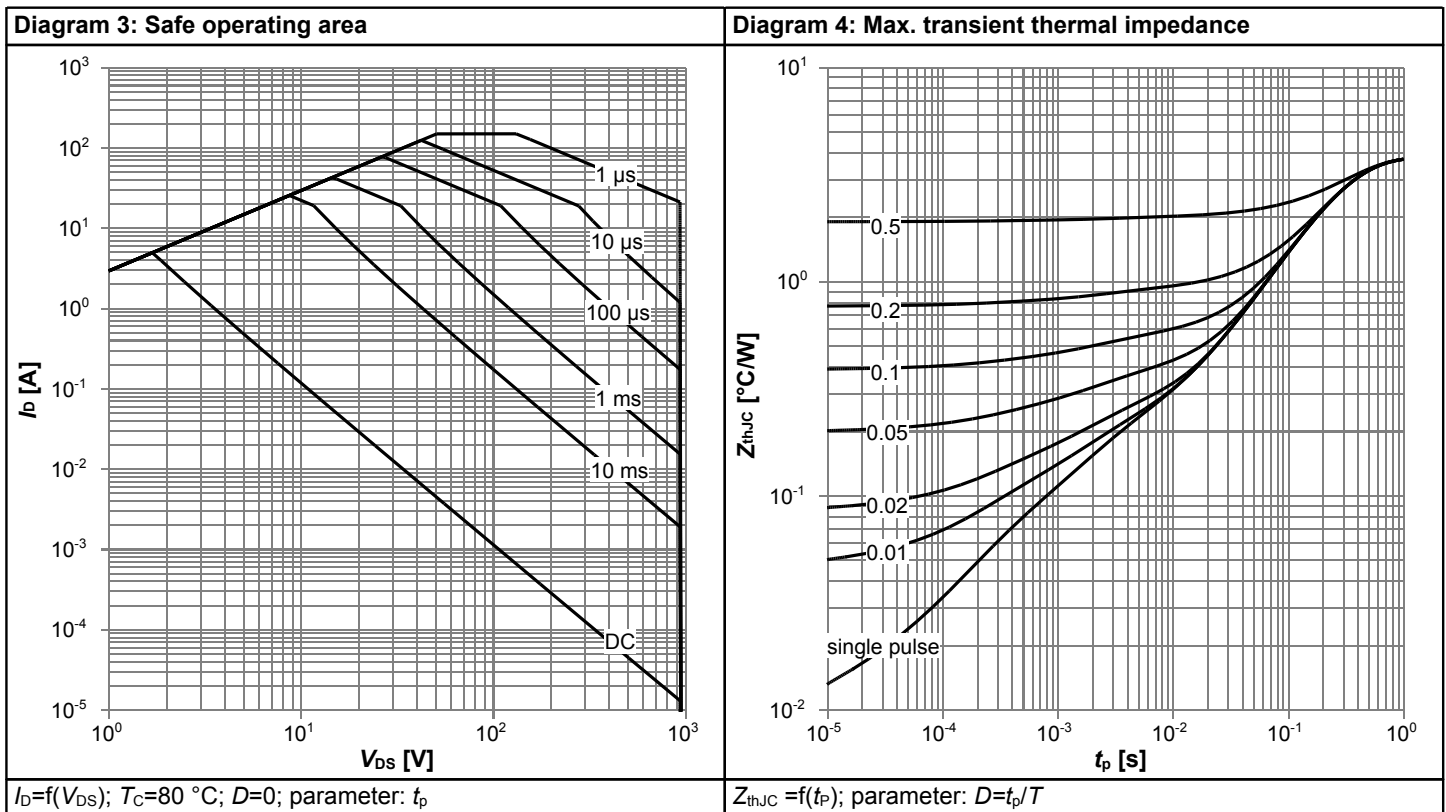
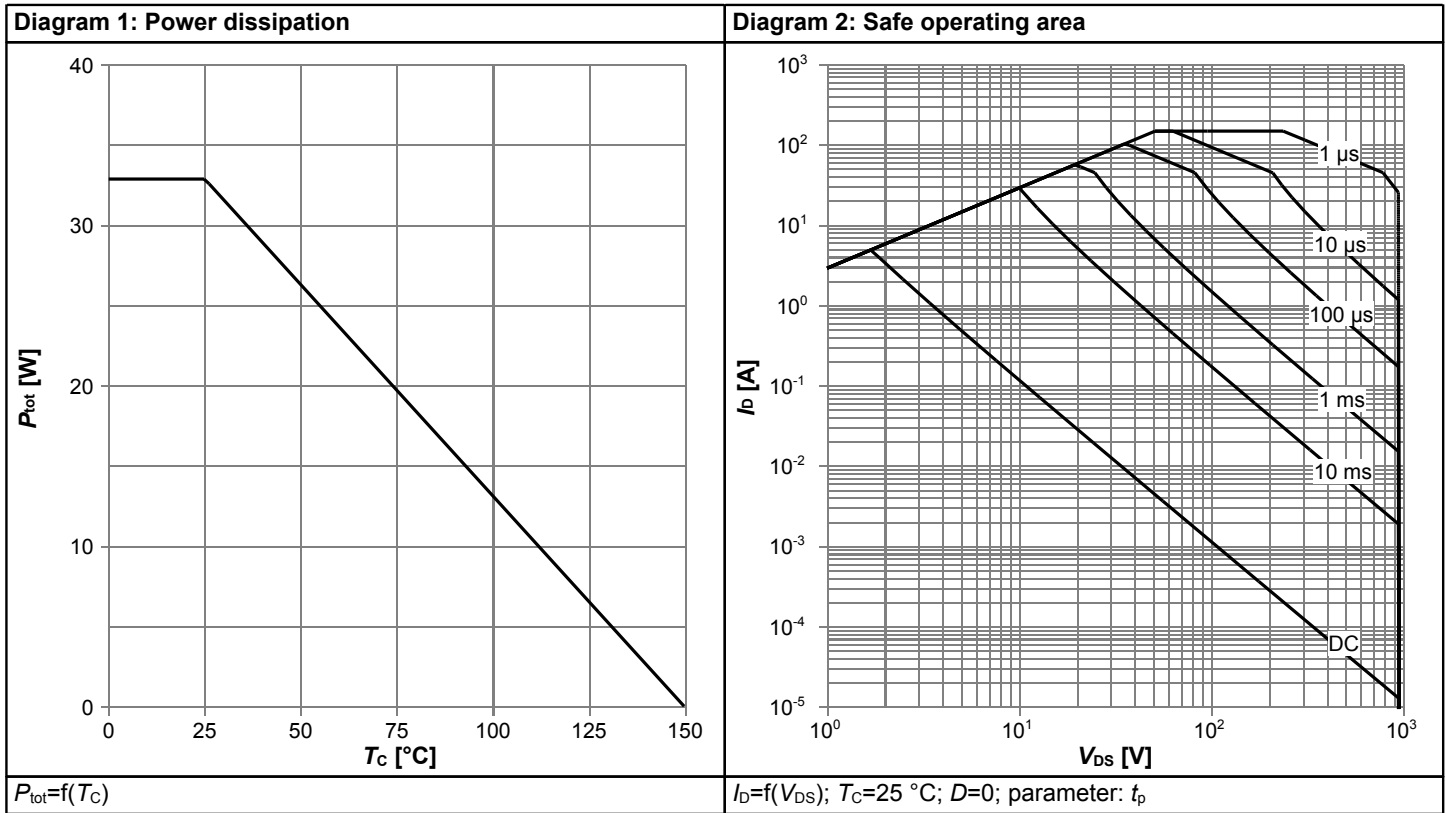
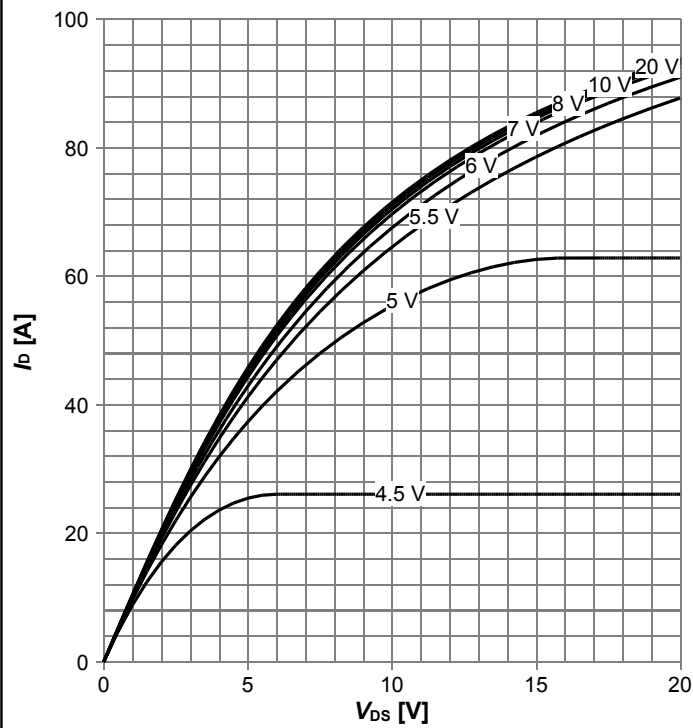
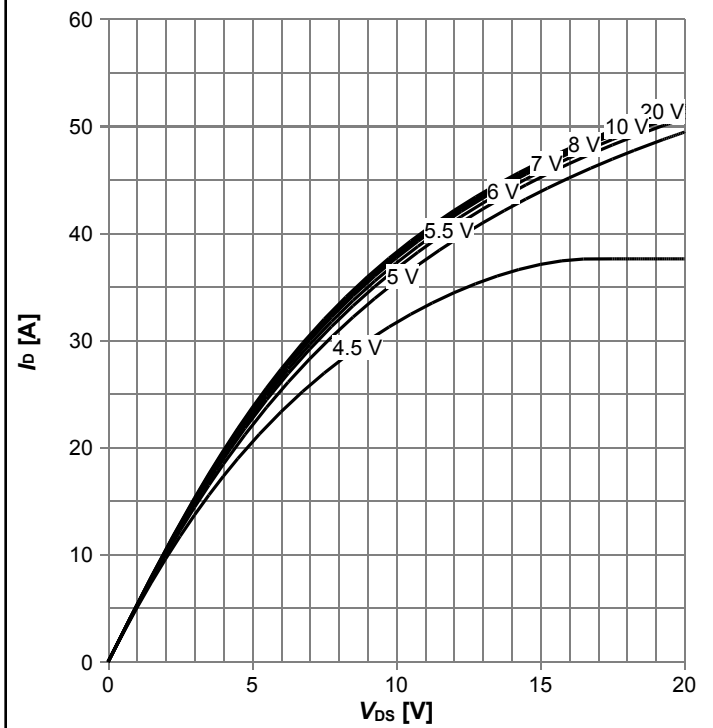


Diagram 5: Typ. output characteristics



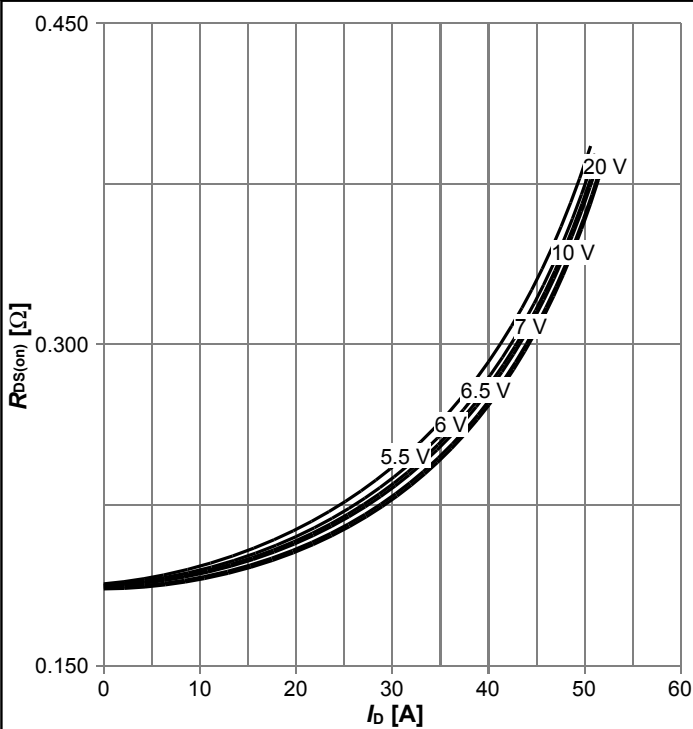
$I_D=f(V_{DS}); T_j=25\text{ °C};$ parameter: V_{GS}

Diagram 6: Typ. output characteristics



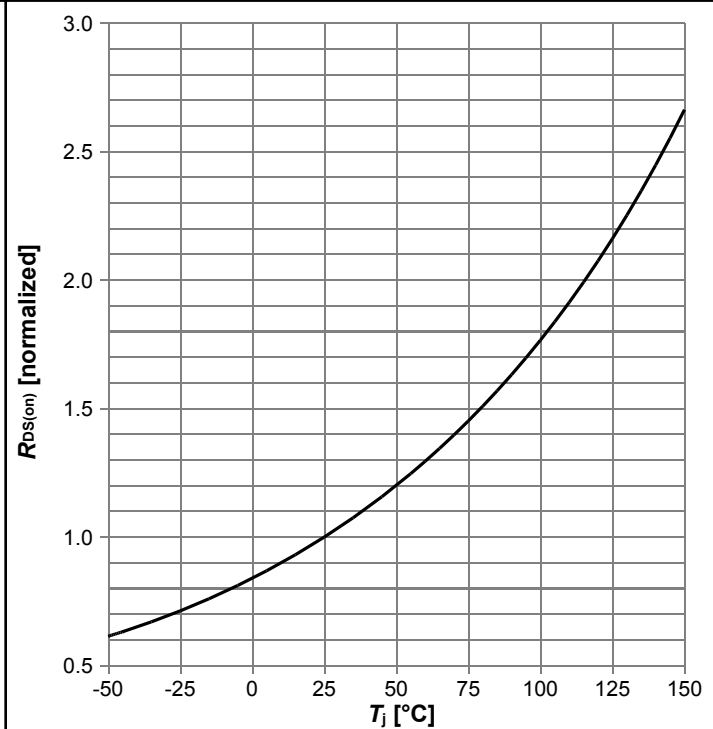
$I_D=f(V_{DS}); T_j=125\text{ °C};$ parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



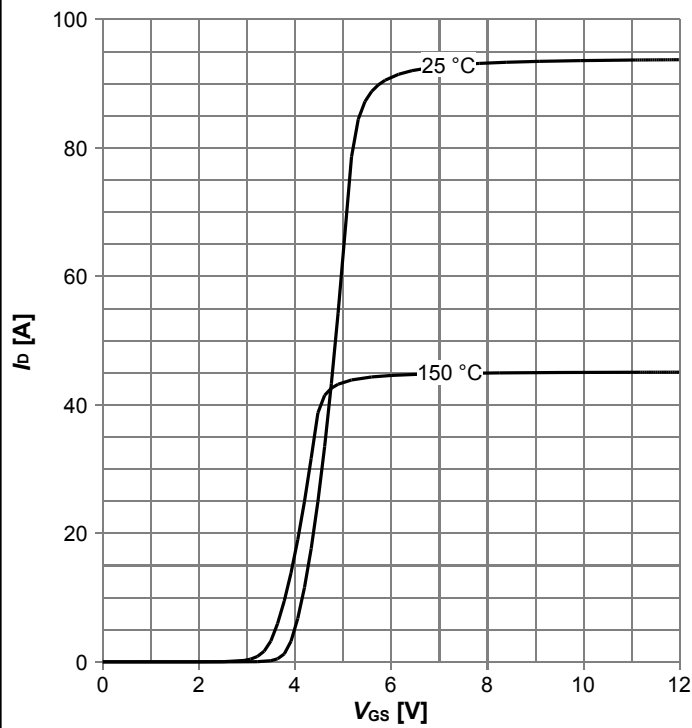
$R_{DS(on)}=f(I_D); T_j=125\text{ °C};$ parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



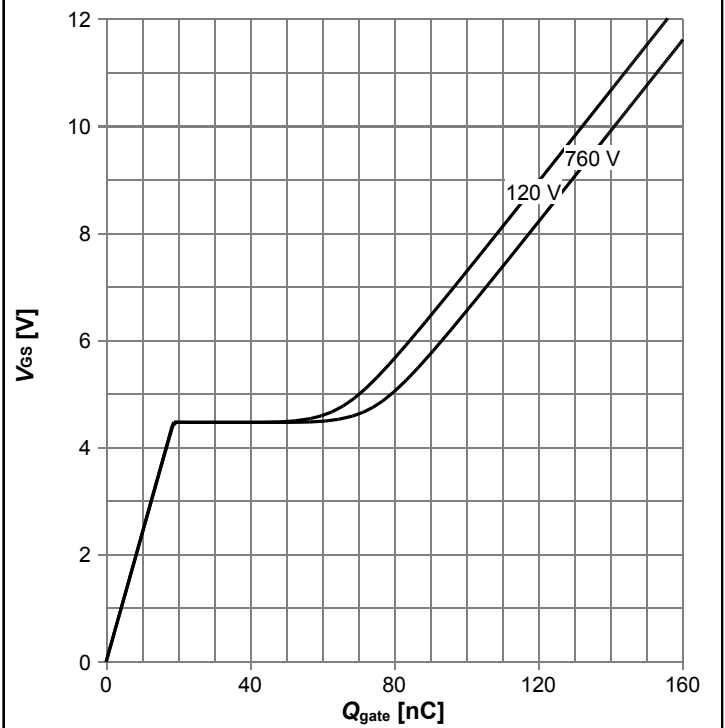
$R_{DS(on)}=f(T_j); I_D=25.1\text{ A}; V_{GS}=10\text{ V}$

Diagram 9: Typ. transfer characteristics



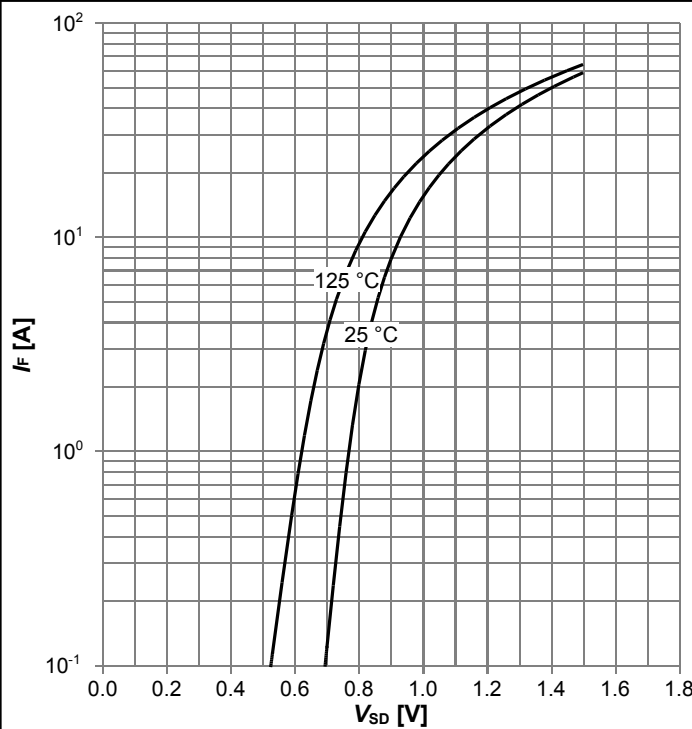
$I_D=f(V_{GS})$; $V_{DS}=20V$; parameter: T_j

Diagram 10: Typ. gate charge



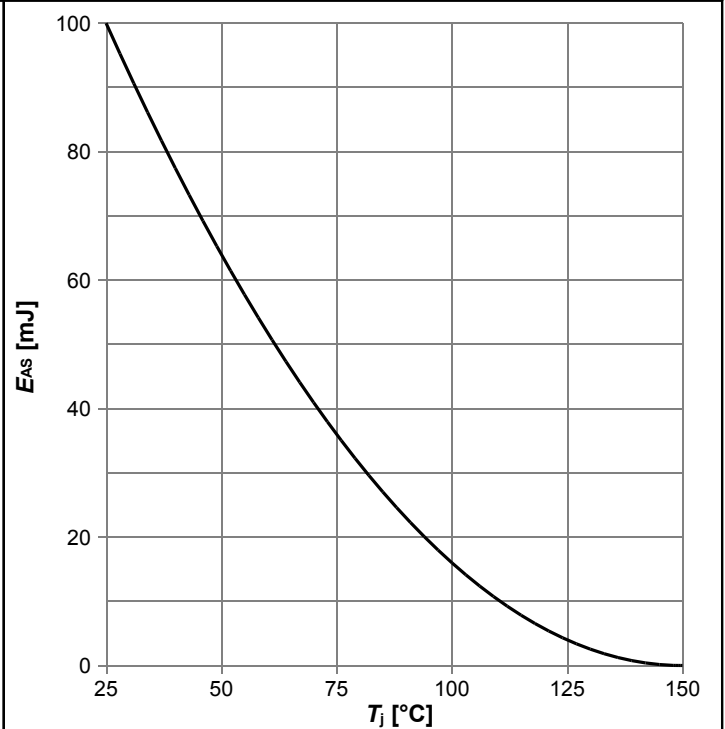
$V_{GS}=f(Q_{gate})$; $I_D=25.1$ A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



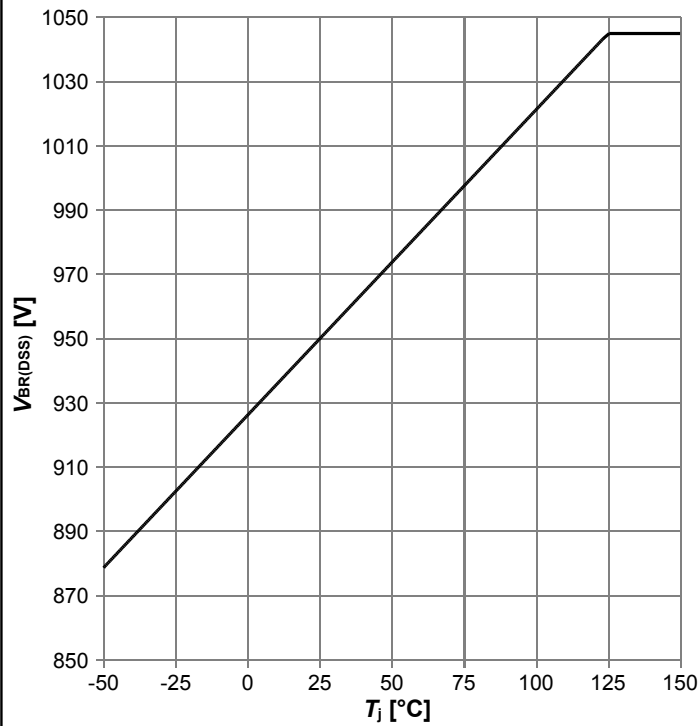
$I_F=f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



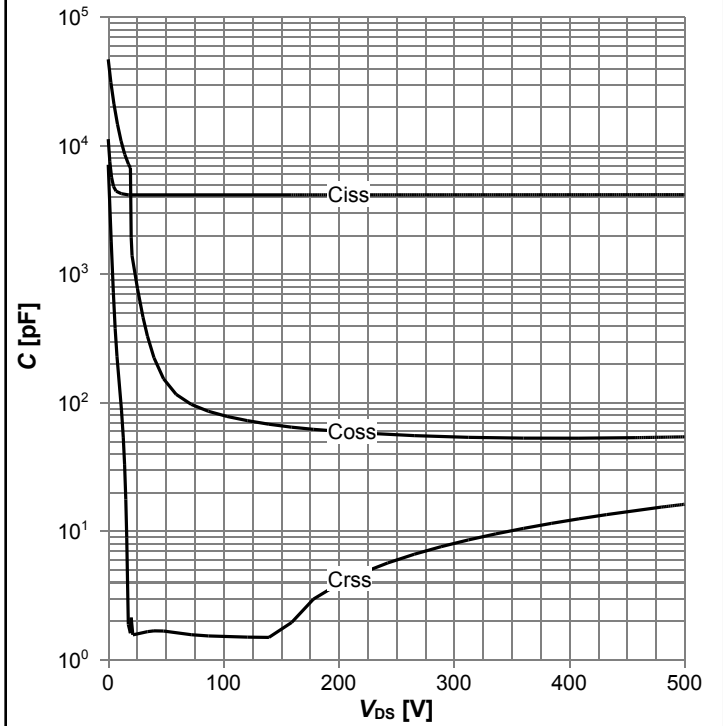
$E_{AS}=f(T_j)$; $I_D=3.8$ A; $V_{DD}=50$ V

Diagram 13: Drain-source breakdown voltage



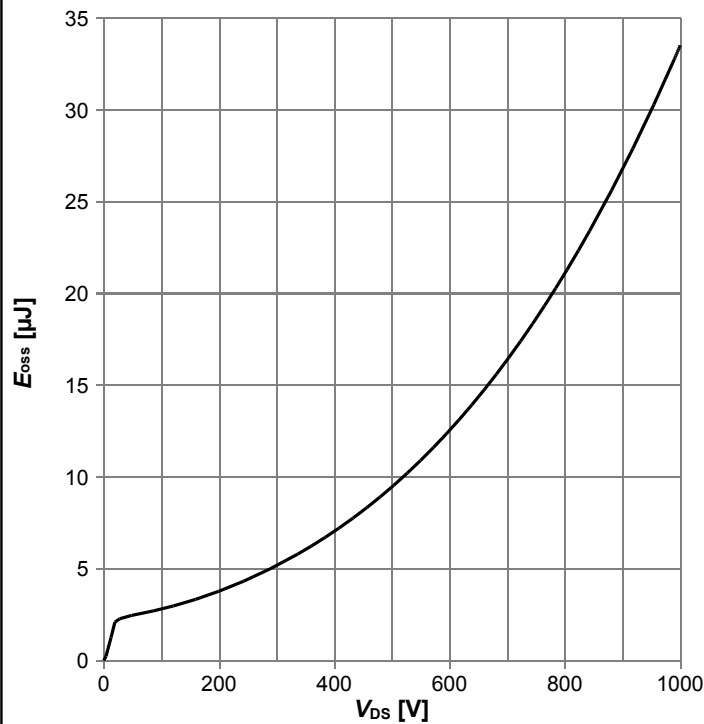
$V_{BR(DSS)}=f(T_j); I_D=1\text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=250\text{ kHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics



Table 9 Switching times

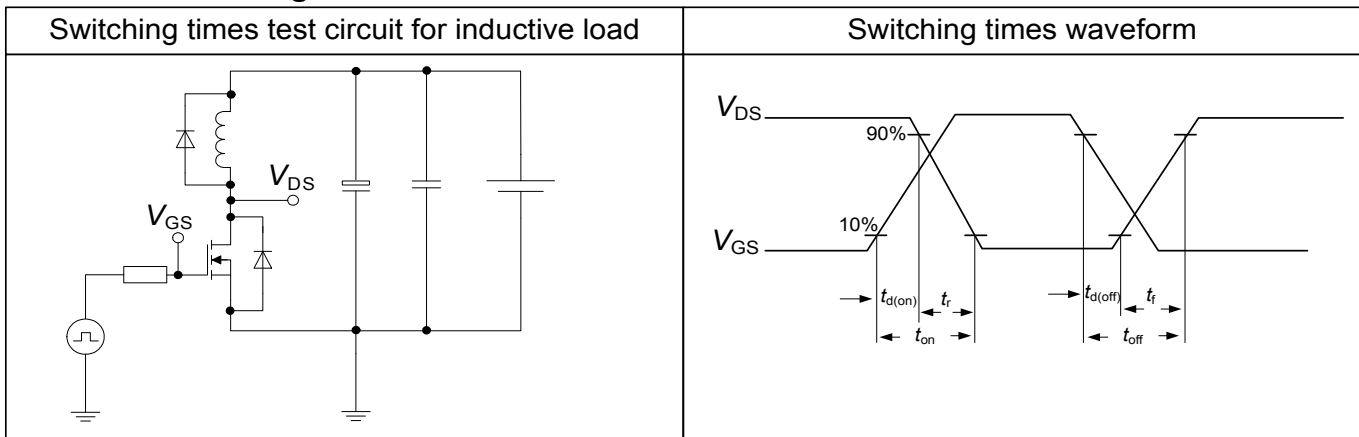
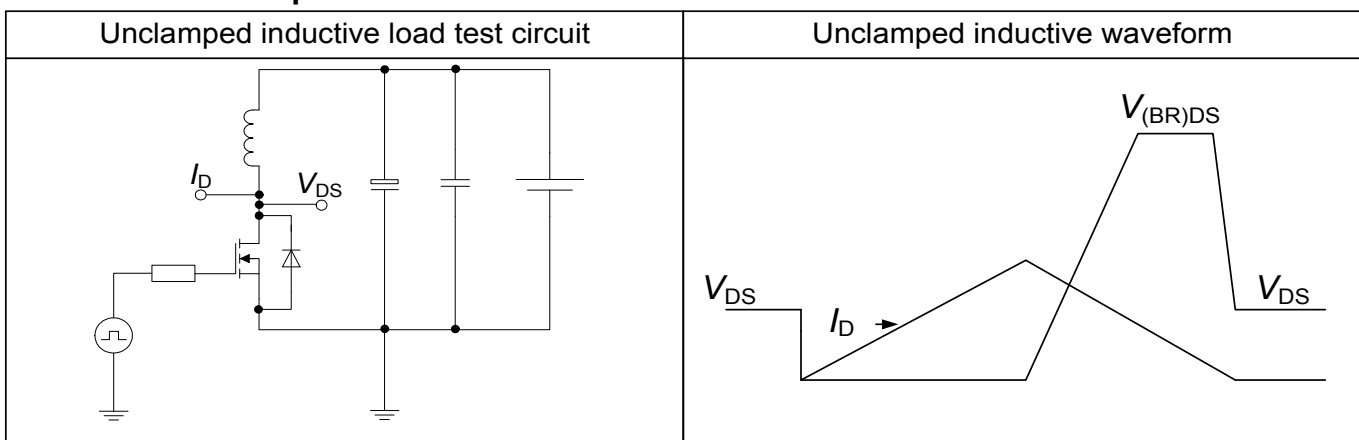


Table 10 Unclamped inductive load



6 Package Outlines

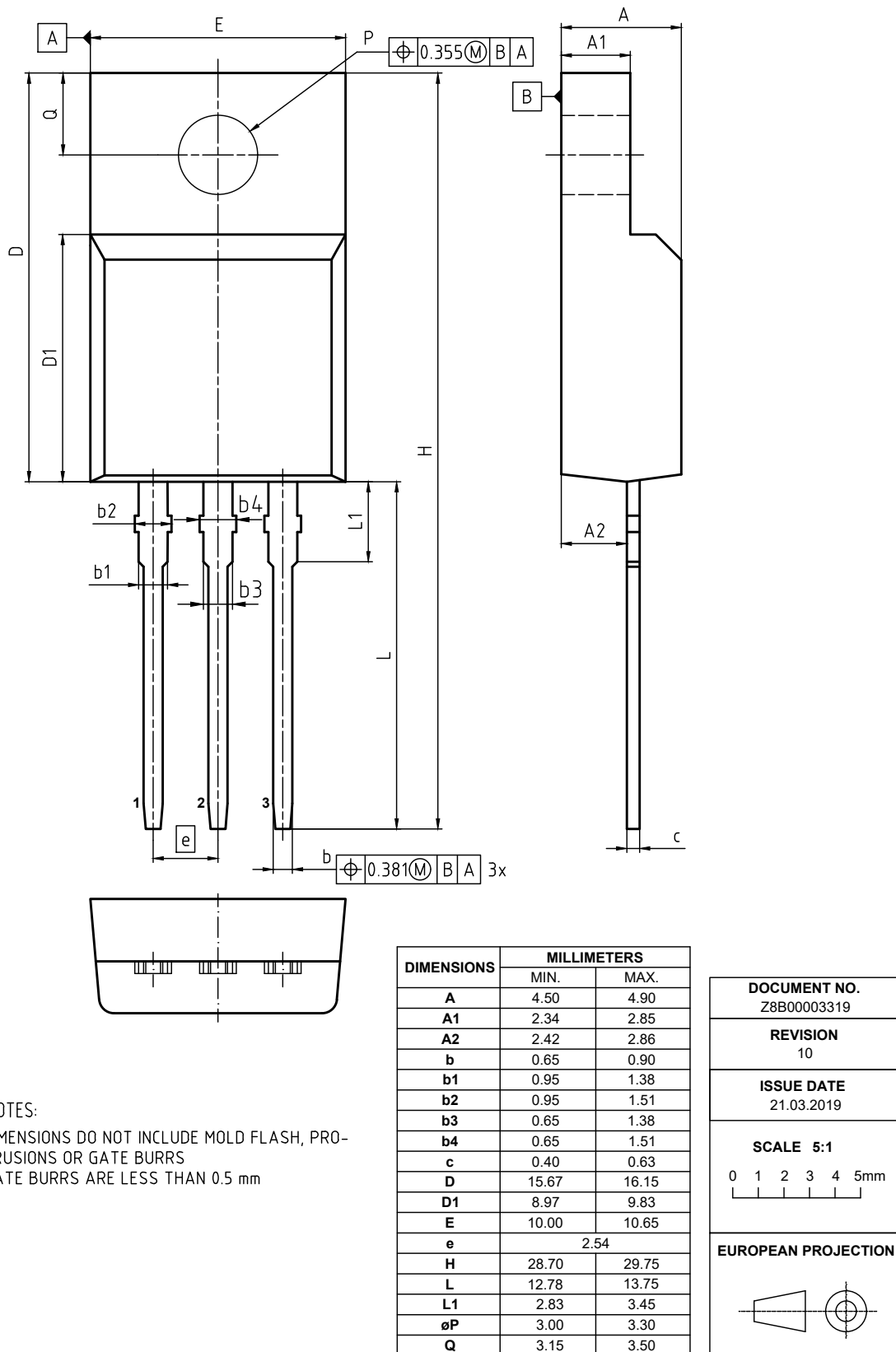


Figure 1 Outline PG-TO220 FullPAK, dimensions in mm

7 Appendix A

Table 11 Related Links

- IFX CoolMOS PFD7 950V Webpage: www.infineon.com
- IFX CoolMOS PFD7 950V application note: www.infineon.com
- IFX CoolMOS PFD7 950V simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPA95R130PFD7

Revision: 2022-04-22, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-03-18	Release of final version
2.1	2022-04-22	Modified features

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