ADuC845/ADuC847/ADuC848 MicroConverter® Quick Reference Guide

Instruction Set

Data Transfer Operations

		bytes	OSC periods
MOV A,Rn	move	1	1
MOV A,@Ri		1	2
MOV A,direct		2	2
MOV A,#data		2	2
MOV Rn,A		1	1
MOV Rn,direct		2	2
MOV Rn,#data		2	2
MOV direct,A		2	2
MOV direct,Rn		2	2
MOV direct,@Ri		2	2
MOV direct,direct		3	3
MOV direct,#data		3	3
MOV @Ri,A		1	2
MOV @Ri,direct		2	2
MOV @Ri,#data		2	2
MOV DPTR,#data16		3	3
MOVC A,@A+DPTR	move from code memory	1	4
MOVC A,@A+PC		1	4
MOVX A,@Ri	move to/from data memory	1	4
MOVX A,@DPTR		1	4
MOVX @Ri,A		1	4
MOVX @DPTR,A		1	4
PUSH direct	push onto stack	2	2
POP direct	pop from stack	2	2
XCH A,Rn	exchange bytes	1	1
XCH A,@Ri		1	2
XCH A,direct		2	2
XCHD A,@Ri	exchg low digits	1	2

Boolean Variable Manipulation

		bytes	OSC periods
CLR C	clear bit to zero	1	1
CLR bit		2	2
SETB C	set bit to one	1	1
SETB bit		2	2
CPL C	complement bit	1	1
CPL bit		2	2
ANL C,bit	AND bit with C	2	2
ANL C,/bit	AND (NOTbit) with C	2	2
ORL C,bit	OR bit with C	2	2
ORL C,/bit	OR (NOTbit) with C	2	2
MOV C,bit	move bit to bit	2	2
MOV bit,C		2	2

Program Branching

		bytes	OSC periods
ACALL addr11	call subroutine	2	3
LCALL addr16		3	4
RET	return from sub.	1	4
RETI	return from int.	1	4
AJMP addr11	jump	2	3
LJMP addr16		3	4
SJMP rel		2	3
JMP @A+DPTR		1	3
JC rel	jump if C set	2	3
JNC rel	jmp if C not set	2	3
JB bit,rel	jump if bit set	3	4
JNB bit,rel	jmp if bit not set	3	4
JBC bit,rel	jmp&clear if set	3	4
JZ rel	jump if A = 0	2	3
JNZ rel	jump if A not 0	2	3
CJNE A,direct,rel	compare and jump if not equal	3	4
CJNE A,#data,rel		3	4
CJNE Rn,#data,rel		3	4
CJNE @Ri,#data,rel		3	4
DJNZ Rn,rel	decrement and	2	3
DJNZ direct, rel	jump if not zero	3	4
NOP	no operation	1	1

Arithmetic Operations

		bytes	OSC periods
ADD A,Rn	add source to A	1	1
ADD A,@Ri		1	2
ADD A,direct		2	2
ADD A,#data		2	2
ADDC A,Rn	add with carry	1	1
ADDC A,@Ri		1	2
ADDC A,direct		2	2
ADDC A,#data		2	2
SUBB A,Rn	subtract from A with borrow	1	1
SUBB A,@Ri		1	2
SUBB A,direct		2	2
SUBB A,#data		2	2
INC A	increment	1	1
INC Rn		1	1
INC @Ri		1	2
INC direct		2	2
INC DPTR *		1	3
DEC A	decrement	1	1
DEC Rn		1	1
DEC @Ri		1	2
DEC direct		2	2
MUL AB	multiply A by B	1	9
DIV AB	divide A by B	1	9
DA A	decimal adjust	1	2

* INC DPTR increments the 24bit value DPP/DPH/DPL

Logical Operations

		bytes	OSC periods
ANL A,Rn	logical AND	1	1
ANL A,@Ri		1	2
ANL A,direct		2	2
ANL A,#data		2	2
ANL direct,A		2	2
ANL direct,#data		3	3
ORL A,Rn	logical OR	1	1
ORL A,@Ri		1	2
ORL A,direct		2	2
ORL A,#data		2	2
ORL direct,A		2	2
ORL direct,#data		3	3
XRL A,Rn	logical XOR	1	1
XRL A,@Ri		1	2
XRL A,direct		2	2
XRL A,#data		2	2
XRL direct,A		2	2
XRL direct,#data		3	3
CLR A	clear A to zero	1	1
CPL A	complement A	1	1
RL A	rotate A left	1	1
RLC A	...through C	1	1
RR A	rotate A right	1	1
RRC A	...through C	1	1
SWAP A	swap nibbles	1	1

Legend

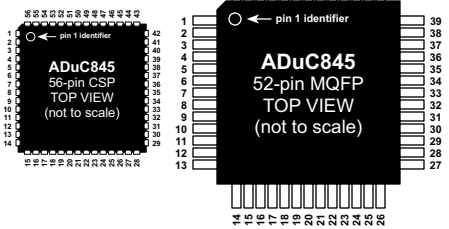
Rn	register addressing using R0-R7
@Ri	indirect addressing using R0 or R1
direct	8-bit internal address (00h-FFh)
#data	8-bit constant included in instruction
#data16	16-bit constant included in instruction
bit	8-bit direct address of bit
rel	signed 8-bit offset
addr11	11-bit address in current 2K page
addr16	16-bit address
x	any of: Rn, @Ri, direct, #data

Instructions That Affect Flags

ADD A,x	C = carry out of bit 7 AC = carry out of bit 3 OV = carry out of bit 6, but not 7	DA A	C = C *or* (x>100)
		RRC A	C = ACC.7
		RLC A	C = ACC.0
		SETB C	C = 1
		CLR C	C = 0
ADDC A,x	C = carry out of bit 7 AC = carry out of bit 3 OV = carry out of bit 6, but not 7	ANL C,bit	C = C *and* bit
		ANL C,/bit	C = C *and* NOTbit
		ORL C,bit	C = C *or* bit
		ORL C,/bit	C = C *or* NOTbit
		MOV C,bit	C = bit
SUBB A,x	C = borrow into bit 7 AC = borrow into bit 3 OV = borrow into bit 6, but not 7	CJNE x,y,rel	C = (x<y)
MUL AB	C = 0 OV = (result>255)		
DIV AB	C = 0 OV = divide by zero		

Pin Functions

MQFP	CSP	
2	1	P1.1 / AIN2
3	2	P1.2 / AIN3 / REFIN2+
4	3	P1.3 / AIN4 / REFIN2-
5	4	AV_{DD}
-	5	AGND
6	6	AGND
7	7	REFIN-
8	8	REFIN+
9	9	P1.4 / AIN5
10	10	P1.5 / AIN6
11	11	P1.6 / AIN7 / IEXC1
12	12	P1.7 / AIN8 / IEXC2
13	13	AINCOM / DAC
14	14	DAC

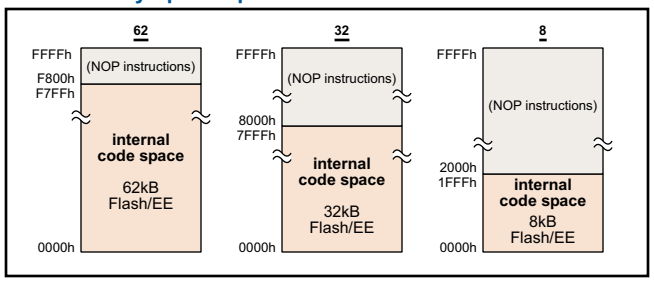


MQFP	CSP	
-	15	AIN9 (CSP package only)
-	16	AIN10 (CSP package only)
15	17	RESET
16	18	P3.0 / $\overline{RxD}$
17	19	P3.1 / $\overline{TxD}$
18	20	P3.2 / INT0
19	21	P3.3 / INT1
20	22	DV_{DD}
21	23	DGND
22	24	P3.4 / T0
23	25	P3.5 / T1
24	26	P3.6 / $\overline{WR}$
25	27	P3.7 / $\overline{RD}$
26	28	SCLK (I^2C)

MQFP	CSP	
27	29	SDATA (I^2C)
28	30	P2.0 / SCLOCK (SPI)
29	31	P2.1 / MOSI (SPI)
30	32	P2.2 / MISO (SPI)
31	33	P2.3 / $\overline{SS}$ / T2
32	34	XTAL1 (in)
33	35	XTAL2 (out)
34	36	DV_{DD}
35	37	DGND
-	38	DGND
36	39	P2.4 / T2EX
37	40	P2.5 / PWM0
38	41	P2.6 / PWM1
39	42	P2.7 / PWMCLK

MQFP	CSP	
40	43	$\overline{EA}$
41	44	$\overline{PSEN}$
42	45	ALE
43	46	P0.0 / AD0
44	47	P0.1 / AD1
45	48	P0.2 / AD2
46	49	P0.3 / AD3
47	50	DGND
48	51	DV_{DD}
49	52	P0.4 / AD4
50	53	P0.5 / AD5
51	54	P0.6 / AD6
52	55	P0.7 / AD7
1	56	P1.0 / AIN1

Code Memory Space Options



Interrupt Vector Addresses

Interrupt Bit	Interrupt Name	Vector Address	Relative Priority
PSMCON.5	Power Supply Monitor Interrupt	43h	1
WDS	WatchDog Timer Interrupt	5Bh	2
IE0	External Interrupt 0	03h	3
RDY0/RDY1	End of ADC Conversion Interrupt	33h	4
TF0	Timer0 Overflow Interrupt	0Bh	5
IE1	External Interrupt 1	13h	6
TF1	Timer1 Overflow Interrupt	1Bh	7
ISPI/I2CI	SPI/I^2C Interrupt	3Bh	8
RI/TI	UART Interrupt	23h	9
TF2/EXF2	Timer2 Interrupt	2Bh	10
TIMECON.2	Time Interval Counter Interrupt	53h	11

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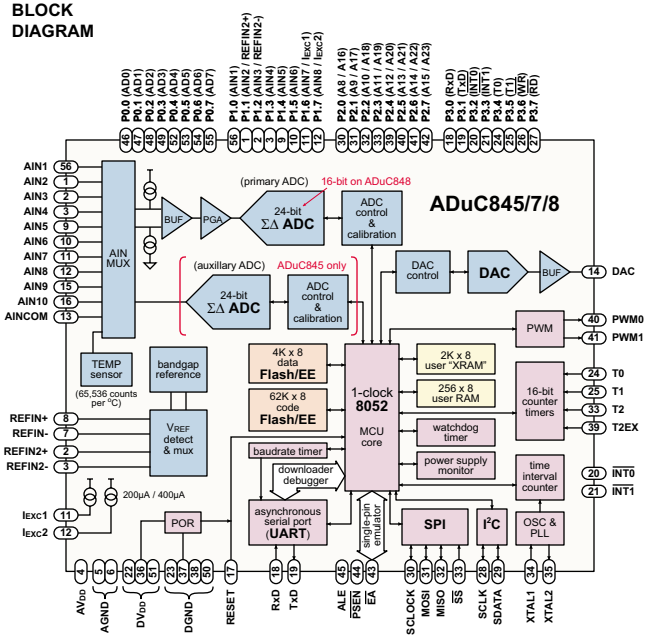
FUNCTIONAL BLOCK DIAGRAM



* pin numbers refer to CSP package

A *Precision Analog* Flash MCU

The ADuC845/ADuC847/ADuC848 is:

ADC:
24-bit* primary ADC, differential w/ programmable gain
24-bit auxiliary ADC, single-ended w/ fixed gain (ADuC845 only)
10-channel input mux (*ADC is 16bit on ADuC848)

DAC:
12-bit, 15µs, voltage output
<1LSB DNL

Flash/EEPROM:
up to 62kB Flash/EE program memory
4kB Flash/EE data memory

Microcontroller:
"single-cycle" 8052, up to 12.6MIPS
32 I/O lines, programmable PLL clock
(98.3kHz to 12.6MHz from 32kHz crystal)

Embedded Tools Support:
on-chip download/debug & single-pin emulation functions

Other on-chip features:
temperature sensor, power supply monitor, watchdog timer, flexible serial interface ports, voltage reference, time interval counter, dual 8-/16-bit PWM, power-on-reset

REV. 0

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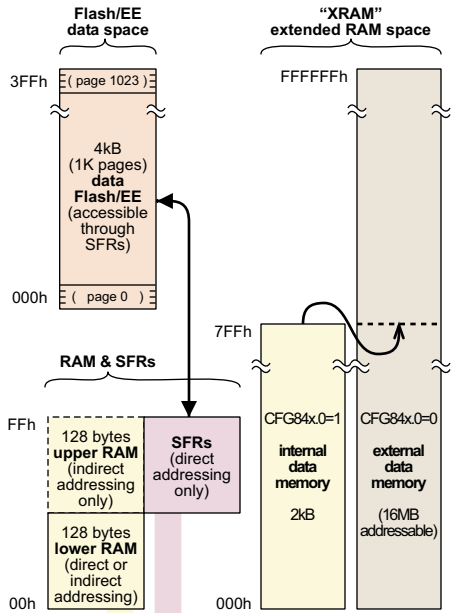
Data Memory: RAM, SFRs, user Flash/EE (all read/write)

Lower RAM

decimal address	HEX address		MSB address			(bit addresses)			LSB address
127	7Fh	General Purpose Area							
...	...								
48	30h								
47	2Fh	Bit Addressable Area	7Fh	7Eh	7Dh	7Ch	7Bh	7Ah	79h	78h
46	2Eh		77h	76h	75h	74h	73h	72h	71h	70h
45	2Dh		6Fh	6Eh	6Dh	6Ch	6Bh	6Ah	69h	68h
44	2Ch		67h	66h	65h	64h	63h	62h	61h	60h
43	2Bh		5Fh	5Eh	5Dh	5Ch	5Bh	5Ah	59h	58h
42	2Ah		57h	56h	55h	54h	53h	52h	51h	50h
41	29h		4Fh	4Eh	4Dh	4Ch	4Bh	4Ah	49h	48h
40	28h		47h	46h	45h	44h	43h	42h	41h	40h
39	27h		3Fh	3Eh	3Dh	3Ch	3Bh	3Ah	39h	38h
38	26h		37h	36h	35h	34h	33h	32h	31h	30h
37	25h		2Fh	2Eh	2Dh	2Ch	2Bh	2Ah	29h	28h
36	24h		27h	26h	25h	24h	23h	22g	21h	20h
35	23h		1Fh	1Eh	1Dh	1Ch	1Bh	1Ah	19h	18h
34	22h		17h	16h	15h	14h	13h	12h	11g	10h
33	21h		0Fh	0Eh	0Dh	0Ch	0Bh	0Ah	09h	08h
32	20h		07h	06h	05h	04h	03h	02h	01h	00h
31	1Fh	R7	Register Bank 3							
30	1Eh	R6								
29	1Dh	R5								
28	1Ch	R4								
27	1Bh	R3								
26	1Ah	R2								
25	19h	R1								
24	18h	R0								
23	17h	R7	Register Bank 2							
22	16h	R6								
21	15h	R5								
20	14h	R4								
19	13h	R3								
18	12h	R2								
17	11h	R1								
16	10h	R0								
15	0Fh	R7	Register Bank 1							
14	0Eh	R6								
13	0Dh	R5								
12	0Ch	R4								
11	0Bh	R3								
10	0Ah	R2								
9	09h	R1								
8	08h	R0								
7	07h	R7	Register Bank 0							
6	06h	R6								
5	05h	R5								
4	04h	R4								
3	03h	R3								
2	02h	R2								
1	01h	R1								
0	00h	R0								



lower RAM details

SFR details

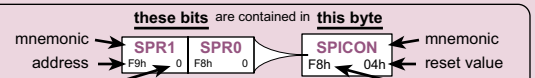
SFR Map

(reserved)	SPIDAT 00h F7h	(reserved)	(reserved)	PSMCON DFh	PLLCON 53h D7h	(reserved)	EADRH 00h C7h	EDATA4 00h BFh	SPH 00h B7h	CFG845/7/8 00h AFh	DPCON 00h A7h	EWAIT 00h 9Fh	(reserved)	(reserved)	PCON 00h 87h
(reserved)	(reserved)	(reserved)	ADC0CON2 00h E6h	ADC1L 00h DEh	(reserved)	(reserved)	EADRL 00h C6h	EDATA3 00h BEh	(reserved)	PWMCON 00h AEh	INTVAL 00h A6h	T3CON 00h 9Eh	(reserved)	(reserved)	(reserved)
DACCON 00h FDh	(reserved)	GN1H *xxh EDh	OF1H *xxh E5h	ADC1H 00h DDh	ICON 00h 0h	TH2 00h CDh	(reserved)	EDATA2 00h BDh	(reserved)	(reserved)	HOUR 00h A5h	T3FD 9Dh	(reserved)	(reserved)	TH1 00h 8Dh
DACH 00h FCh	(reserved)	GN1L *xxh ECh	OF1L *xxh E4h	ADC1M 00h DCh	SF 45h D4h	TL2 00h CCh	(reserved)	EDATA1 00h BCh	PWM1H 00h B4h	(reserved)	MIN 00h A4h	SEC 00h A3h	I2CADD 55h 9Bh	(reserved)	TH0 00h 8Ch	DPP 00h 84h
DACL 00h FBh	(not used)	GN0H *xxh EBh	OF0H *xxh E3h	ADC0H 00h DBh	ADC1CON 00h D3h	RCAP2H 00h CBh	(reserved)	(reserved)	PWM1L 00h B3h	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	TL1 00h 8Bh	DPH 00h 83h
(reserved)	I2CADD1 7Fh F2h	GN0M *xxh EAh	OF0M *xxh E2h	ADC0M 00h DAh	ADC0CON1 07h D2h	RCAP2L 00h CAh	CHIPID AXh C2h	(reserved)	PWM0H 00h B2h	HTHSEC 00h A2h	I2CDAT 00h 9Ah	(reserved)	(reserved)	TL0 00h 8Ah	DPL 00h 82h
(reserved)	GN0L *xxh E9h	OF0L *xxh E1h	ADC0L 00h D9h	ADCMODE 08h D1h	PSW 00h D0h	T2CON 00h C8h	(reserved)	ECON 00h B9h	PWM0L 00h B1h	IEIP2 A0h A9h	TIMECON 00h A1h	SBUF 00h 99h	SCON 00h 98h	P1 FFh 90h	TCON 00h 88h	TMOD 00h 89h	SP 07h 81h
SPICON 05h F8h	B 00h F0h	I2CCON 00h E8h	ACC 00h E0h	ADCSTAT 00h D8h	PSW 00h D0h	T2CON 00h C8h	WDCON 10h C0h	IP 00h B8h	P3 FFh B0h	IE 00h A8h	P2 FFh A0h	SCON 00h 98h	P1 FFh 90h	TCON 00h 88h	P0 FFh 80h

SPR0 0 F8h	SPR1 0 F9h	CPHA 1 FAh	CPOL 0 FBh	SPIM 0 FCh	SPE 0 FDh	WCOL 0 FEh	ISPI 0 FFh	F8h
I2CI 0 E8h	I2CTX 0 E9h	I2CRS 0 EAh	I2CM 0 EBh	MDI 0 ECh	MCO 0 EDh	MDE 0 EEh	MDO 0 EFh	F7h
P 0 D0h	F1 0 D1h	OV 0 D2h	RS0 0 D3h	RS1 0 D4h	F0 0 D5h	AC 0 D6h	CY 0 D7h	E8h
CAP2 0 C8h	CNT2 0 C9h	TR2 0 CAh	EXEN2 0 CBh	TCLK 0 CCh	RCLK 0 CDh	PRE1 0 CEh	PRE2 0 CFh	E7h
WDWR 0 C0h	WDE 0 C1h	WDS 0 C2h	WDIR 0 C3h	PRE0 1 C4h	PRE1 0 C5h	PRE2 0 C6h	PRE3 0 C7h	E0h
PX0 0 B8h	PT0 0 B9h	PX1 0 BAh	PT1 0 BBh	PS 0 BCh	PT2 0 BDh	PADC 0 BEh	RD 1 B8h	D8h
RXD 1 B0h	TXD 1 B1h	INT0 1 B2h	INT1 1 B3h	T0 1 B4h	T1 1 B5h	WR 1 B6h	EADC 0 AEh	D0h
EX0 0 A8h	ET0 0 A9h	EX1 0 AAh	ET1 0 ABh	ES 0 ACh	ET2 0 ADh	EA 0 AFh	A8h	C8h
A0h	A1h	A2h	A3h	A4h	A5h	A6h	A7h	B8h
RI 0 98h	TI 0 99h	RB8 0 9Ah	TB8 0 9Bh	REN 0 9Ch	SM2 0 9Dh	SM1 0 9Eh	SM0 0 9Fh	98h
T2 1 90h	T2EX 1 91h	IT1 0 92h	IE1 0 93h	TR0 0 94h	TF0 0 95h	TR1 0 96h	TF1 0 97h	90h
IT0 0 88h	IE0 0 89h	IT1 0 8Ah	TR0 0 8Bh	IE1 0 8Ch	TF0 0 8Dh	TR1 0 8Eh	TF1 0 8Fh	88h
80h	81h	82h	83h	84h	85h	86h	87h	F8h

MAP KEY

these bits are contained in this byte



* calibration coefficients are preconfigured at power-up to factory-calibrated values

ADCMODE ADC Mode register
- ADCMODE.6 60Hz reject filter enable (0=disable)
- ADCMODE.5 primary ADC enable bit (0=disable)
- ADCMODE.4 auxiliary ADC enable bit (0=disable)
- ADCMODE.3 chop mode disable bit (1=disable)
- ADCMODE.2 ADC mode bits: [off, idle, single-conv, continuous-conv, zero-cal, fs-cal, sys-zero-cal, sys-fs-cal]
- ADCMODE.1
- ADCMODE.0

ADCSTAT ADC Status register
- RDY0 ADC0 ready indicator flag
- RDY1 ADC1 ready indicator flag
- CAL calibration start control bit (set to begin cal)
- NOXREF no external reference flag (only valid if ADC active)
- ERR0 primary ADC error flag (indicates result is clamped)
- ERR1 auxiliary ADC error flag (indicates result is clamped)

ADC0CON1 ADC0 Control register #1
- ADC0CON1.7 buffer configuration bits: [0=buffered, 10=unbuffered, others reserved]
- ADC0CON1.6
- ADC0CON1.5 unipolar select bit (0=bipolar)
- ADC0CON1.2 range select bits: [±20mV, ±40mV, ±80mV, ±160mV, ±320mV, ±640mV, ±1.28V, ±2.56V]
- ADC0CON1.1
- ADC0CON1.0

ADC0CON2 ADC0 Control register #2
- ADC0CON2.7 reference select bits [internal, REFIN pins, REFIN2 pins, reserved]
- ADC0CON2.6
- ADC0CON2.3 channel select bits [1-COM, 2-COM, 3-COM, 4-COM, 5-COM, 6-COM, 7-COM, 8-COM, 9-COM, 10-COM, COM-COM]
- ADC0CON2.2
- ADC0CON2.1
- ADC0CON2.0 1-2, 3-4, 5-6, 7-8, 9-10, COM-COM

ADC1CON ADC1 Control register
- ADC1CON.6 REFIN select bit (0=internal reference)
- ADC1CON.5 unipolar select bit (0=bipolar)
- ADC1CON.3 channel select bits [1-COM, 2-COM, 3-COM, 4-COM, 5-COM, 6-COM, 7-COM, 8-COM, 9-COM, 10-COM, COM-COM]
- ADC1CON.2
- ADC1CON.1
- ADC1CON.0 1-2, 3-4, 5-6, 7-8, tempsens, COM-COM

SF Sync Filter Register:
$f_{ADC} = 4.096Hz / (3 \cdot SF)$ (chop on)
$f_{ADC} = 4.096Hz / (SF)$ (chop off)

OF0H,OF0M,OF0L ADC0 offset coefficient

OF1H,OF1L ADC1 offset coefficient

GN0H,GN0M,GN0L ADC0 gain coefficient

GN1H,GN1L ADC1 gain coefficient

ADC0H,ADC0M,ADC0L ADC0 data

ADC1H,ADC1M,ADC1L ADC1 data

ICON Current Source Control Register
- ICON.6 burnout current enable bit (0=disable)
- ICON.3 IEXC2 pin select bit [0=AIN8 / 1=AIN7]
- ICON.2 IEXC1 pin select bit [0=AIN7 / 1=AIN8]
- ICON.1 IEXC2 enable bit (0=disable)
- ICON.0 IEXC1 enable bit (0=disable)

DACCON DAC Control register
- DACCON.4 DAC pin select bit [0=DAC pin, 1=AINCOM pin]
- DACCON.3 ModeSelect (0=12bit, 1=8bit)
- DACCON.2 RangeSelect (0=2.5V, 1=AV_{DD})
- DACCON.1 Clear DAC (0=0V, 1=normal operation)
- DACCON.0 PowerDown DAC (0=off, 1=on)

DACH,DACL DAC data registers

PLLCON PLL Control register
- PLLCON.7 oscillator powerdown control bit (0=XTAL on)
- PLLCON.6 PLL lock indicator flag (0=out of lock)
- PLLCON.4 returns state of EA pin latched at power-up
- PLLCON.3 "fast interrupt" control bit (0=normal)
- PLLCON.2 3-bit clock divider value, "CD" (default=3):
- PLLCON.1
- PLLCON.0

$F_{CORE} = 12,582,912Hz / 2^{CD}$

TIMECON Time Interval Counter Control Register
- TIMECON.6 24-hour mode select (0=0..255hour, 1=0..23hour)
- TIMECON.5 INTVAL timebase select bits
- TIMECON.4 [128th sec, seconds, minutes, hours]
- TIMECON.3 single time interval control bit (0=reload&restart)
- TIMECON.2 time interval interrupt bit, "TII"
- TIMECON.1 time interval enable bit (0=disable&clear)
- TIMECON.0 time clock enable bit (0=disable)

INTVAL TIC Interval Register

HTHSEC TIC Elapsed 128th Second Register

SEC TIC Elapsed Seconds Register

MIN TIC Elapsed Minutes Register

HOUR TIC Elapsed Hours Register

ECON Data Flash/EE comand register

01h	READ page	81h	READ byte
02h	PROGRAM page	82h	PROGRAM byte
04h	VERIFY page	0Fh	EXIT ULOAD mode
05h	ERASE page	F0h	ENTER ULOAD mode
06h	ERASE ALL		(all others reserved)

EADRH,EADRL Data Flash/EE address registers

EDATA1,EDATA2,EDATA3,EDATA4 Data Flash/EE data registers

SPICON SPI Control register
- ISPI SPI interrupt (set by hardware at end of SPI transfer)
- WCOL collision error flag
- SPE SPI enable (0=I^2C enable, 1=SPI enable)
- SPIM master mode select (0=slave)
- CPOL polarity select (0=SCLK idles low)
- CPHA clock phase select (0=leading edge latch)
- SPR1 SPI bitrate select bits
- SPR0 bitrate = F_{CORE} / [2,4,8,16] (slave: SPR0=SS)

SPIDAT SPI Data register

I2CCON I^2C Control register
- MDO master mode SDATA output bit
- MDE master mode SDATA output enable (0=disable)
- MCO master mode SCLK output bit
- MDI master mode SDATA input bit
- I2CM master mode select bit (0=slave mode)
- I2CRS serial port reset
- I2CTX transmission direction status (0=RX,1=TX)
- I2CI serial interface interrupt

I2CADD,I2CADD1 I^2C slave Address registers

I2CDAT I^2C Data register

PWMCON PWM Control register
- PWMCON.6 PWM mode bits [0=disabled, 1=single/var.res., 2=twin/8bit, 3=twin/16bit, 4=dual/16bitNRZ, 5=dual/8bit, 6=dual/16bitRZ, 7=reset/disable]
- PWMCON.5
- PWMCON.4
- PWMCON.3 PWM clock divide bits
- PWMCON.2 PWM counter = clock / [1,4,16,64]
- PWMCON.1 PWM clock source bits [0=F_{XTAL}/15, 1=F_{XTAL}, 2=ext.clk. on P2.7, 3=F_{VCO}(12.583MHz)]
- PWMCON.0

PWM0H,PWM0L PWM0 data registers

PWM1H,PWM1L PWM1 data registers

DPCON Data Pointer Control register
- DPCON.6 data pointer auto-toggle enable (0=disable)
- DPCON.5 shadow data pointer mode control bits
- DPCON.4 [1=8052, 2=post-inc, 3=post-dec, 4=LSBtgl]
- DPCON.3 main data pointer mode control bits
- DPCON.2 [1=8052, 2=post-inc, 3=post-dec, 4=LSBtgl]
- DPCON.1 (not implemented to allow INC DPCON toggling)
- DPCON.0 data pointer select [0=main, 1=shadow]

T3CON Timer 3 Control register
- T3CON.7 Timer 3 baud rate enable (0=disable)
- T3CON.2 binary divide factor (DIV)
- T3CON.1 DIV = log[F_{CORE}/(16·baudrate)] / log2
- T3CON.0 (rounded down)

T3FD Timer 3 Fractional Divider register

T3FD = $(2 \cdot F_{CORE}) / (baudrate \cdot 2^{(DIV-1)}) - 64$

CHIPID Chip ID Register (AX hex = ADuC845/7/8)

CFG845/CFG847/CFG848 Config. Register
- CFG84x.7 extended stack-pointer enable (0=disable)
- CFG84x.0 internal XRAM select (0=external XRAM)

WDCON Watchdog Timer control register
- PRE3 watchdog timeout selection bits
- PRE2 0-7=[15.6,31.2,62.5,125,250,500,1000,2000]ms
- PRE1 8=0ms (immediate reset)
- PRE0 >8=reserved
- WDIR watchdog interrupt response bit
- WDS watchdog status flag (1 indicates watchdog timeout)
- WDE watchdog enable control (0=disabled)
- WDWR watchdog write enable bit (set to enable write)

PSMCON Power Supply Monitor control register
- PSMCON.7 DV_{DD} status bit (1=above / 0=below trip point)
- PSMCON.6 AV_{DD} status bit (1=above / 0=below trip point)
- PSMCON.5 PSM interrupt bit
- PSMCON.4 DV_{DD} trip point select bits
- PSMCON.3 [4.63V, 3.08V, 2.93V, 2.63V]
- PSMCON.2 AV_{DD} trip point select bits
- PSMCON.1 [4.63V, 3.08V, 2.93V, 2.63V]
- PSMCON.0 PSM enable (1=on / 0=off)

SP Stack Pointer

SPH Stack Pointer High byte

IE Interrupt Enable register #1
- EA enable interrupts (0=all interrupts disabled)
- EADC enable ADCI (ADC interrupt)
- ET2 enable TF2/EXF2 (Timer2 overflow interrupt)
- ES enable RI/TI (serial port interrupt)
- ET1 enable TF1 (Timer1 overflow interrupt)
- EX1 enable IE1 (external interrupt 1)
- ET0 enable TF0 (Timer0 overflow interrupt)
- EX0 enable IE0 (external interrupt 0)

IEIP2 Interrupt Enable/Priority register #2
- IEIP2.6 priority of TII interrupt (time interval)
- IEIP2.5 priority of PSMI interrupt (power supply monitor)
- IEIP2.4 priority of ISPI/I2CI interrupt (serial interface)
- IEIP2.3 (this bit must contain zero)
- IEIP2.2 enable TII interrupt (time interval)
- IEIP2.1 enable PSMI interrupt (power supply monitor)
- IEIP2.0 enable ISPI/I2CI interrupt (serial interface)

IP Interrupt Priority register
- PADC priority of ADCI (ADC interrupt)
- PT2 priority of TF2/EXF2 (Timer2 overflow interrupt)
- PS priority of RI/TI (serial port interrupt)
- PT1 priority of TF1 (Timer1 overflow interrupt)
- PX1 priority of IE1 (external interrupt 1)
- PT0 priority of TF0 (Timer0 overflow interrupt)
- PX0 priority of IE0 (external interrupt 0)

TMOD Timer Mode register
- TMOD.3/.7 gate control bit (0=ignore INTx)
- TMOD.2/.6 counter/timer select bit (0=timer)
- TMOD.1/.5 timer mode selecton bits [13bIT, 16bIT/C, 8bIT/Creload, 2x8bIT] (upper nibble = Timer1, lower nibble = Timer0)

TCON Timer Control register
- TF1 Timer1 overflow flag (auto cleared on vector to ISR)
- TR1 Timer1 run control (0=off, 1=run)
- TF0 Timer0 overflow flag (auto cleared on vector to ISR)
- TR0 Timer0 run control (0=off, 1=run)
- IE1 external INT1 flag (auto cleared on vector to ISR)
- IT1 IE1 type (0=level trig, 1=edge trig)
- IE0 external INT0 flag (auto cleared on vector to ISR)
- IT0 IE0 type (0=level trig, 1=edge trig)

TH0,TL0 Timer0 registers

TH1,TL1 Timer1 registers

T2CON Timer2 Control register
- TF2 overflow flag
- EXF2 external flag
- RCLK receive clock enable (0=Timer1 used for RxD clk)
- TCLK transmit clock enable (0=Timer1 used for TxD clk)
- EXEN2 external enable (0=ignore T2EX, 1=cap/rld on T2EX)
- TR2 run control (0=stop, 1=run)
- CNT2 timer/counter select (0=timer, 1=counter)
- CAP2 capture/reload select (0=reload, 1=capture)

TH2,TL2 Timer2 register

RCAP2H,RCAP2L Timer2 Reload/Capture

P0 Port0 register (also A0-A7 & D0-D7)

P1 Port1 register (analog & digital inputs)
- T2EX timer/counter 2 capture/reload trigger
- T2 timer/counter 2 external input

P2 Port2 register (also A8-A15 & A16-A23)

P3 Port3 register
- RD external data memory read strobe
- WR external data memory write strobe
- T1 timer/counter 1 external input
- T0 timer/counter 0 external input
- INT1 external interrupt 1
- INT0 external interrupt 0
- TxD serial port transmit data line
- RxD serial port receive data line

SCON Serial communications Control register
- SM0 UART mode control bits
- SM1 00 - 8bit shift register - F_{CORE}/12; 01 - 8bit UART - variable; 10 - 9bit UART - F_{CORE}/64(x2); 11 - 9bit UART - variable
- SM2 in modes 2&3, enables multiprocessor communication
- REN receive enable control bit
- TB8 in modes 2&3, 9th bit transmitted
- RB8 in modes 2&3, 9th bit received
- TI transmit interrupt flag
- RI receive interrupt flag

SBUF Serial port Buffer register

PCON Power Control register
- PCON.7 double baud rate control
- PCON.4 ALE disable (0=normal, 1=forces ALE high)
- PCON.3 general purpose flag
- PCON.2 general purpose flag
- PCON.1 power-down control bit (recoverable with hard reset)
- PCON.0 idle-mode control (recoverable with enabled interrupt)

PSW Program Status Word
- CY carry flag
- AC auxiliary carry flag
- F0 general purpose flag 0
- RS1 register bank select control bits
- RS0 active register bank = [0,1,2,3]
- OV overflow flag
- F1 general purpose flag 1
- P parity of ACC

DPP Data Pointer Page

DPH,DPL (DPTR) Data Pointer

ACC Accumulator

B auxiliary math register