



## Features

- ESD Protect for 2 high-speed I/O channels
- Provide ESD protection for each channel to IEC 61000-4-2 (ESD)  $\pm 15\text{kV}$  (air),  $\pm 10\text{kV}$  (contact) IEC 61000-4-5 (Lightning) 3.5A (8/20 $\mu\text{s}$ )
- **Ultra low capacitance: 0.35pF typical**
- For low operating voltage applications: **3.3V**
- **Ultra-small DFN1006P3X package** (1.0mmx0.6mmx0.45mm) saves board space
- Fast turn-on and Low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green Part**

## Applications

- USB 3.0
- USB 2.0
- MHL (Mobile High-Definition Link)
- HDMI
- DisplayPort interface
- SATA and eSATA interface
- Mobile Phones
- Hand Held Portable Applications

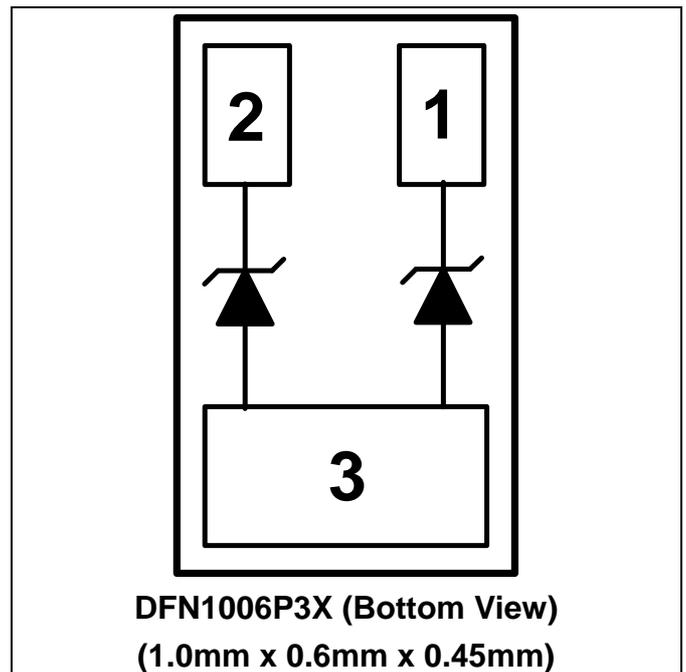
## Description

AZ5313-02F is a design which includes two uni-directional ESD rated clamping cells to protect high speed data interfaces. The AZ5313-02F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD), Lightning, and Cable Discharge Event (CDE).

AZ5313-02F is a unique design which includes proprietary clamping cells in a small package. During transient conditions, the proprietary clamping cells prevent over-voltage on the control/data/power lines, protecting any downstream components.

AZ5313-02F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ( $\pm 15\text{kV}$  air,  $\pm 8\text{kV}$  contact discharge).

## Circuit Diagram / Pin Configuration





## SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	SYMBOL	RATING	UNITS
Peak Pulse Current (tp=8/20μs)	I <sub>PP</sub>	3.5	A
Operating Voltage (pin-1,-2 to pin-3)	V <sub>DC</sub>	3.6	V
ESD per IEC 61000-4-2 (Air)	V <sub>ESD</sub>	±15	kV
ESD per IEC 61000-4-2 (Contact)		±10	
Lead Soldering Temperature	T <sub>SOL</sub>	260 (10 sec.)	°C
Operating Temperature	T <sub>OP</sub>	-55 to +85	°C
Storage Temperature	T <sub>STO</sub>	-55 to +150	°C

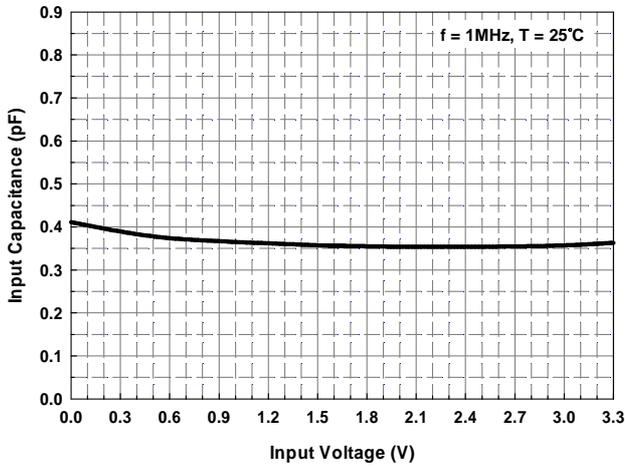
ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MINI	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V <sub>RWM</sub>	Pin-1, -2 to pin-3, T = 25 °C.			3.3	V
Reverse Leakage Current	I <sub>CH-Leak</sub>	V <sub>Pin-1,-2</sub> = 3.3V, V <sub>Pin-3</sub> = 0V, T = 25 °C.			1	μA
Reverse Breakdown Voltage	V <sub>BV</sub>	I <sub>BV</sub> = 1mA, T = 25 °C, pin-1, -2 to pin-3.	4.5			V
Forward Voltage	V <sub>F</sub>	I <sub>F</sub> = 15mA, T = 25 °C, pin-3 to pin-1, -2.	0.6		1.2	V
ESD Clamping Voltage (Note 1)	V <sub>clamp</sub>	IEC 61000-4-2 +8kV (I <sub>TLP</sub> = 16A), Contact mode, T = 25 °C, pin-1, -2 to pin-3.		9.5		V
ESD Dynamic Turn-on Resistance	R <sub>dynamic</sub>	IEC 61000-4-2 0~+8kV, T = 25 °C, Contact mode, pin-1, -2 to pin-3.		0.25		Ω
Channel Input Capacitance	C <sub>IN</sub>	V <sub>Pin-3</sub> = 0V, V <sub>IN</sub> = 1.65V, f = 1MHz, T = 25 °C, pin-1, -2 to pin-3.		0.35	0.5	pF
Channel to Channel Input Capacitance	C <sub>CROSS</sub>	V <sub>pin-3</sub> = 0V, V <sub>IN</sub> = 1.65V, f = 1MHz, T = 25 °C, between I/O pins.		0.04	0.08	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

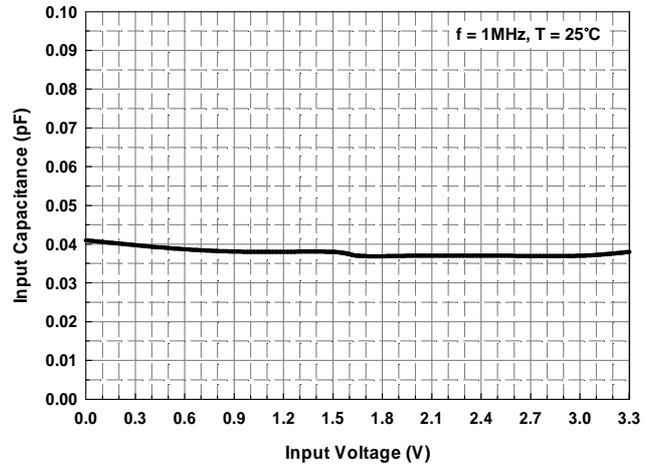
TLP conditions: Z<sub>0</sub>= 50Ω, t<sub>p</sub>= 100ns, t<sub>r</sub>= 1ns.

## Typical Characteristics

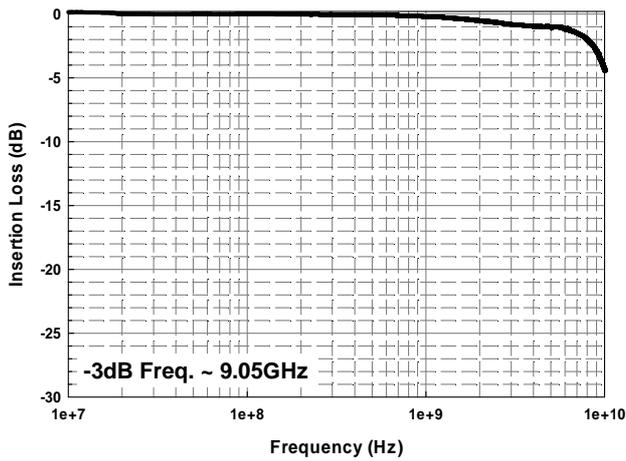
Typical Variation of  $C_{IN}$  vs.  $V_{IN}$



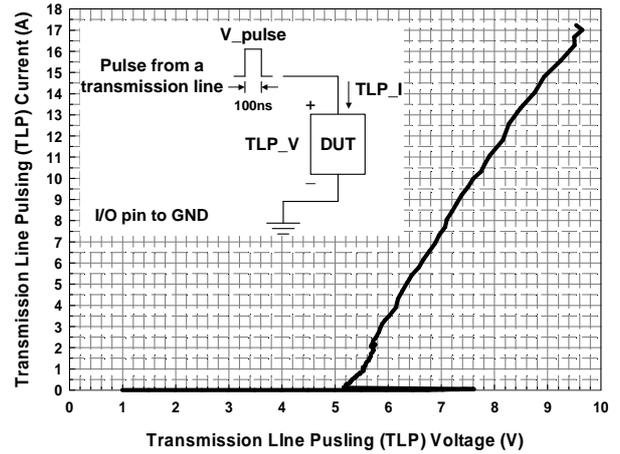
Typical Variation of  $C_{IO-to-IO}$  vs.  $V_{IN}$



Insertion Loss  $S_{DD}$



Transmission Line Pulsing (TLP) Measurement



## Applications Information

### A. Device Connection

The AZ5313-02F is designed to protect two data lines from transient over-voltage (such as ESD stress pulse). The device connection of AZ5313-02F is shown in the Fig. 1. In Fig. 1, the two protected data lines are connected to the ESD protection pins (pin1, pin2) of AZ5313-02F. The ground pin (pin3) of AZ5313-02F is a

negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible.

AZ5313-02F can provide protection for 2 I/O signal lines simultaneously. If the number of I/O signal lines is less than 2, the unused I/O pin can be simply left as NC pin.

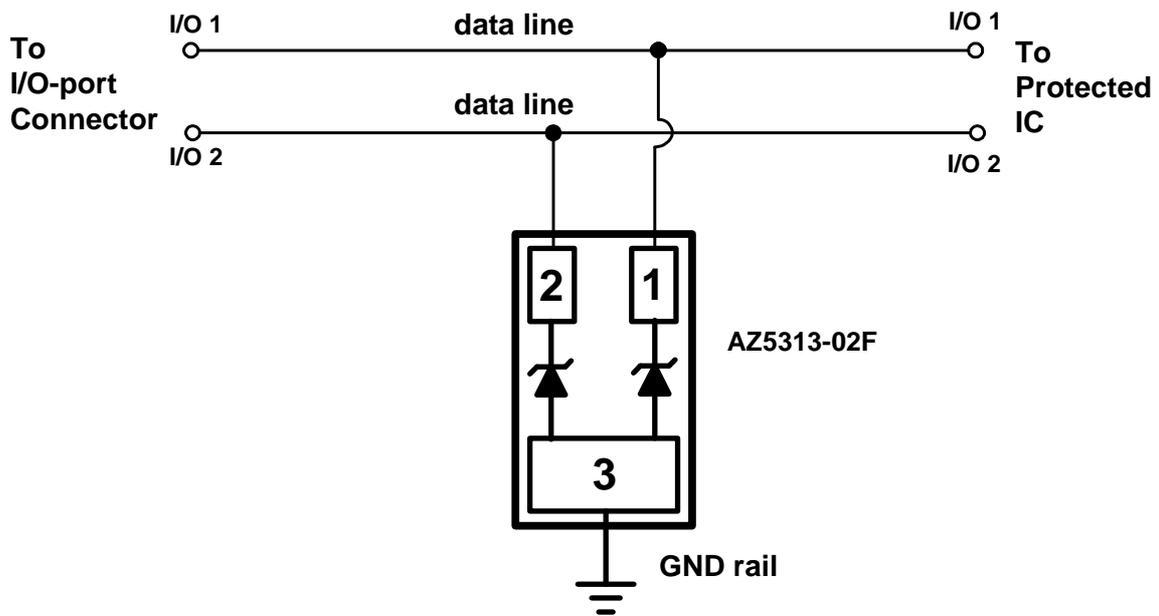
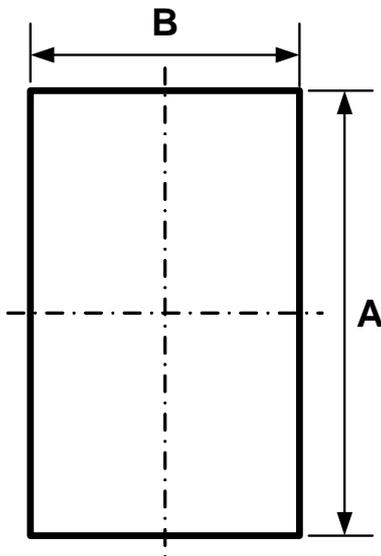


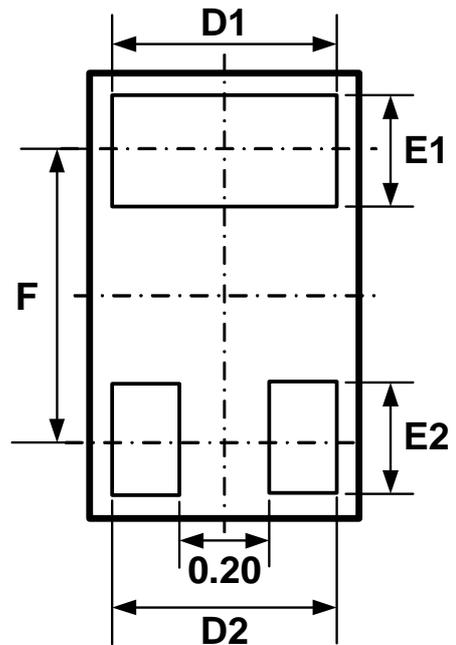
Fig. 1 Data lines connection of AZ5313-02F.

## Mechanical Details

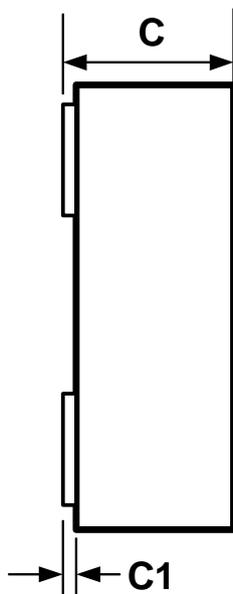
### DFN1006P3X PACKAGE DIAGRAMS AND DIMENSIONS



TOP VIEW



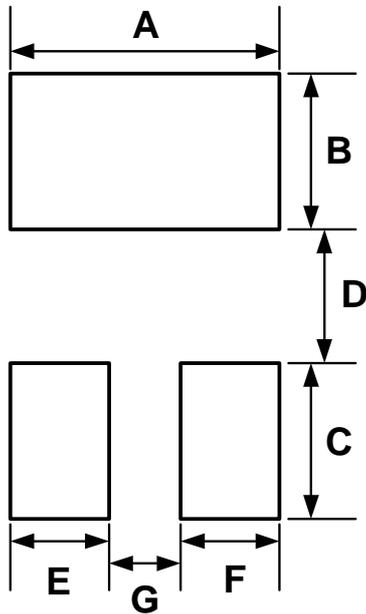
BOTTOM VIEW (unit in mm)



SIDE VIEW

SYMBOL	Millimeters	
	MIN.	MAX.
A	0.95	1.05
B	0.55	0.65
C	0.40	0.55
C1	0.00	0.05
D1	0.45	0.55
D2	0.45	0.55
E1	0.20	0.30
E2	0.20	0.30
F	0.65	

## LAND LAYOUT

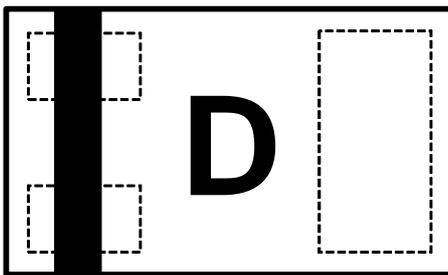


Dimensions		
Index	Millimeter	Inches
A	0.600	0.024
B	0.350	0.014
C	0.350	0.014
D	0.300	0.012
E	0.225	0.009
F	0.225	0.009
G	0.150	0.006

### Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

## MARKING CODE



Top View

Part Number	Marking Code
AZ5313-02F (Green part)	D

Note. Green means Pb-free, RoHS, and Halogen free compliant.

## Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ5313-02F.R7GR	Green	T/R	7 inch	12,000/reel	4 reel = 48,000/box	6 box = 288,000/carton



## Revision History

Revision	Modification Description
Revision 2014/02/20	Preliminary Release.
Revision 2015/11/17	Formal Release.