May 2007

DM74ALS161B, DM74ALS162B, DM74ALS163B Synchronous Four-Bit Counter

Features

- Switching specifications at 50pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts
- Synchronously programmable
- Internal look ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- ESD inputs

General Description

These synchronous presettable counters feature an internal carry look ahead for application in high speed counting designs. The DM74ALS162B is a four-bit decade counter, while the DM74ALS161B and DM74ALS163B are four-bit binary counters. The DM74ALS161B clears asynchronously, while the DM74ALS162B and DM74ALS163B clear synchronously. The carry output is decoded to prevent spikes during normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable, that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with set up data after the next clock pulse regardless of the levels of enable input. LOW-to-HIGH transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs.

The DM74ALS161B clear function is asynchronous. A low level at the clear input sets all four of the flip-flop outputs LOW regardless of the levels of clock, load or enable inputs. These two counters are provided with a clear on power-up feature. The DM74ALS162B and DM74ALS163B clear function is synchronous; and a low level at the clear input sets all four of the flip-flop outputs LOW after the next clock pulse, regardless of the levels of enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs. LOW-to-HIGH transitions at the clear input of the DM74ALS162B and DM74ALS163B are also permissible regardless of the levels of logic on the clock, enable or load inputs.

The carry look ahead circuitry provides for cascading counters for n bit synchronous application without additional gating. Instrumental in accomplishing this function are two count enable inputs (P and T) and a ripple carry output. Both count enable inputs must be HIGH to count. The T input is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high level output pulse with a duration approximately equal to the high level portion of QA output. This high level overflow ripple carry pulse can be used to enable successive cascaded stages. HIGH-to-LOW level transitions at the enable P or T inputs of the DM74ALS161B through DM74ALS163B may occur regardless of the logic level on the clock.

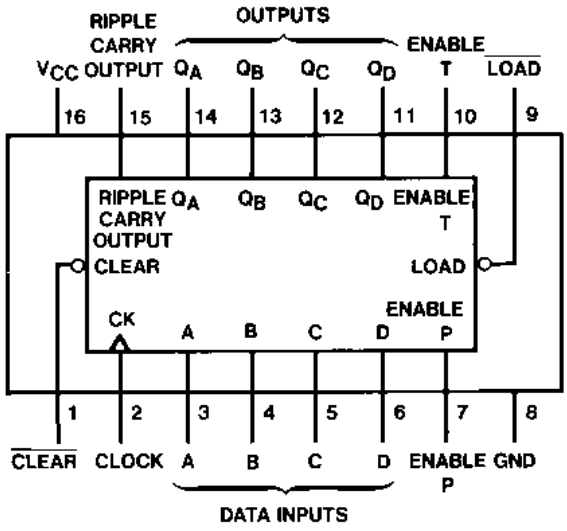
The DM74ALS161B through DM74ALS163B feature a fully independent clock circuit. changes made to control inputs (enable P or T, or load) that will modify the operating mode will have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

Ordering Information

Order Number	Package Number	Package Description
DM74ALS161BM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
DM74ALS162BM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
DM74ALS162BN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
DM74ALS163BM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
DM74ALS163BN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering number.

Connection Diagram



Mode Select Table

$\overline{\text{Clear}}$	$\overline{\text{Load}}$	Enable T	Enable P	Action on the Rising Clock Edge (⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

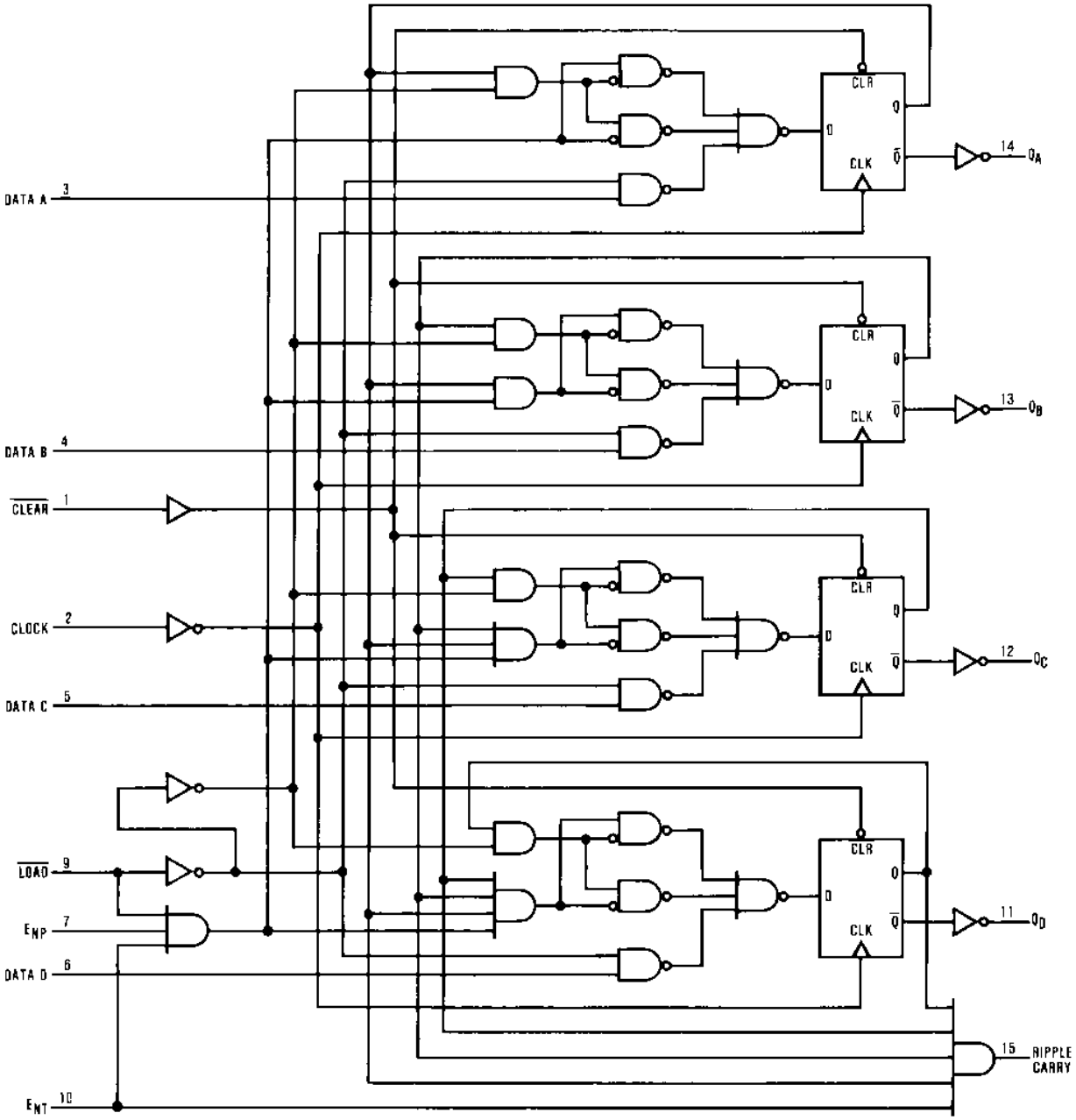
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

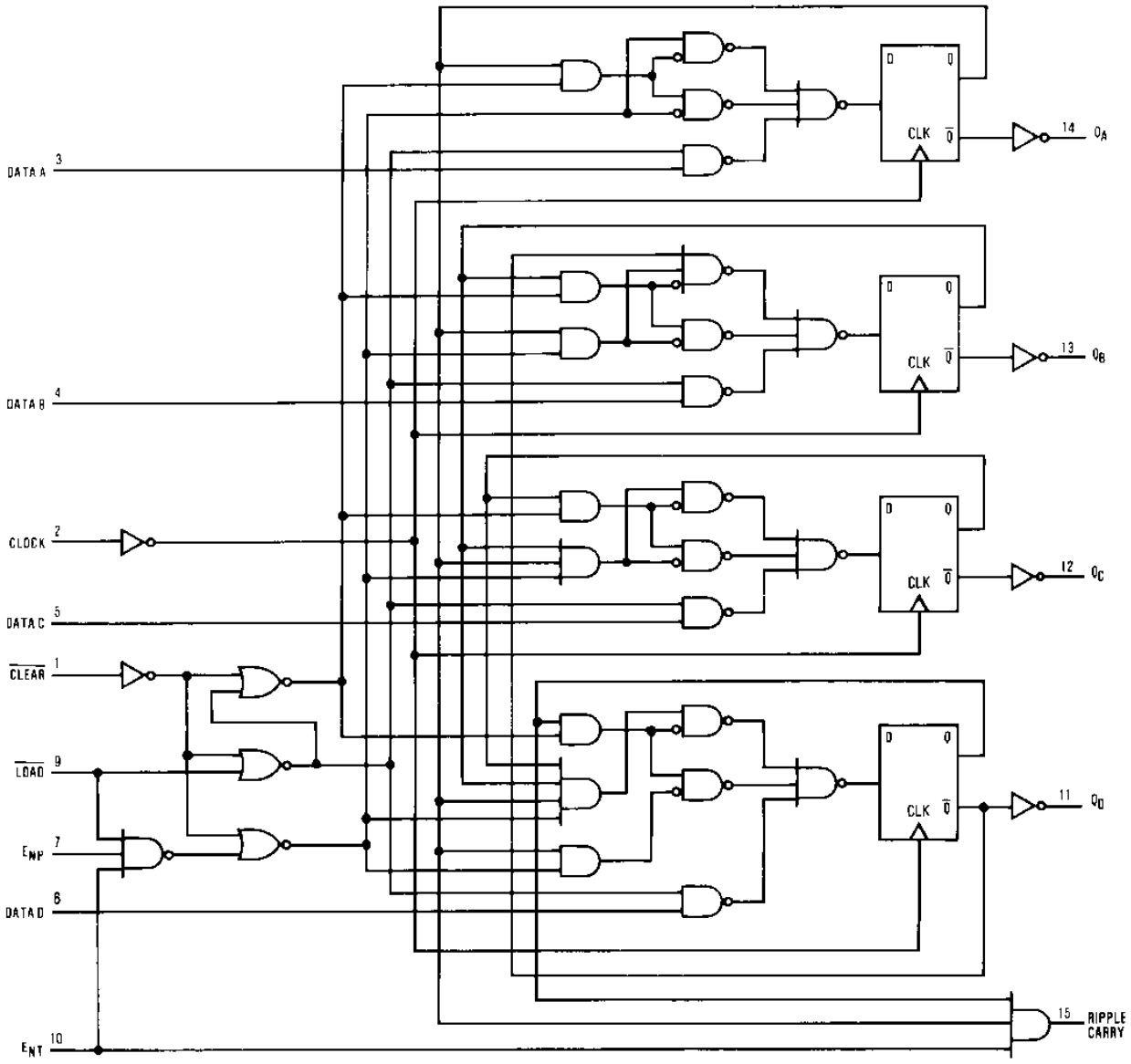
Logic Diagrams

DM74ALS161B



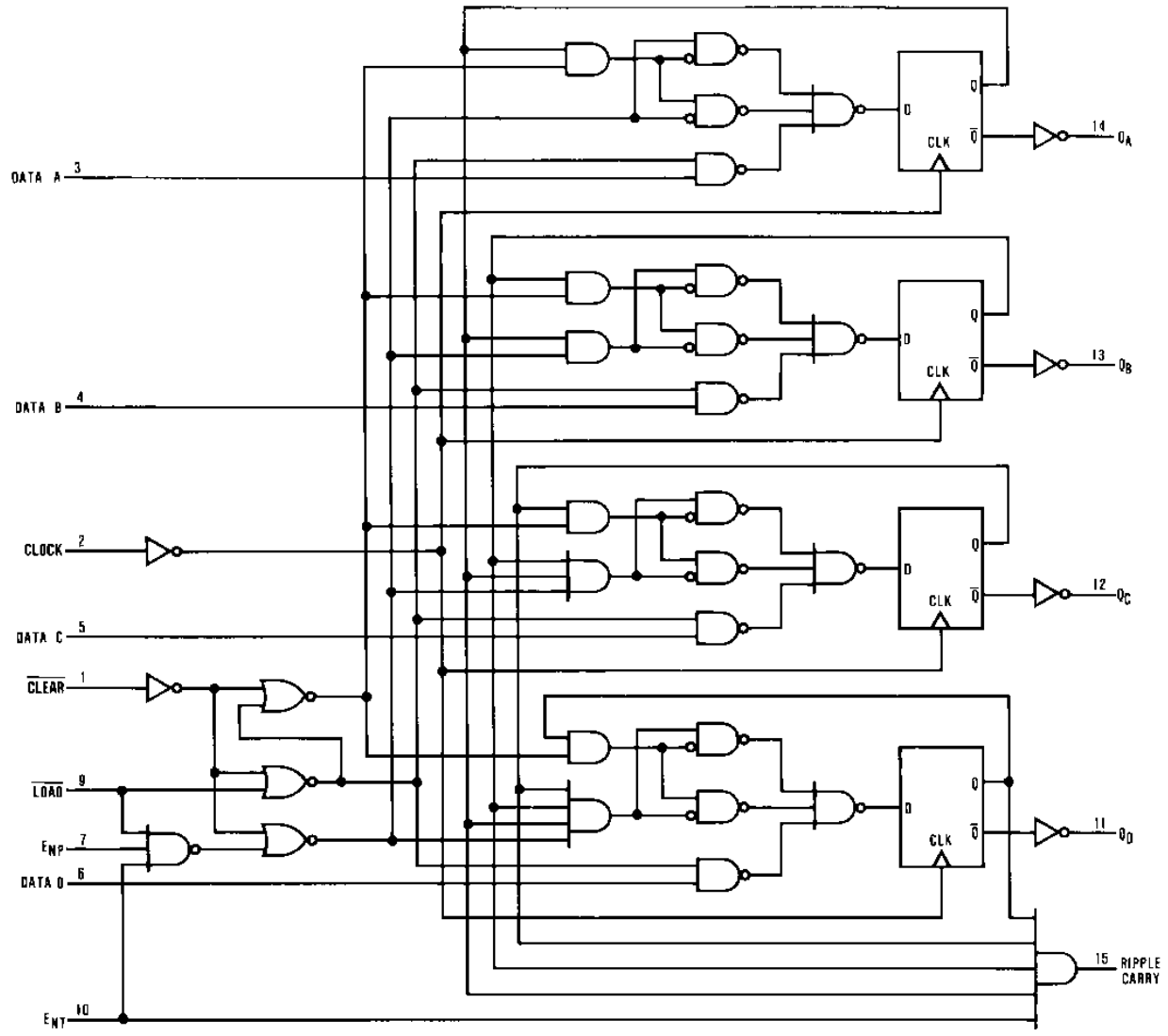
Logic Diagrams (Continued)

DM74ALS162B



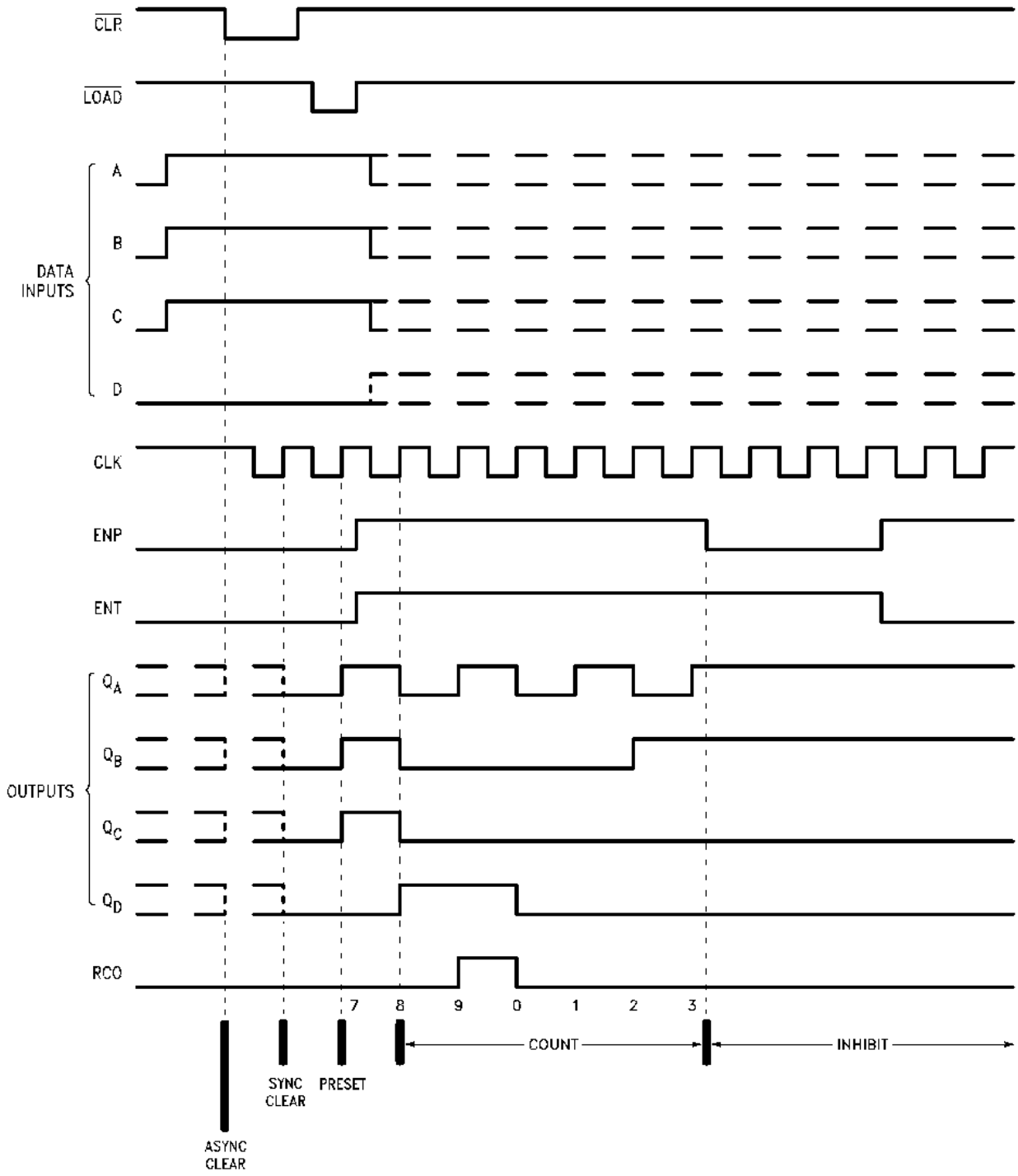
Logic Diagrams (Continued)

DM74ALS163B



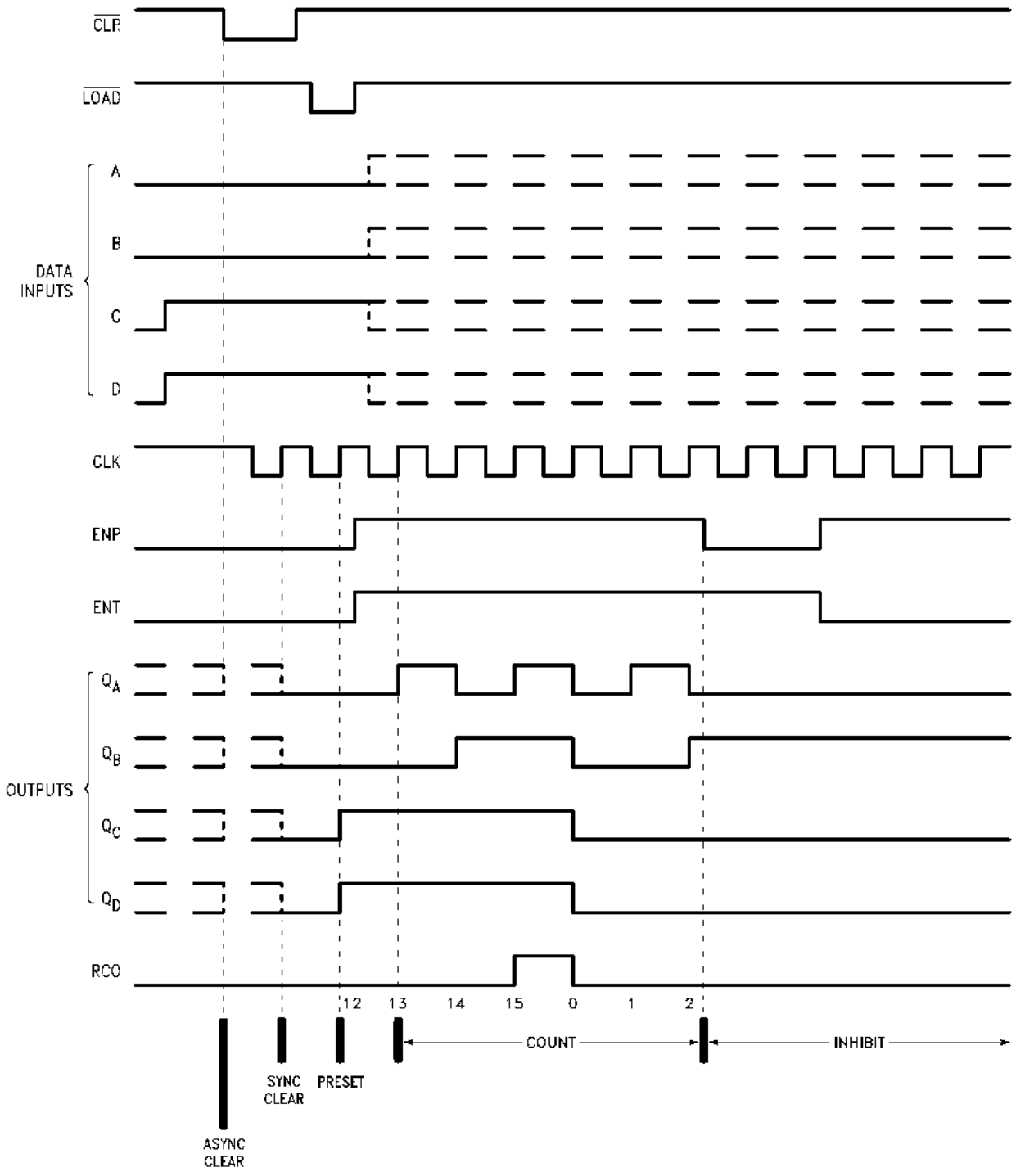
Timing Diagrams

DM74ALS162B



Timing Diagrams (Continued)

DM74ALS161B, DM74ALS163B



Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	7V
V_I	Input Voltage	7V
T_A	Operating Free Air Temperature Range	0°C to +70°C
T_{STG}	Storage Temperature Range	–65°C to +150°C
θ_{JA}	Typical Thermal Resistance	
	N Package	78.1°C/W
	M Package	106.8°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter			Min.	Nom.	Max.	Units
V_{CC}	Supply Voltage			4.5	5	5.5	V
V_{IH}	HIGH Level Input Voltage			2			V
V_{IL}	LOW Level Input Voltage					0.8	V
I_{OH}	HIGH Level Output Current					–0.4	mA
I_{OL}	LOW Level Output Current					8	mA
f_{CLK}	Clock Frequency			0		40	MHz
t_{SETUP}	Setup Time	Data; A, B, C, D		$15\uparrow^{(1)}$			ns
		En P, En T		$15\uparrow^{(1)}$			
		Load		$15\uparrow^{(1)}$			
		$\overline{\text{Clear}}$ (Only for DM74ALS162B and DM74ALS163B)	LOW	$15\uparrow^{(1)}$			
			HIGH	$12\uparrow^{(1)}$			
	Setup 1 (Only for 161B)	$\overline{\text{Clear}}$ Inactive		10	4		
t_{HOLD}	Hold Time	Data; A, B, C, D		$0\uparrow^{(1)}$	–3		ns
		En P, En T		$0\uparrow^{(1)}$	–3		
		Load		$0\uparrow^{(1)}$	–4		
		$\overline{\text{Clear}}$ (Only for DM74ALS162B and DM74ALS163B		$0\uparrow^{(1)}$	–7		
	Hold 0 (Only for 161B)	Clear		0	–4		
t_W	Width of Clock or $\overline{\text{Clear}}$ Pulse	CLK HIGH or LOW		12.5			ns
		DM74ALS161B $\overline{\text{CLR}}$ LOW		15			
	Width of $\overline{\text{Load}}$ Pulse			15			
T_A	Operating Free Air Temperature			0		70	°C

Note:

1. The symbol (↑) indicates that the rising edge of the clock is used as a reference.

Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = –18mA				–1.5	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = –0.4mA, V_{CC} = 4.5V to 5.5V		V_{CC} – 2			V
V_{OL}	LOW Level Output Voltage	V_{CC} = 4.5V	I_{OL} = 4mA		0.25	0.4	V
			I_{OL} = 8mA		0.35	0.5	
I_I	Input Current at Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	µA
I_{IL}	LOW Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				–0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			12	21	mA

Switching Characteristics DM74ALS161B

Over recommended operating free air temperature range.

Symbol	Parameter	Conditions	From	To	Min.	Max.	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50pF			40		MHz
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output		Clock	Ripple Carry	5	20	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output		Clock	Ripple Carry	5	20	ns
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output		Clock	Any Q	4	15	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output		Clock	Any Q	6	20	ns
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output		En T	Ripple Carry	3	13	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output		En T	Ripple Carry	3	13	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output		Clear	Any Q	8	24	ns
			Clear	Ripple Carry	11	23	

Switching Characteristics DM74ALS162B, DM74ALS163B

Over recommended operating free air temperature range.

Symbol	Parameter	Conditions	From	To	Min.	Max.	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50pF, T_A = Min. to Max.			40		MHz
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output		Clock	Ripple Carry	5	20	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output		Clock	Ripple Carry	5	20	ns
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output		Clock	Any Q	4	15	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output		Clock	Any Q	6	20	ns
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output		En T	Ripple Carry	3	13	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output		En T	Ripple Carry	3	13	ns

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

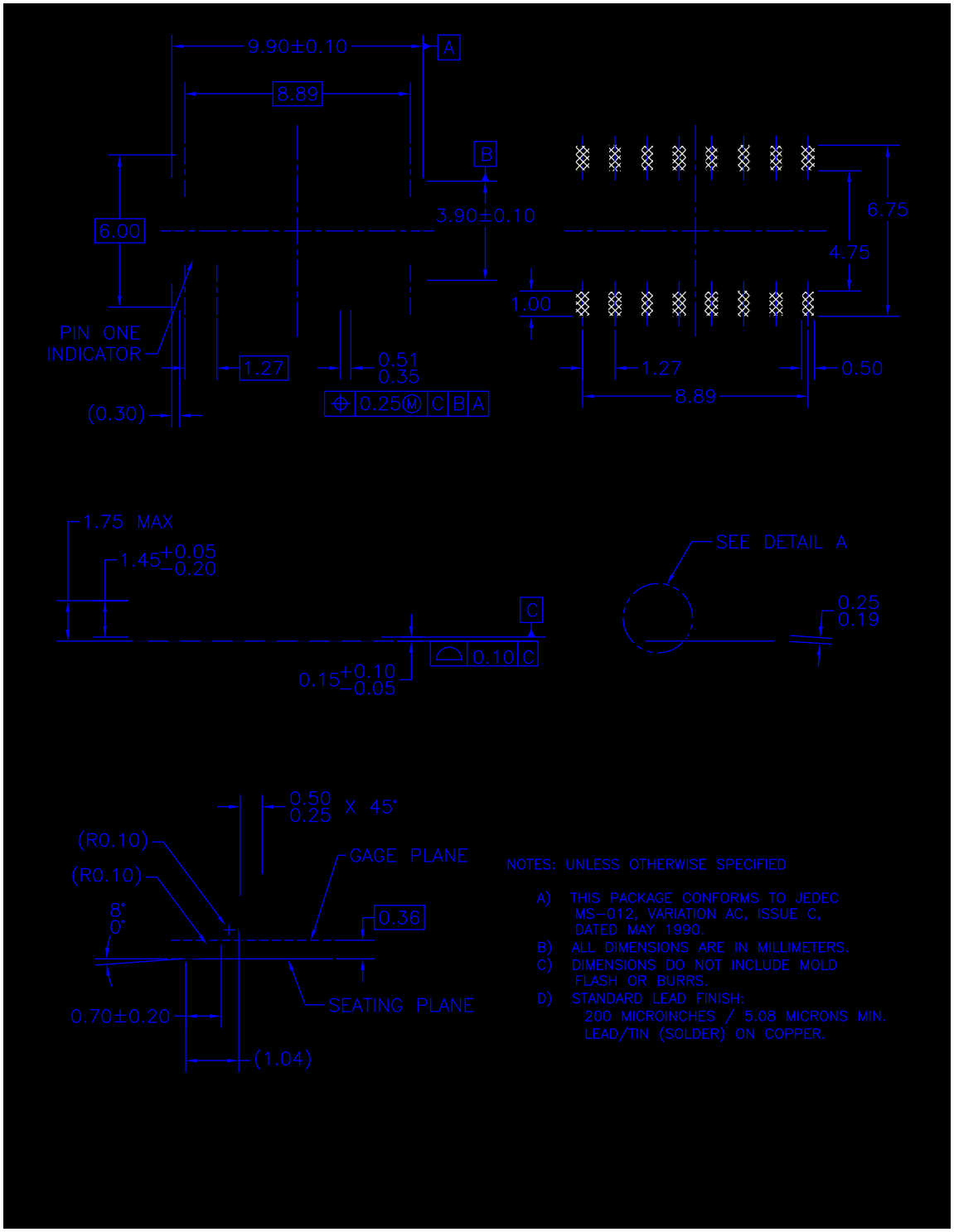


Figure 1. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.

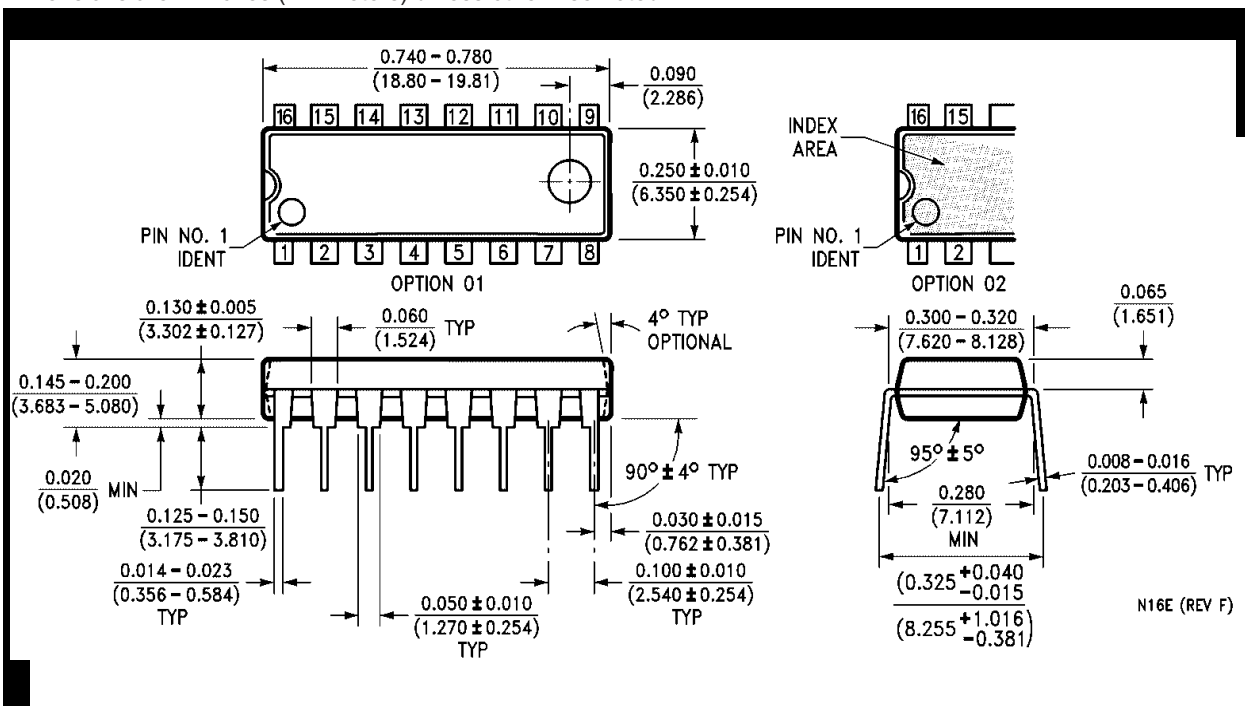


Figure 2. 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E