BGS12PN10

SPDT high linearity, high power RF Switch

Data Sheet

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Power Management & Multimarket

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Revision History

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Previous Version: 1.1

Page	Subjects (major changes since last revision)
1	title updated
5	key features updated

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Last Trademarks Update 2012-12-13

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BGS12PN10 SPDT high linearity, high power RF Switch

1 Features

- High max RF power: 40 dBm CW @ 900 MHz, room temperature
- Two ultra-low loss ports:
  0.17 dB @ f=0.9 GHz, P_{IN}=38 dBm
  0.22 dB @ f=1.9 GHz, P_{IN}=38 dBm
  0.26 dB @ f=2.7 GHz, P_{IN}=33 dBm
  0.37 dB @ f=3.6 GHz, P_{IN}=33 dBm
  0.68 dB @ f=5.8 GHz, P_{IN}=33 dBm
- No DC decoupling components required, if no external DC is applied on RF ports
- High ESD robustness
- Low harmonic generation
- High linearity: 75dBm IIP3
- No power supply blocking required
- Supply voltage range: 1.8 to 3.6 V
- No insertion loss change within supply voltage range
- No linearity change within supply voltage range
- Suitable for EDGE / C2K / LTE / WCDMA / SV-LTE Applications
- Mobile cellular Rx/Tx applications, suitable for LTE/3G
- Applicable for main path and entire RF Front-end without any power restrictions in mobile communication
  - DL/UL CA and MIMO
  - Micro/Pico Cells/Cellular base stations
  - Test equipment
  - Suitable for SV-LTE
- 0.5 to 6.0 GHz coverage
- Small form factor 1.1 mm x 1.5 mm
- 400 μm pad pitch
- RoHS and WEEE compliant package

RoHS

2 Product Description

The BGS12PN10 is a Single Pole Dual Throw (SPDT) high power RF switch optimized for mobile phone applications up to 6.0 GHz. This single supply chip integrates on-chip CMOS logic driven by a simple, CMOS or TTL compatible control input signal. Unlike GaAs technology, the 0.1 dB compression point exceeds the switch maximum input power level, resulting in linear performance at all signal levels and external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally.

Table 1: Ordering Information

Type	Package	Marking	Chip
BGS12PN10	TSNP10-1	2P	M4821A

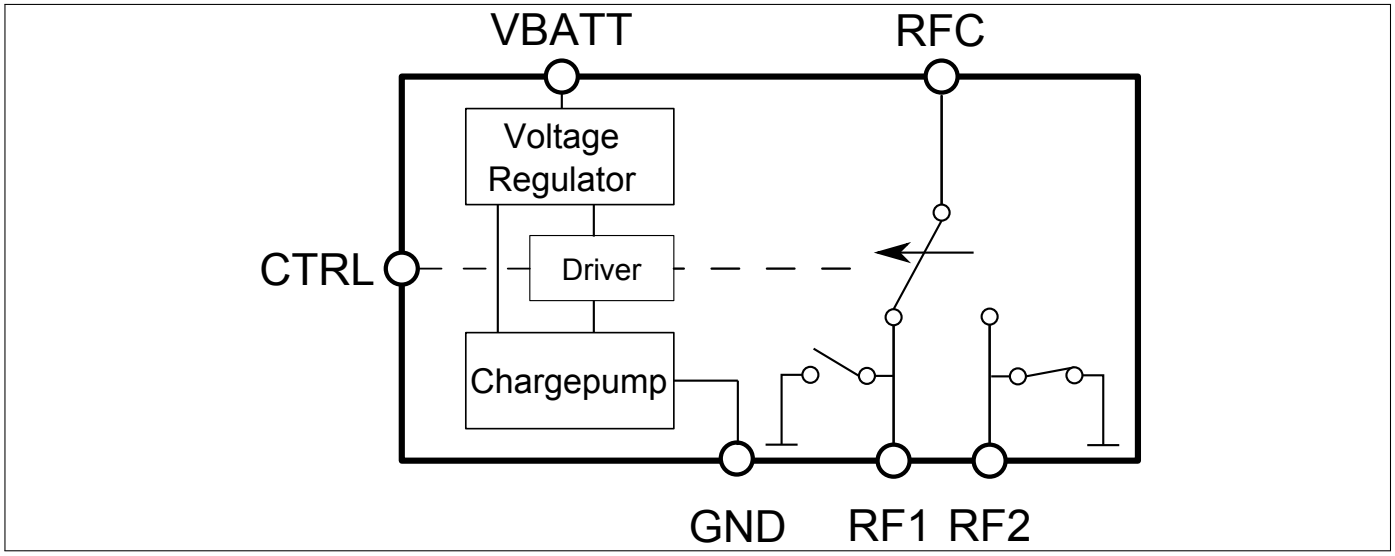

Figure 1: BGS12PN10 block diagram

3 Maximum Ratings

Table 2: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range	f	0.5	–	6.0	GHz	1)
Supply voltage	V_{DD}	-0.5	–	3.6	V	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
RF input power	P_{RF_TRx}	–	–	40	dBm	CW, 900 MHz
ESD capability Human Body Model	$V_{ESD_{HBM}}$	-1.5	–	+1.5	*kV*	2)
ESD capability RFC port3)	$V_{ESD_{RFC}}$	-10	–	+10	*kV*	On application board with 27nH shunt inductor
Junction temperature	T_j	–	–	125	°C	–

1) Switch has no highpass response. There is also a high ohmic DC to the RF path. The DC voltage at RF ports V_{RFDC} has to be 0V.
2) Field-Induced Charged-Device Model JESD22-C101. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
3) Human Body Model ANSI/ESDA/JEDEC JS-001-2012 (R = 1.5 kΩ, C = 100 pF).
4) IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

Table 3: Maximum Ratings, Table II at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum DC-voltage on RF-Ports and RF-Ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF-Ports
Control Voltage Levels	V_{CTRL}	-0.7	–	3.3	V	–

4 Operation Ranges

Table 4: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	1.8	2.85	3.6	V	–
Supply current[1)]	I_{DD}	–	75	120	μA	–
Control voltage low	$V_{Ctrl,low}$	0		0.45	V	–
Control voltage high	$V_{Ctrl,high}$	1.2	1.8	2.85	V	$V_{Ctrl,high} \ll V_{DD}$
Control current low	$I_{Ctrl,low}$	-1	0	1	μA	–
Control current high	$I_{Ctrl,high}$	-1	0	1	μA	$V_{Ctrl,high} \ll V_{DD}$
Ambient temperature	T_A	-30	25	85	°C	–
RF switching time [2)]	t_{sw}	1	3.5	5	μs	–
Startup time [2)]	t_{st}		10	30	μs	–

[1)] T_A = -30 °C – +85 °C, V_{BATT} = 1.8 – 3.6 V

[2)], Represents actual alpha status. To be updated.

5 Logic Table

Table 5: Logic Table

CTRL	Mode
0	RF1 connected to RFC
1	RF2 connected to RFC

6 RF Characteristics

Table 6: RF Specifications

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion Loss						
698 - 960 MHz	*IL*	–	0.16	0.25	dB	V_{DD} = 1.8 – 3.6 *V*, T_A = -30 ... +85 °C, Z_0 = 50 Ω, P_{IN} up to 38 dBm
1710 - 1980 MHz		–	0.22	0.29	dB	
1981 - 2170 MHz		–	0.23	0.3	dB	
2171 - 2690 MHz		–	0.26	0.35	dB	
3400 - 3800 MHz		–	0.37	0.49	dB	
5150 - 5850 MHz		–	0.68	0.99	dB	
Return Loss						
All Ports @ 698 - 960 MHz	*RL*	25	30	–	dB	
All Ports @ 1710 - 1980 MHz		19	22	–	dB	
All Ports @ 1981 - 2170 MHz		18	21	–	dB	
All Ports @ 2171 - 2690 MHz		17	19	–	dB	
All Ports @ 3400 - 3800 MHz		13	17	–	dB	
All Ports @ 5150 - 5850 MHz		10	12	–	dB	
Isolation RFC						
698 - 915 MHz	*ISO*	36	39	–	dB	
1710 - 1980 MHz		30	32	–	dB	
1981 - 2170 MHz		28	29	–	dB	
2171 - 2690 MHz		26	27	–	dB	
3400 - 3800 MHz		22	23	–	dB	
5150 - 5850 MHz		16	17	–	dB	
Isolation RF1,2 - RF2,1						
698 - 915 MHz	*ISO*	49	54	–	dB	
1710 - 1980 MHz		39	40	–	dB	
1981 - 2170 MHz		37	38	–	dB	
2170 - 2690 MHz		33	34	–	dB	
3400 - 3800 MHz		28	29	–	dB	
5150 - 5850 MHz		19	20	–	dB	

7 RF large signal parameter

Table 7: RF large signal specifications

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Harmonic Generation up to 12.75 GHz(1,2,3)						
Second Order Harmonics	P_{H2}	–	-105	–	dBc	25 dBm, 50Ω, CW mode
Third Order Harmonics	P_{H3}	–	-115	–	dBc	25 dBm, 50Ω, CW mode
All RF Ports	P_{Hx}	–	-105	–	dBc	25 dBm, 50Ω, CW mode
Intermodulation Distortion IMD2 (1,2,3)						
IIP2, low	IIP2,l	–	115	–	dBm	IIP2 conditions table 8
IIP2, high	IIP2,h	–	125	–	dBm	
Intermodulation Distortion IMD3 (1,2,3)						
IIP3	IIP3	–	75	–	dBm	IIP3 conditions table 9
SV LTE Intermodulation (1,2,3)						
IIP3,SVLTE	IIP3,SV	–	75	–	dBm	SV-LTE conditions table 10

[1)]Terminating Port Impedance: $Z_0 = 50\ \Omega$ [2)]Supply Voltage: $V_{DD} = 1.8 - 3.6\ V$ [3)]On application board without any matching components

Table 8: IIP2 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1 Low	2140	1950	20	190	-15
Band 1 High	2140	1950	20	4090	-15
Band 5 Low	881.5	836.5	20	45	-15
Band 5 High	881.5	836.5	20	1718	-15

Table 9: IIP3 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1	2140	1950	20	1760	-15
Band 5	881.5	836.5	20	791.5	-15

Table 10: SV-LTE conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 5	872	827	23	872	14
Band 13	747	786	23	747	14
Band 20	878	833	23	2544	14

8 Package Outline and Pin Configuration

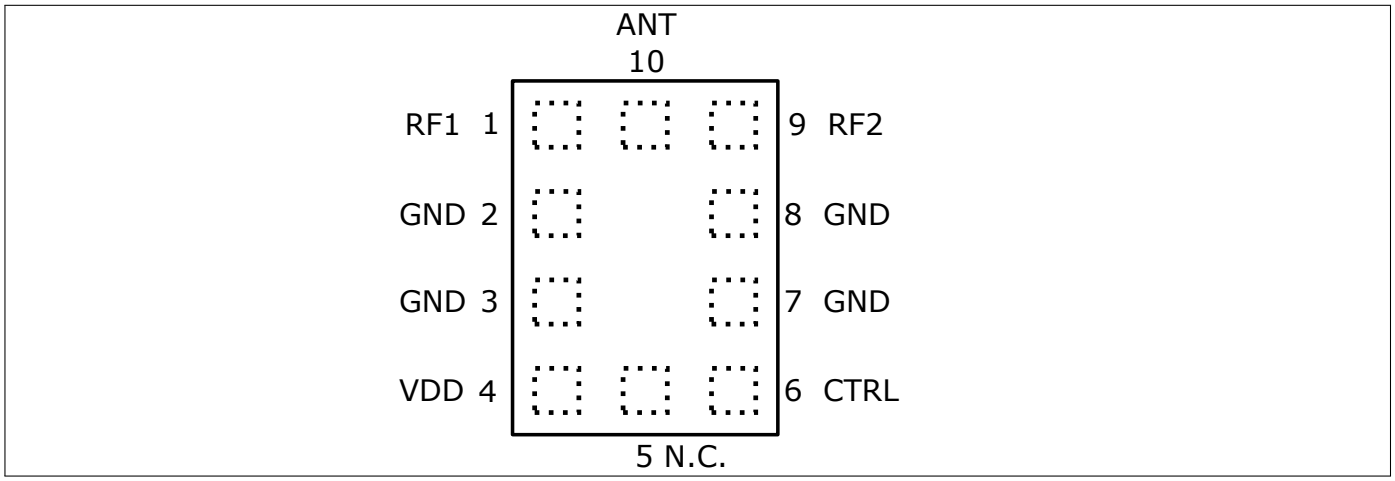

Figure 2: Pinout (top view)

Table 11: Pin Description

Pin No.	Name	Pin Type	Buffer Type	Function
1	RF1	I/O.		RF1
2	GND	GND		Ground
3	GND	GND		Ground
4	VDD	PWR		Supply voltage
5	N.C.	N.C.		Not connected
6	CTRL	I		Control Pin
7	GND	GND		Ground
8	GND	GND		Ground
9	RF2.	I/O		RF2
10	ANT	I/O		Common RF / Antenna

Table 12: Mechanical Data

Parameter	Symbol	Value	Unit
X-Dimension	*X*	1.1 $\pm$ 0.05	*mm*
Y-Dimension	*Y*	1.5 $\pm$ 0.05	*mm*
Size	*Size*	1.65	mm^2
Height	*H*	0.375	*mm*

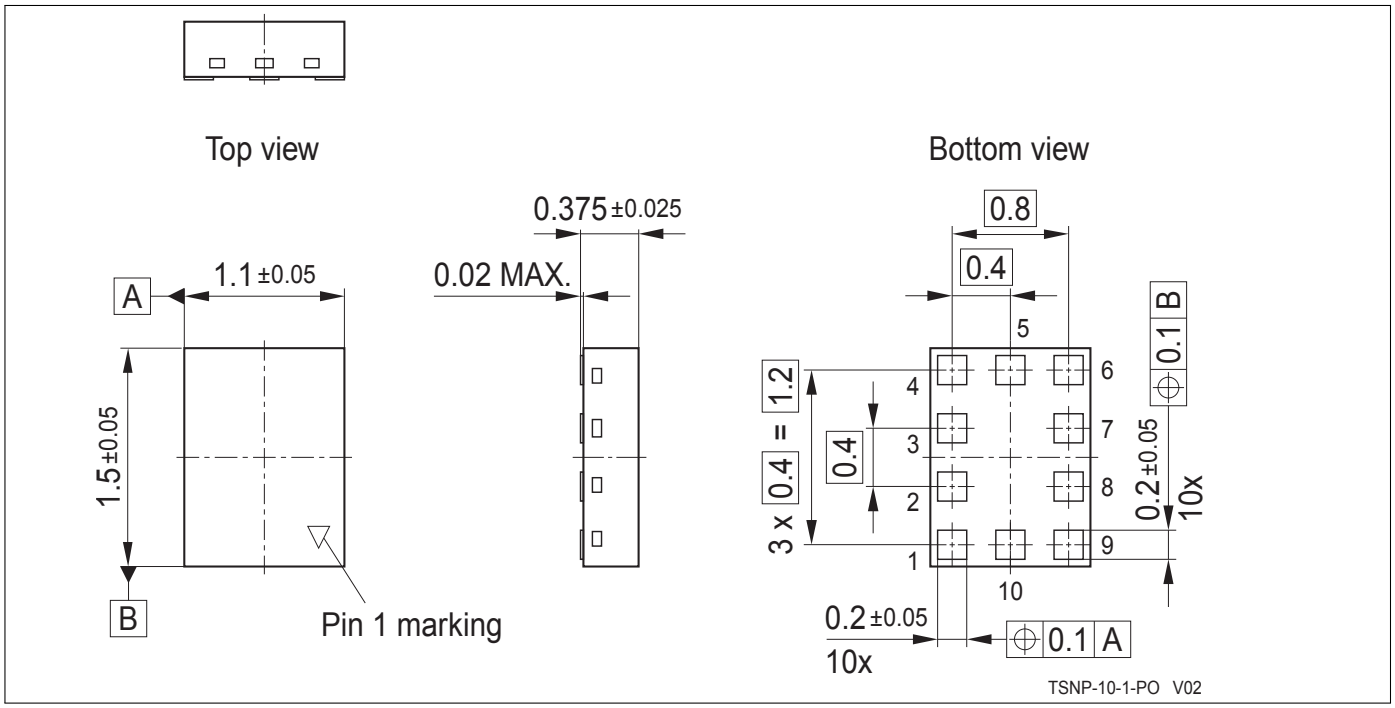

Figure 3: Package Dimensions Drawing

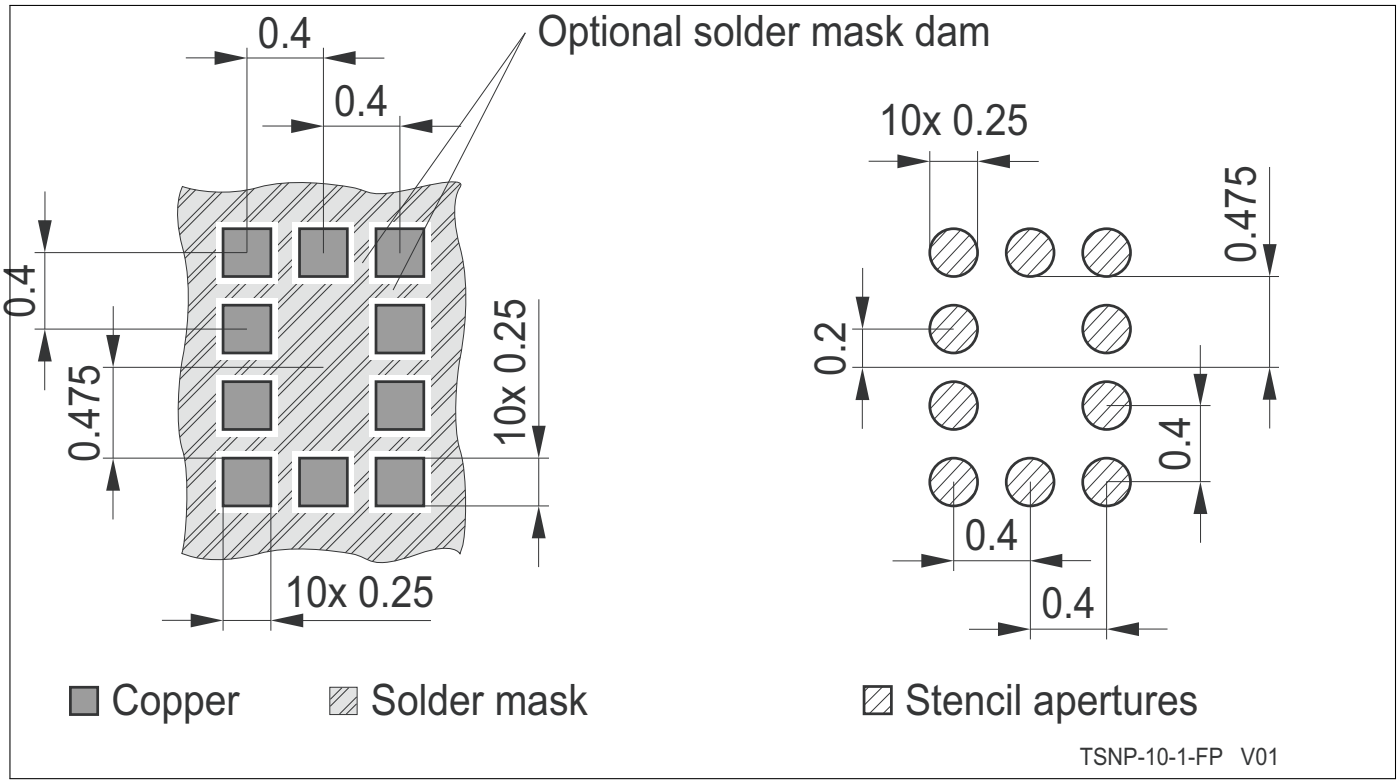

Figure 4: Land pattern and stencil mask

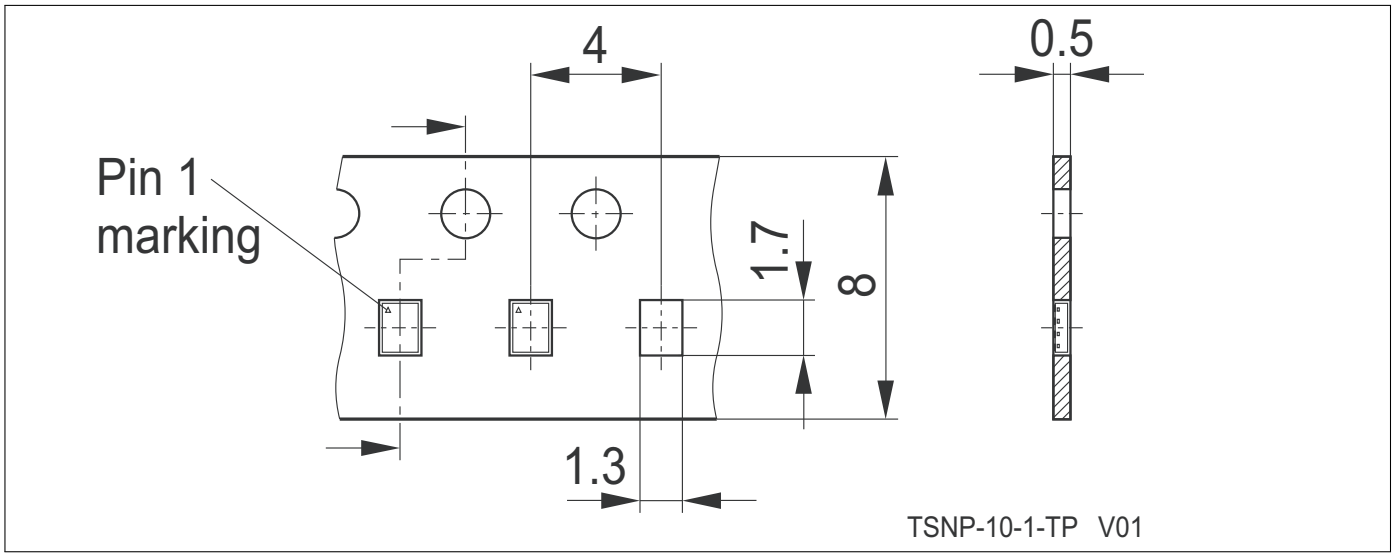

Figure 5: Tape drawing

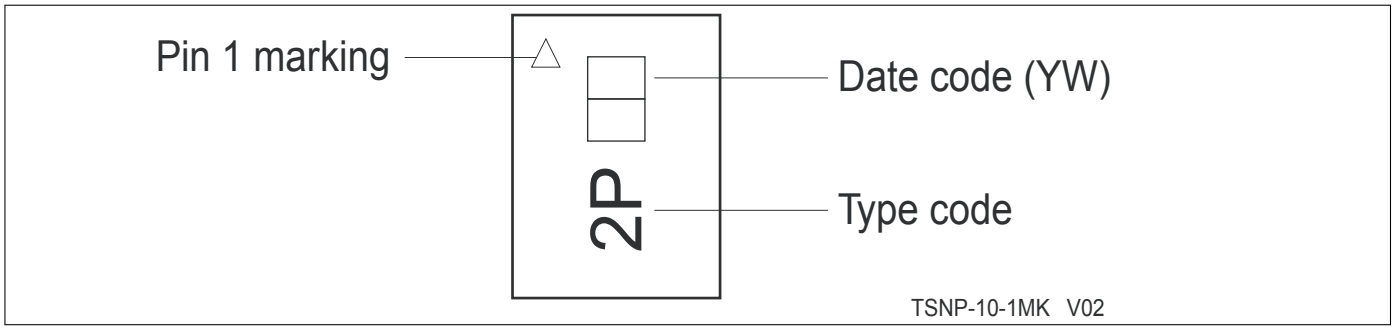

Figure 6: Package marking: Date code digits Y and W are found in Table 13/14

Table 13: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"	Year	"Y"
2000	0	2010	0	2020	0
2001	1	2011	1	2021	1
2002	2	2012	2	2022	2
2003	3	2013	3	2023	3
2004	4	2014	4	2024	4
2005	5	2015	5	2025	5
2006	6	2016	6	2026	6
2007	7	2017	7	2027	7
2008	8	2018	8	2028	8
2009	9	2019	9	2029	9

Table 14: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s		
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

9 RF measurements

All measurement data performed

- represents typical performance
- on evaluation PCB
- without external RF matching components
- load impedance: Z_0 = 50 Ω
- deembedded PCB insertion loss
- supply voltage: 2.85 V (no change for 1.8-3.6 V due to internal voltage regulator)
- room temperature: 25°C

unless otherwise noted.

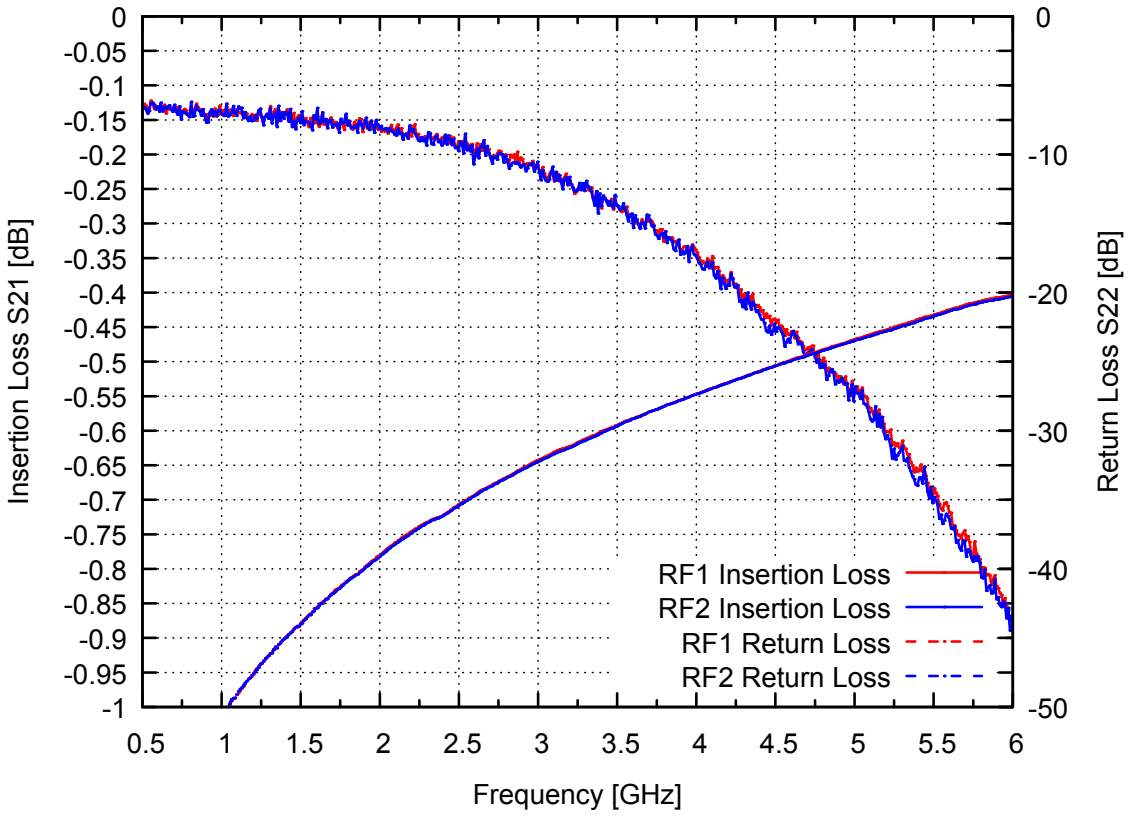

Figure 7: Insertion loss and return loss at room temperature

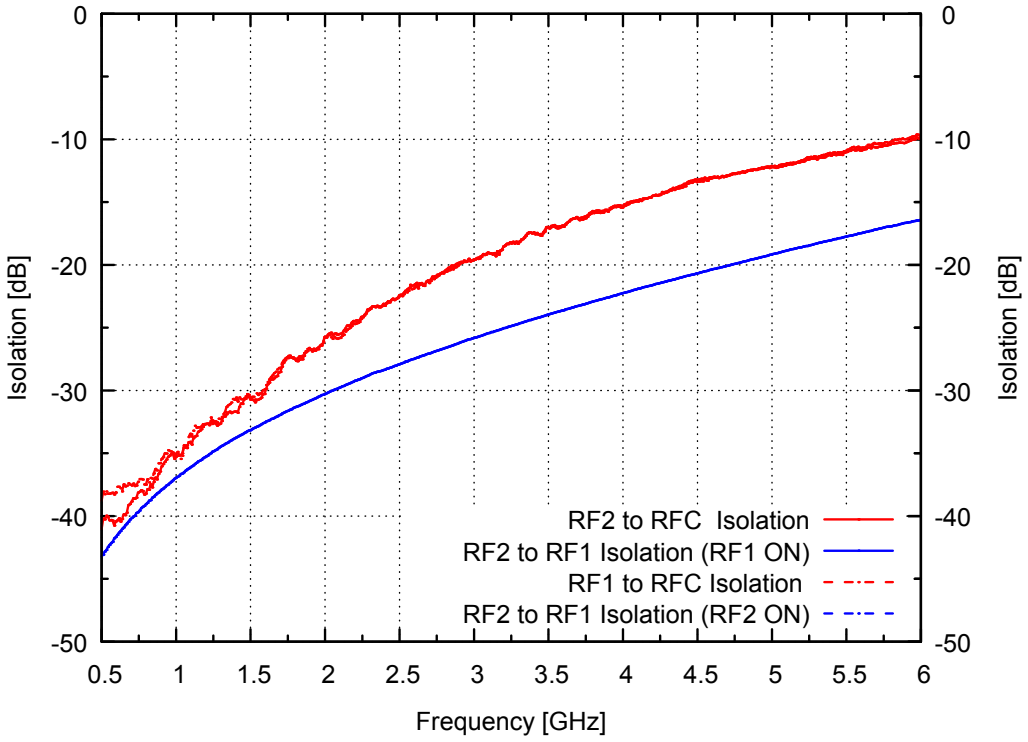

Figure 8: Port to port isolation at room temperature

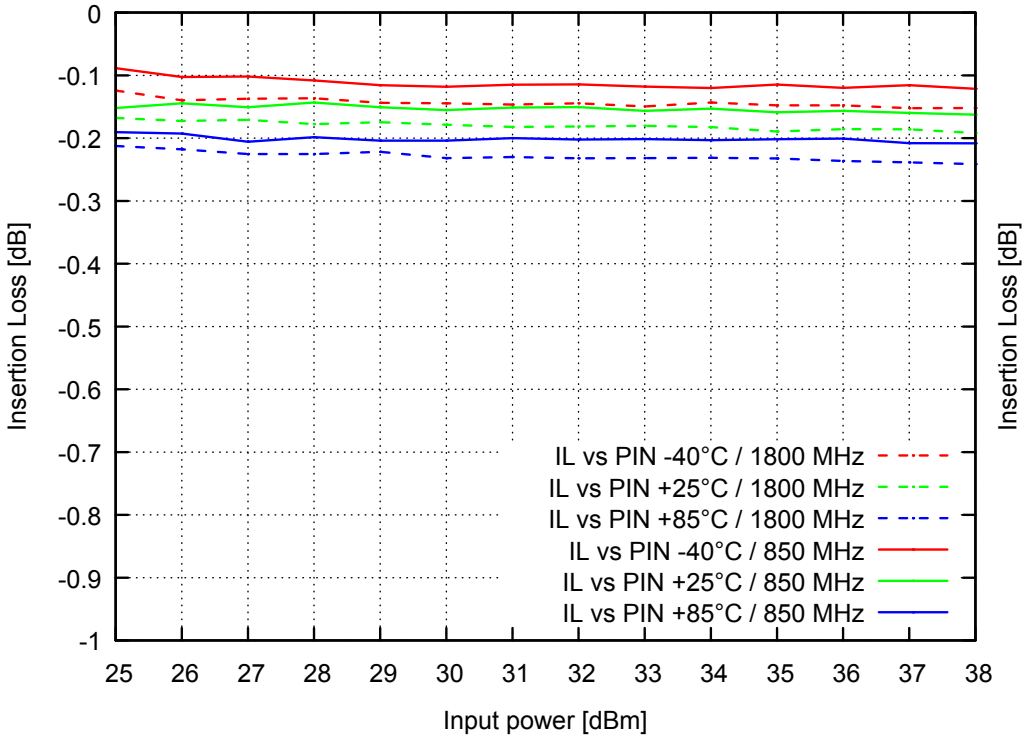

Figure 9: Insertion loss vs input power and temperature

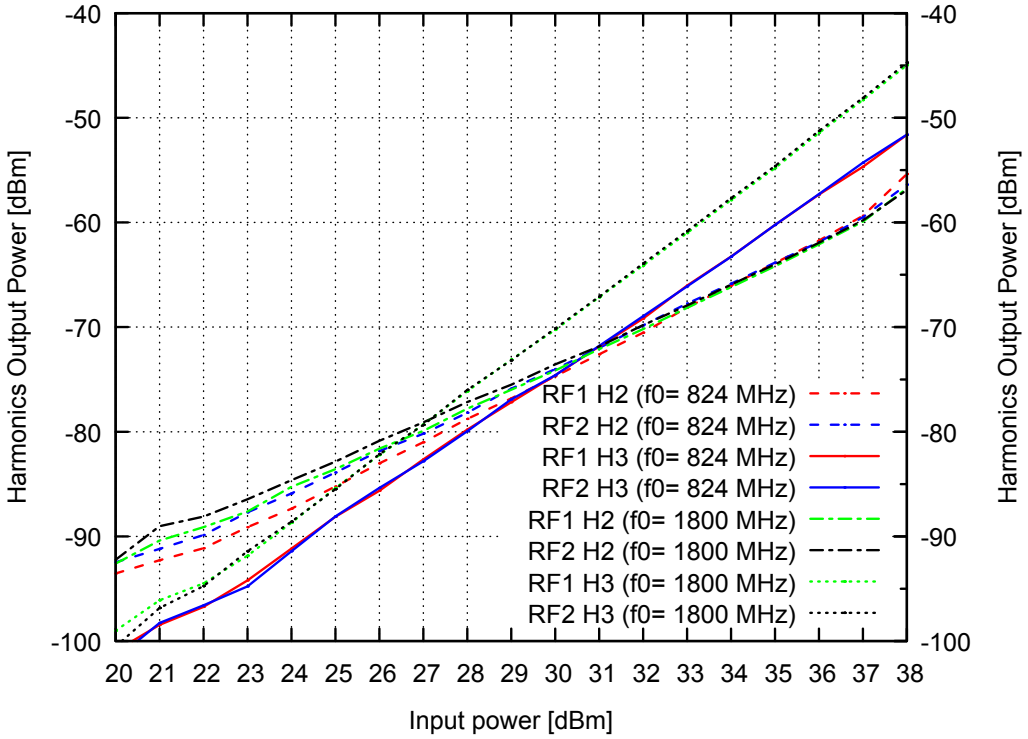

Figure 10: H2/H3 harmonic output power vs frequency at room temperature

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