Evaluation Board for ADP2118

EVAL-ADP2118

GENERAL DESCRIPTION

The evaluation (demo) board provides an easy way to evaluate the ADP2118 buck regulator. This data sheet describes how to quickly set up the board to begin collecting performance data. Full details on the ADP2118 are available in the ADP2118 data sheet, which is available from Analog Devices, Inc., and should be consulted in conjunction with this data sheet when using the evaluation board.

This data sheet also describes the design process for the ADP2118 buck regulator, including external component selection, and how to obtain the best dynamic performance.

Thermal performance is described, which provides a current derating reference for the user when the ADP2118 is operating at different ambient temperatures.

PRODUCT DESCRIPTION

The ADP2118 is a low quiescent current, synchronous, step-down, dc-to-dc regulator in a compact 4 mm × 4 mm LFCSP_WQ package. It uses a current mode, constant frequency pulse width modulation (PWM) control scheme for excellent stability and transient response. Under light loads, the ADP2118 can be configured to operate in pulse frequency modulation (PFM) mode that reduces switching frequency to save power.

The ADP2118 runs from input voltages of 2.3 V to 5.5 V. The ADP2118 requires minimal external parts and provides a high efficiency solution with its integrated power switch, synchronous rectifier, and internal compensation. Other key features include undervoltage lockout (UVLO), integrated soft start to limit inrush current at startup, overvoltage protection (OVP), overcurrent protection (OCP), and thermal shutdown (TSD).

ADP2118 EVALUATION BOARD

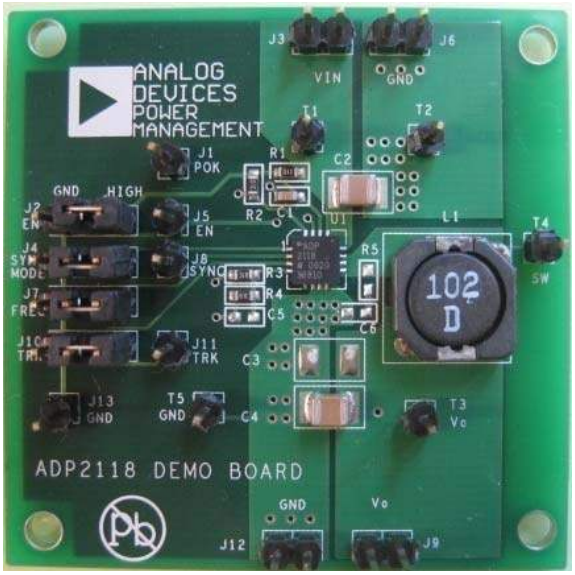

Figure 1.

Rev. 0

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REVISION HISTORY

1/10—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWERING UP THE EVALUATION BOARD

The ADP2118 evaluation board is fully assembled and tested. Before applying power to the evaluation board, follow the setup procedures in this section.

Jumper Settings

Refer to Table 1 for selecting the jumper positions.

Make sure the enable input, EN, is high.

Table 1. Jumper Settings

Jumper	States	Function
J2 (EN)	High	Enable V_{OUT}
	Low	Disable V_{OUT}
J4 (SYNC/MODE)	High	Force PWM
	Low	Enable PFM
	External clock	Synchronize to the external clock
J7 (FREQ)	High	f_S = 1.2 MHz 180° out of phase with external clock if synchronize function used
	Low	f_S = 600 kHz In phase with external clock if synchronize function used
J10 (TRK)	High	Tracking function not used
	External voltage	Tracking with the external voltage

Input Power Source Connection

Before connecting the power source to the ADP2118 evaluation board, make sure that it is turned off. If the input power source includes a current meter, use that meter to monitor the input current.

Connect the positive terminal of the power source to the VIN terminal (J3) on the evaluation board, and the negative terminal of the power source to the GND terminal (J6) of the board. If the power source does not include a current meter, connect a current meter in series with the input source voltage.

Connect the positive terminal of the power source to the ammeter positive terminal (+), the negative terminal of the power source to the GND terminal (J6) on the evaluation board, and the negative terminal (−) of the ammeter to the VIN terminal (J3) on the board.

Output Load Connection

Make sure that the board is turned off before connecting the load. If the load includes an ammeter, or if the current is not measured, connect the load directly to the evaluation board with the positive (+) load connection to the VOUT terminal (J9) and negative (−) load connection to the GND terminal (J12).

If an ammeter is used, connect it in series with the load; connect the positive (+) ammeter terminal to the evaluation board VOUT terminal (J9), the negative (−) ammeter terminal to the positive (+) load terminal, and the negative (−) load terminal to the evaluation board GND terminal (J12).

Input and Output Voltmeter Connections

Measure the input and output voltages with voltmeters. Make sure that the voltmeters are connected to the appropriate test points on the board. If the voltmeters are not connected to the right test point, the measured voltages may be incorrect due to the voltage drop across the leads and/or connections between the boards, the power source, and/or load.

Connect the positive (+) terminal of the input voltage measuring voltmeter to Test Point T1, and the negative (−) terminal to Test Point T2.

Connect the positive (+) terminal of the output voltage measuring voltmeter's to the Test Point T3 and the negative (−) terminal to Test Point T5.

Power On the Evaluation Board

When the power source and load are connected to the ADP2118 evaluation board, it can be powered up for operation. If the input power source is above 2.3 V, the output voltage goes up to 1.2 V.

MEASURING EVAULATION BOARD PERFORMANCE

Measuring the Switching Waveform

To observe the switching waveform with an oscilloscope, place the oscilloscope probe tip at Test Point T4 with the probe ground at GND. Set the scope to dc, 2 V/division, and 1 µs/division time base. The switching waveform should alternate between 0 V and approximately the input voltage.

Measuring Load Regulation

Load regulation should be tested by increasing the load at the output and measuring the output voltage between the T3 and T5 test points.

Measuring Line Regulation

Vary the input voltage and measure the output voltage at a fixed output current. Input voltage can be measured between T1 and T2. The output voltage is measured between T3 and T5.

Measuring Efficiency

The efficiency, η, is measured by comparing the input power with the output power.

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$$

Measuring Inductor Current

The inductor current can be measured by removing one end of the inductor from the pad on the board and using a wire connected between the pad and the inductor. Then, a current probe can be used to measure the inductor current.

Measuring Output Voltage Ripple

To observe the output voltage ripple, place an oscilloscope probe across the output capacitor (C4) with the probe ground lead at the negative (−) capacitor terminal and the probe tip at the positive (+) capacitor terminal. Set the oscilloscope to ac, 10 mV/division, 2 µs/division time base, and 20 MHz bandwidth.

A standard oscilloscope probe has a long wire ground clip. For high frequency measurements, this ground clip picks up high frequency noise and injects it into the measured output ripple. Figure 2 shows an easy way to measure the output ripple properly. It requires removing the oscilloscope probe sheath and wrapping a nonshielded wire around the oscilloscope probe. By keeping the ground lengths on the oscilloscope probe as short as possible, true ripple can be measured.

Output Voltage Change

The ADP2118 evaluation board output is preset to 1.2 V; however, the output voltage can be adjusted to other voltages using the following equation:

$$V_{OUT} = 0.6\ \text{V} \times \left(\frac{R4 + R3}{R3} \right)$$

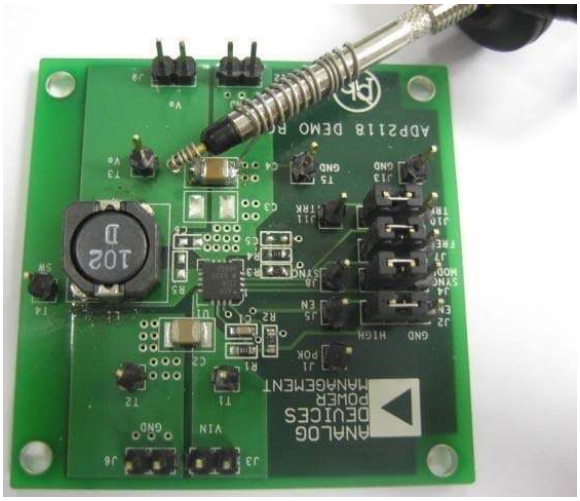

Figure 2. Output Ripple Measurement

ADP2118 DESIGN PROCESS

EXTERNAL COMPONENT SELECTION

This section describes how to select the external components for the ADP2118 application.

Input Capacitor Selection

The input decoupling capacitor is used to attenuate high frequency noise on the input. This capacitor should be a ceramic capacitor in the range of 22 µF to 100 µF. This capacitor must be placed close to the PVIN pin. The loop, composed of C_{IN}, PFET, and NFET, must be kept as small as possible.

VIN RC Filter

An RC filter is needed at the VIN pin to attenuate switching noise. Generally, a 10 Ω resistor and 0.1 µF, 6.3 V capacitor is recommended.

Output Filter Selection

The ADP2118 has internal compensation, so there are some limitations in choosing the output filter. Table 2 to Table 7 show the stability with different output filter components.

For the inductor selection, check the rms current and saturation current rating.

The selected inductor rms current must be higher than the value calculated by Equation 1, and the saturation current must be higher than the value calculated by Equation 2.

$$I_{L\_RMS} = \sqrt{I_O{}^2 + \frac{1}{12}\left(\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_S \times L}\right)^2} \quad (1)$$

$$I_{L\_Peak} = I_O + \frac{1}{2} \times \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_S \times L} \quad (2)$$

where:
I_O is the output current.
V_{OUT} is the output voltage.
V_{IN} is the input voltage.
f_S is the switching frequency.
L is the selected inductance.

For the ADP2118 design, X5R or X7R ceramic capacitors are recommended. When selecting the capacitor, the dc voltage rating and the rms current rating must be considered.

Make sure that the capacitor dc voltage rating is greater than the output voltage.

The capacitor's rms current rating must be larger than the value calculated by Equation 3.

$$I_{C_{OUT}\_RMS} = \sqrt{\frac{1}{12}} \times \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_S \times L} \quad (3)$$

Output Voltage Setting

If using the adjustable output version of the ADP2118, the output voltage is set by the resistor divider (see Figure 3). Equation 4 is used to set the output voltage:

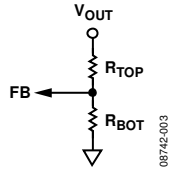

Figure 3. Resistor Divider for Adjustable Version

$$V_{OUT} = 0.6\ V \times \frac{R_{TOP} + R_{BOT}}{R_{BOT}} \quad (4)$$

To limit the output voltage accuracy degradation due to FB bias current (0.1 µA maximum) to less than 0.5%, ensure that R_{BOT} is less than 30 kΩ. It is recommended to use a 10 kΩ, 1% accuracy resistor for R_{BOT}.

If using the fixed output version, connect V_{OUT} directly to the FB pin.

Cross Frequency and Phase Margin with Different Output Filter and f_S = 1.2 MHz

Table 2. Cross Frequency and Phase Margin—V_{OUT} = 1.0 V

C_{OUT} (µF)	L (µH)	V_{IN}	3.3 V	5 V
47	1	f_C (kHz)	150	150
		PM (Degrees)	42	39
	1.5	f_C (kHz)	126	133
		PM (Degrees)	33	31
	2.2	f_C (kHz)	118	124
		PM (Degrees)	28	27
	3.3	f_C (kHz)	103	112
		PM (Degrees)	30	25
100	1	f_C (kHz)	104	105
		PM (Degrees)	59	55
	1.5	f_C (kHz)	92	91
		PM (Degrees)	47	50
	2.2	f_C (kHz)	78	63
		PM (Degrees)	41	42
	3.3	f_C (kHz)	72	77
		PM (Degrees)	34	35

Table 3. Cross Frequency and Phase Margin—V_{OUT} = 1.5 V

C_{OUT} (µF)	L (µH)	V_{IN}	3.3 V	5 V
47	1	f_C (kHz)	121	124
		PM (Degrees)	57	57
	1.5	f_C (kHz)	93	114
		PM (Degrees)	53	49
	2.2	f_C (kHz)	84	98
		PM (Degrees)	42	51
	3.3	f_C (kHz)	74	83
		PM (Degrees)	34	40
100	1	f_C (kHz)	72	75
		PM (Degrees)	65	66
	1.5	f_C (kHz)	67	71
		PM (Degrees)	54	57
	2.2	f_C (kHz)	61	67
		PM (Degrees)	46	50
	3.3	f_C (kHz)	57	63
		PM (Degrees)	40	44

Table 4. Cross Frequency and Phase Margin—V_{OUT} = 2.5 V

C_{OUT} (µF)	L (µH)	V_{IN}	3.3 V	5 V
47	1	f_C (kHz)	67	73
		PM (Degrees)	70	71
	1.5	f_C (kHz)	59	68
		PM (Degrees)	55	59
	2.2	f_C (kHz)	53	64
		PM (Degrees)	46	51
	3.3	f_C (kHz)	48	59
		PM (Degrees)	39	44
100	1	f_C (kHz)	50	53
		PM (Degrees)	73	72
	1.5	f_C (kHz)	45	51
		PM (Degrees)	61	64
	2.2	f_C (kHz)	42	48
		PM (Degrees)	53	56
	3.3	f_C (kHz)	38	44
		PM (Degrees)	48	50

Table 5. Cross Frequency and Phase Margin—V_{OUT} = 1.2 V

C_{OUT} (µF)	L (µH)	V_{IN}	3.3 V	5 V
47	1	f_C (kHz	130	135
		PM (Degrees)	40	41
	1.5	f_C (kHz)	121	131
		PM (Degrees)	42	44
	2.2	f_C (kHz)	105	119
		PM (Degrees)	35	38
	3.3	f_C (kHz)	96	109
		PM (Degrees)	30	33
100	1	f_C (kHz)	83	81
		PM (Degrees)	67	61
	1.5	f_C (kHz)	76	83
		PM (Degrees)	51	53
	2.2	f_C (kHz)	73	78
		PM (Degrees)	45	46
	3.3	f_C (kHz)	66	75
		PM (Degrees)	39	41

Table 6. Cross Frequency and Phase Margin—V_{OUT} = 1.8 V

C_{OUT} (µF)	L (µH)	V_{IN}	3.3 V	5 V
47	1	f_C (kHz)	103	103
		PM (Degrees)	61	61
	1.5	f_C (kHz)	86	94
		PM (Degrees)	47	50
	2.2	f_C (kHz)	74	82
		PM (Degrees)	42	49
	3.3	f_C (kHz)	67	76
		PM (Degrees)	36	41
100	1	f_C (kHz)	63	65
		PM (Degrees)	68	68
	1.5	f_C (kHz)	61	66
		PM (Degrees)	54	57
	2.2	f_C (kHz)	57	63
		PM (Degrees)	46	51
	3.3	f_C (kHz)	51	58
		PM (Degrees)	39	45

Table 7. Cross Frequency and Phase Margin—V_{OUT} = 3.3 V

C_{OUT} (µF)	L (µH)	V_{IN}	3.3 V	5 V
47	1	f_C (kHz)	N/A	64
		PM (Degrees)		73
	1.5	f_C (kHz)		62
		PM (Degrees)		65
	2.2	f_C (kHz)		58
		PM (Degrees)		55
	3.3	f_C (kHz)		53
		PM (Degrees)		47
100	1	f_C (kHz)	N/A	45
		PM (Degrees)		74
	1.5	f_C (kHz)		42
		PM (Degrees)		70
	2.2	f_C (kHz)		40
		PM (Degrees)		62
	3.3	f_C (kHz)		38
		PM (Degrees)		55

PERFORMANCE IMPROVEMENT

The ADP2118 uses internal compensation for ease-of-use but limits optimization of the converter's transient performance. This section describes how to use a feedforward capacitor in the feedback resistor divider to optimize the transient response.

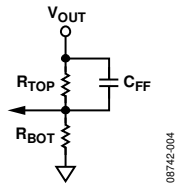

Figure 4. Feedforward Capacitor Added to Resistor Divider

Figure 4 shows the feedback resistor divider with the feedforward capacitor. Using a feedforward capacitor allows the regulator to be more responsive to high frequency disturbances on the output. This capacitor introduces a zero (Equation 5) and pole (Equation 6) in the system:

$$f_Z = \frac{1}{2 \times \pi \times R_{TOP} \times C_{FF}} \quad (5)$$

$$f_P = \frac{R_{TOP} + R_{BOT}}{2 \times \pi \times C_{FF} \times R_{TOP} \times R_{BOT}} \quad (6)$$

From Table 2 to Table 7, the cross frequency (f_C) without the feedforward capacitor is known. Using Equation 7, calculate the required feedforward capacitor. Based on this calculated value, a standard value can be selected to obtain the best transient performance.

$$f_C = \sqrt{f_Z \times f_P} \quad (7)$$

From Equation 5, Equation 6, and Equation 7, the C_{FF} value shown in Equation 8 can be obtained.

$$C_{FF} = \frac{1}{2 \times \pi \times f_C} \times \sqrt{\frac{(R_{TOP} + R_{BOT})}{R_{TOP}^2 \times R_{BOT}}} \quad (8)$$

The feedforward capacitor can be used to improve dynamic response with the following conditions: V_{IN} = 5 V, V_{OUT} = 3.3 V, f_S = 1.2 MHz, L = 1 µH, C_{OUT} = 100 µF, R_{TOP} = 10 kΩ, R_{BOT} = 2.21 kΩ.

Figure 5 and Figure 6 show the bode plot and load dynamic response without the C_{FF} capacitor.

From Table 7, f_C (cross frequency) = 45 kHz.

From Equation 8,

$$C_{FF} = \frac{1}{2 \times \pi \times 45\ \text{kHz}} \times \sqrt{\frac{(10\ \text{k}\Omega + 2.21\ \text{k}\Omega)}{(10\ \text{k}\Omega)^2 \times 2.21\ \text{k}\Omega}} = 831\ \text{pF}$$

Therefore, C_{FF} = 1000 pF.

Figure 7 and Figure 8 show the bode plot and load dynamic response with C_{FF} = 1000 pF.

The cross frequency with C_{FF} added is improved to 171 kHz with a phase margin of 67°.

Comparing Figure 6 and Figure 8, the load dynamic response is significantly improved with the addition of the C_{FF} capacitor.

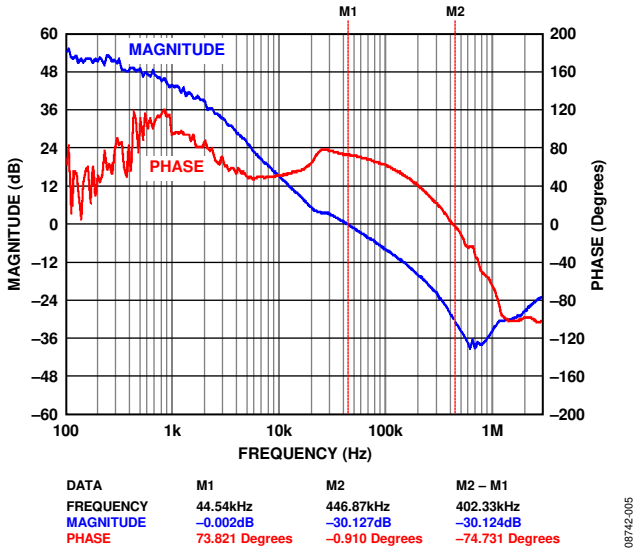

Figure 5. Bode Plot Without C_{FF}

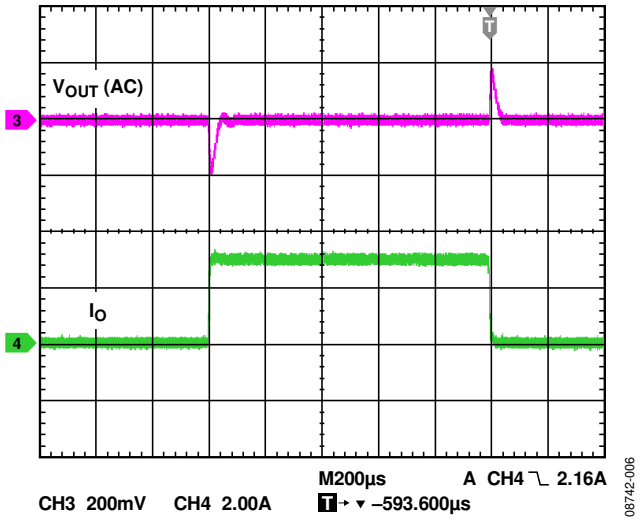

Figure 6. Load Dynamic Without C_{FF}

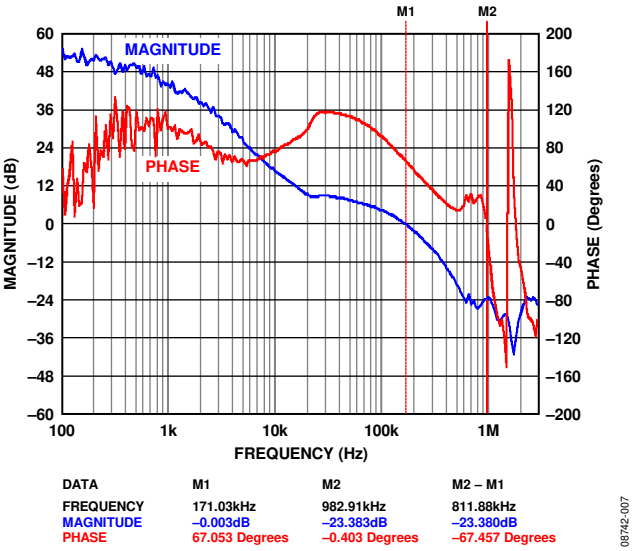

Figure 7. Bode Plot with C_{FF} = 1000 pF

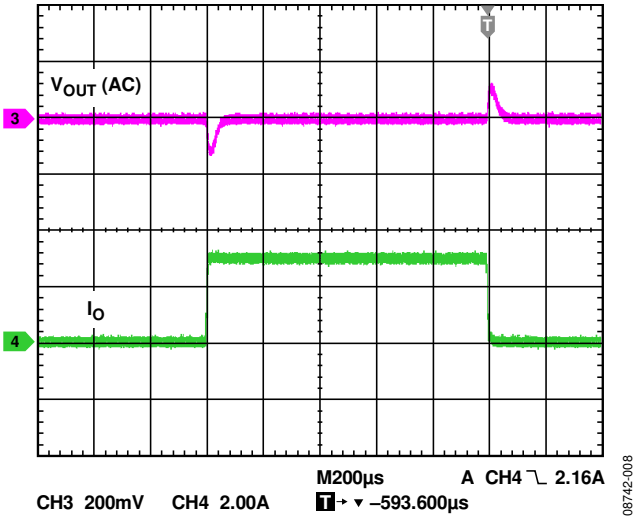

Figure 8. Load Dynamic with C_{FF} = 1000 pF

LAYOUT GUIDELINES

The input decoupling capacitor (C_{IN}) should be as close as possible to the PVIN and PGND pins. Make the loop composed of PVIN, PGND, and C_{IN} as small as possible.

The VIN filter needs to be placed as close as possible to the VIN pin.

A ground plane is recommended to minimize noise and maximize heat dissipation. If a ground plane layer is not used, the analog ground (GND) and the power ground (PGND) should be separated and tied together at the output capacitor terminal.

Flood all unused areas on all layers with copper to reduce the temperature rise of power components. The copper areas must be connected to a dc net, for example, PVIN, V_{OUT}, PGND, or GND.

Connect the FB pin directly to the feedback resistor divider or to the output if the fixed output version is used. The feedback node must be kept well away from noise sources like the switching node.

An RC snubber between SW and PGND can reduce spikes at the switching node under heavy load conditions.

THERMAL PERFORMANCE

Measured from the evaluation board with L = 1 µH, Part Number MSS1038-102NL, and C_{OUT} = 100 µF.

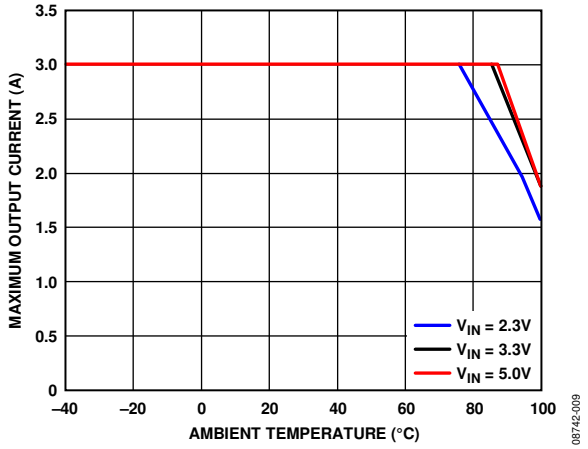

Figure 9. Thermal Derating Performance at 110°C Case Temperature, V_{OUT} = 1.0 V, f_S = 1.2 MHz

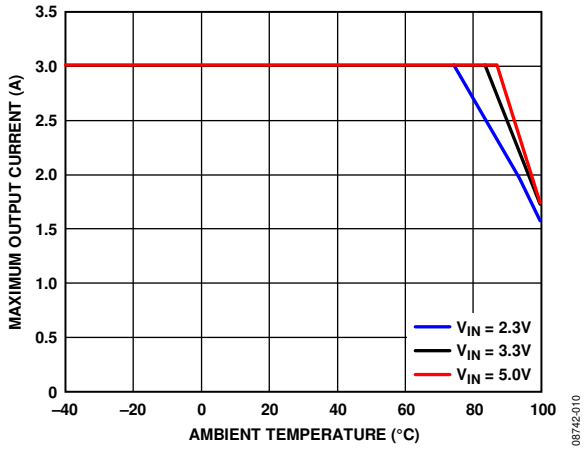

Figure 10. Thermal Derating Performance at 110°C Case Temperature, V_{OUT} = 1.5 V, f_S = 1.2 MHz

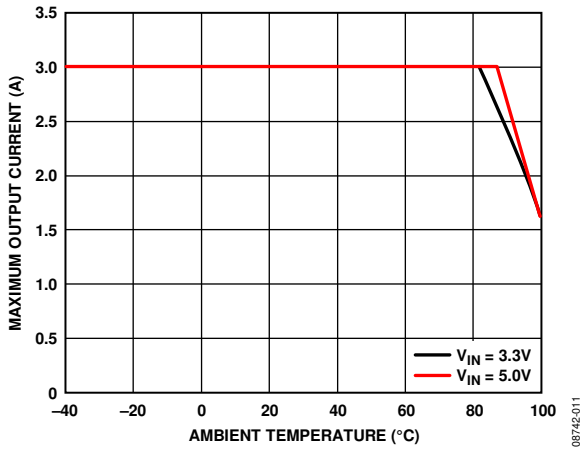

Figure 11. Thermal Derating Performance at 110°C Case Temperature, V_{OUT} = 2.5 V, f_S = 1.2 MHz

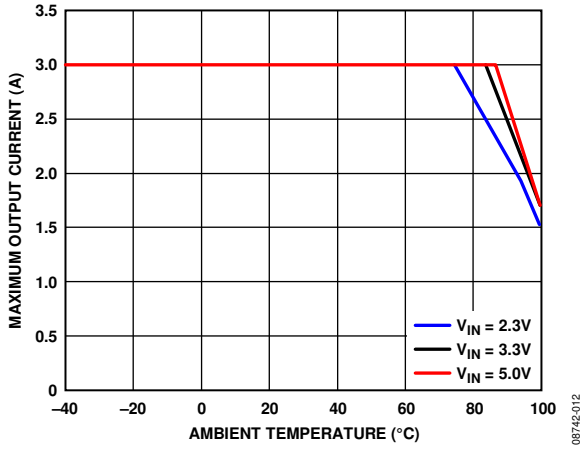

Figure 12. Thermal Derating Performance at 110°C Case Temperature, V_{OUT} = 1.2 V, f_S = 1.2 MHz

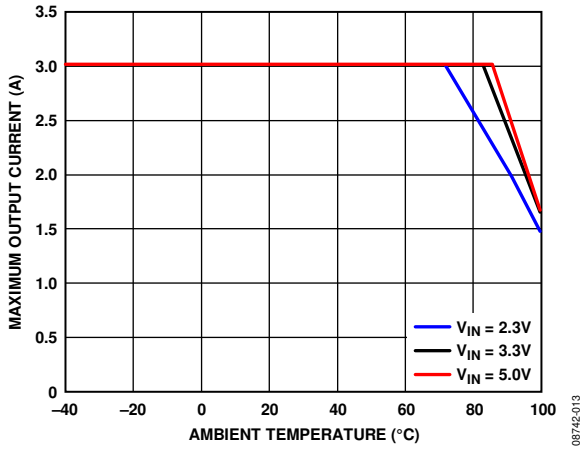

Figure 13. Thermal Derating Performance at 110°C Case Temperature, V_{OUT} = 1.8 V, f_S = 1.2 MHz

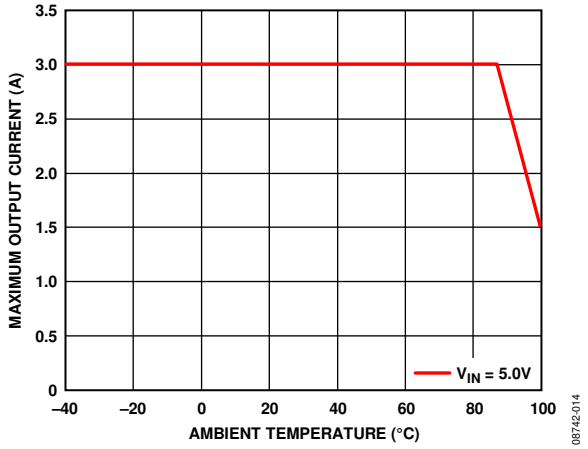

Figure 14. Thermal Derating Performance at 110°C Case Temperature, V_{OUT} = 3.3 V, f_S = 1.2 MHz

EVALUATION BOARD SCHEMATIC AND ARTWORK

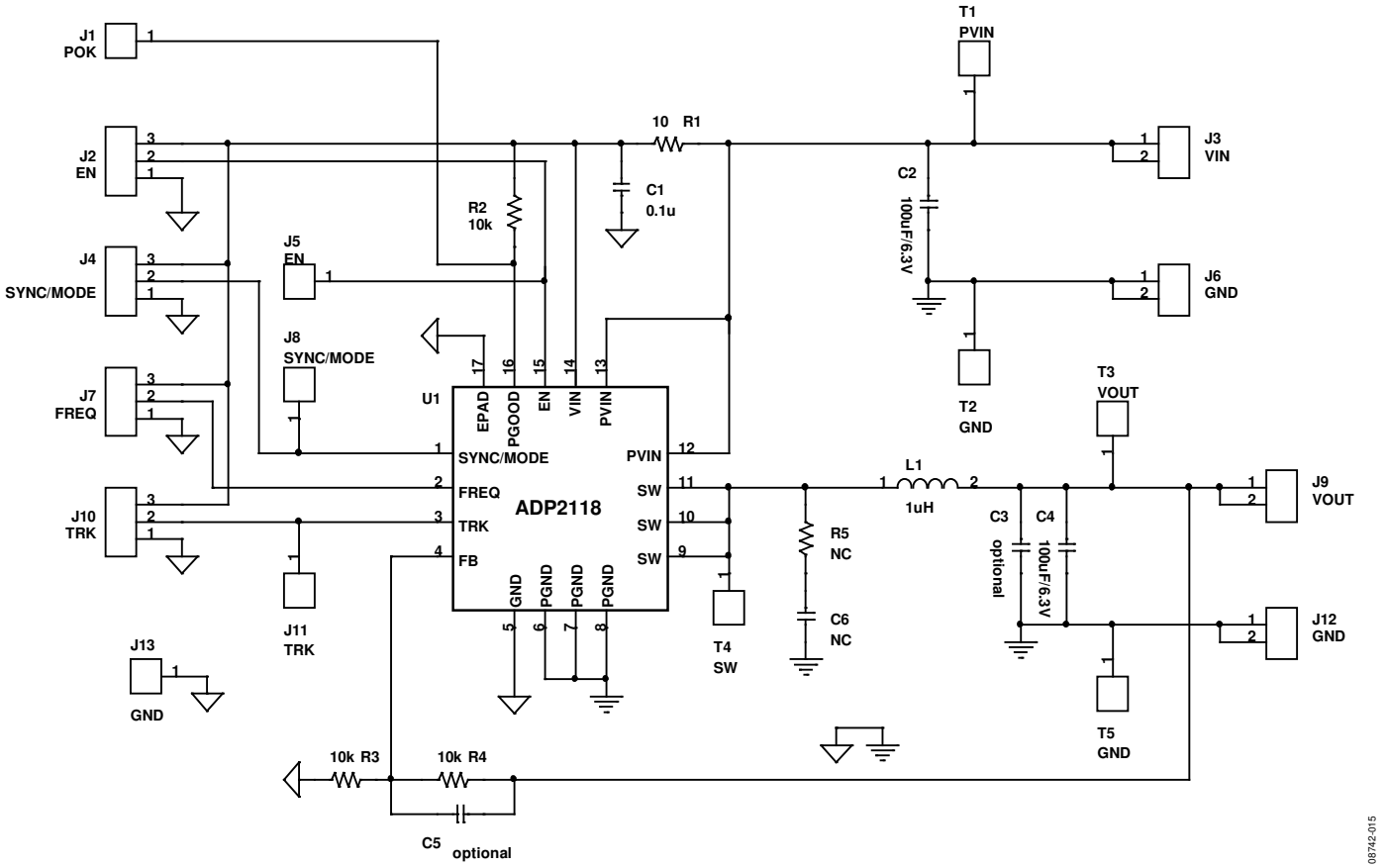

Figure 15. Evaluation Board Schematic

EVALUATION BOARD LAYOUT

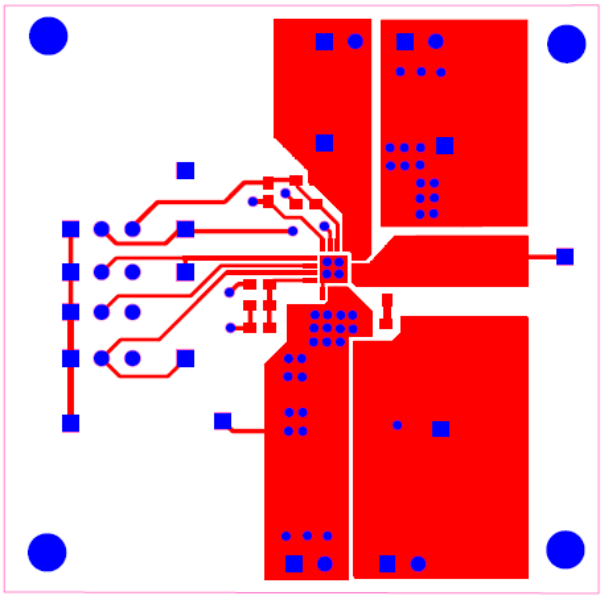

Figure 16.Top Layer

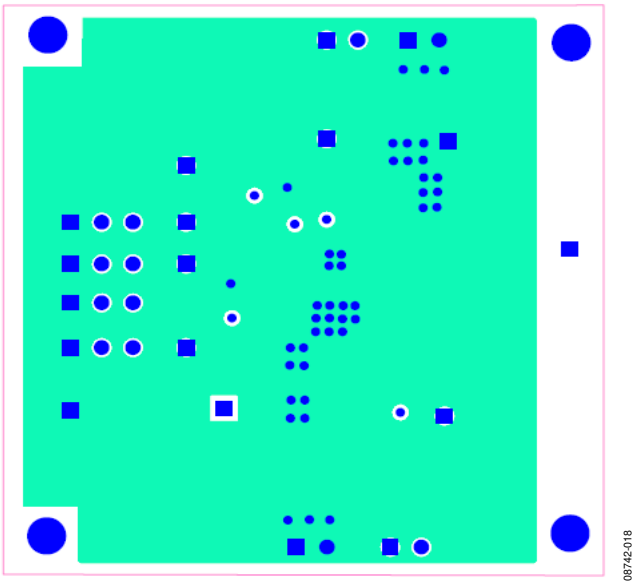

Figure 18. 2nd Layer

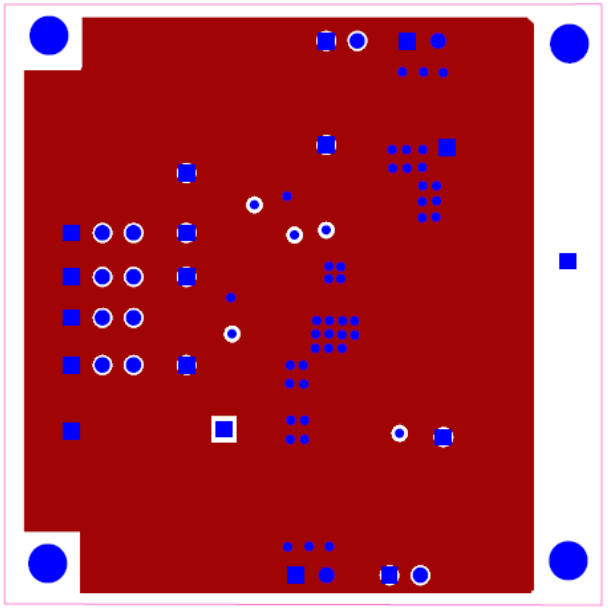

Figure 17. 3rd Layer

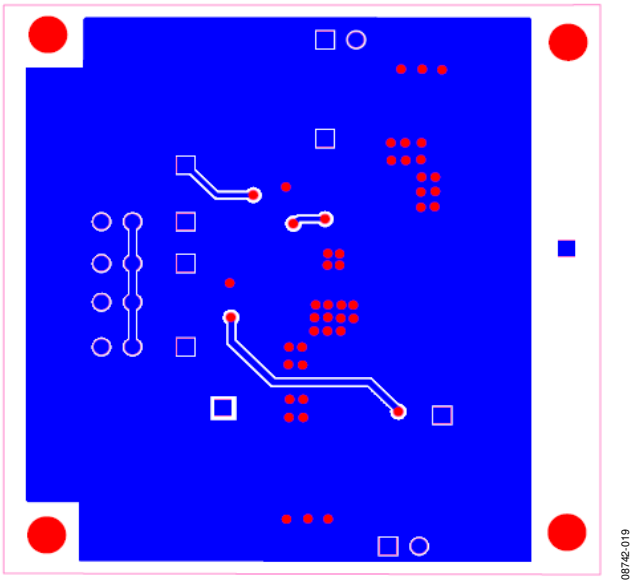

Figure 19. Bottom Layer

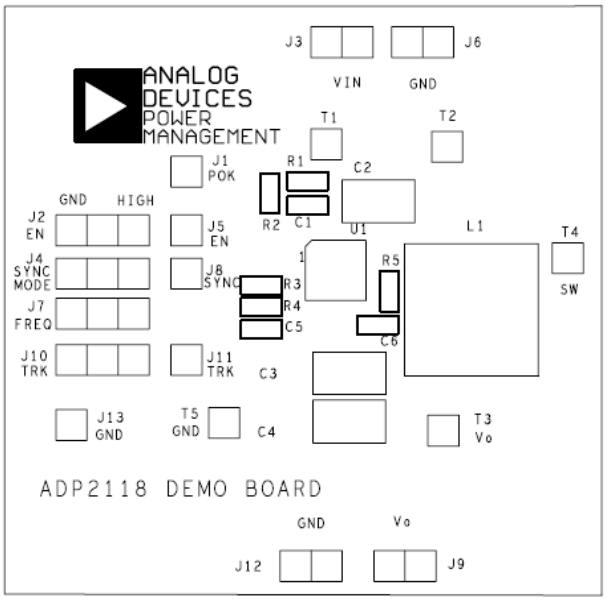

Figure 20. Silkscreen Top

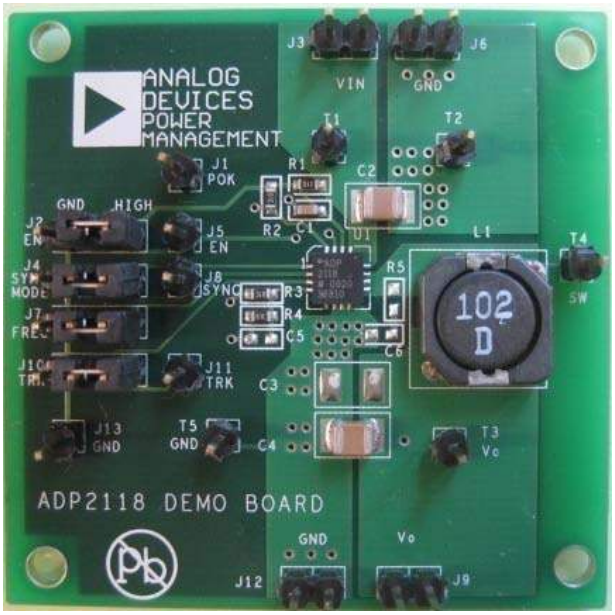

Figure 21. Evaluation Board

ORDERING INFORMATION

BILL OF MATERIALS

Table 8.

Qty	Reference Designator	Part Number	Type	Description	PCB Footprint	Vendor
1	C1	GRM188F51H104ZA01	Capacitor	0.1 µF, 50 V	C0603	Murata
1	C2	GRM32ER60J107ME20	Capacitor	100 µF, 6.3 V	C1210	Murata
1	C3	Optional	Capacitor	Optional	C1210	Murata
1	C4	GRM32ER60J107ME20	Capacitor	100 µF, 6.3 V	C1210	Murata
1	C5	Optional	Capacitor	Optional	C0603	Murata
1	C6	Optional	Capacitor	Optional	C0603	Murata
1	L1	MSS1038-102NL	Inductor	L = 1.0 µH, I_{RMS} = 7.3 A, I_{SAT} = 12.1 A, DCR = 6 mΩ	Coilcraft_MSS1038	Coil Craft
1	R1	CRCW060310R0FKEA	Resistor	10 Ω	R0603	Vishay Dale
1	R2	CRCW060310K0JKTA	Resistor	10 kΩ, 5%	R0603	Vishay Dale
1	R3	CRCW060310K0FKEA	Resistor	10 kΩ, 1%	R0603	Vishay Dale
1	R4	CRCW060310K0FKEA	Resistor	10 kΩ, 1%	R0603	Vishay Dale
1	R5	Optional	Resistor	Optional	R0603	Vishay Dale
1	U1	ADP2118	IC	3 A buck regulator	16-lead, 4 mm × 4 mm LFCSP	Analog Devices
5	J1, J5, J8, J11, J13	M20-9990245	Test point	SIP1	SIP1	Harwin
5	T1, T2, T3, T4, T5	M20-9990245	Test point	SIP1	SIP1	Harwin
4	J3, J6, J9, J12	M20-9990245	Connector	SIP2	SIP2	Harwin
4	J2, J4, J7, J10	M20-9990346	Jumper	SIP3	SIP3	Harwin

ORDERING GUIDE

Model[1]	Description
ADP2118-EVALZ	Adjustable Version ADP2118 Evaluation Board, V_{OUT} = 1.2 V

[1] Z = RoHS Compliant Part.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

NOTES

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