TEXAS INSTRUMENTS

TPS79601, TPS79613, TPS79618, TPS79625
TPS79628, TPS79630, TPS79633, TPS79650

SLVS351P – SEPTEMBER 2002 – REVISED MARCH 2015

TPS796xx Ultralow-Noise, High PSRR, Fast, RF, 1-A Low-Dropout Linear Regulators

1 Features

- 1-A Low-Dropout Regulator With Enable
- Available in Fixed and Adjustable (1.2 V to 5.5 V) Versions
- High PSRR (53 dB at 10 kHz)
- Ultralow-Noise (40 μV_{RMS}, TPS79630)
- Fast Start-Up Time (50 µs)
- Stable With a 1-µF Ceramic Capacitor
- Excellent Load and Line Transient Response
- Very Low Dropout Voltage (250 mV at Full Load, TPS79630)
- 3 × 3 VSON PowerPAD™, SOT223-6, and TO-263 Packages

2 Applications

- RF: VCOs, Receivers, ADCs
- Audio
- Bluetooth®, Wireless LAN
- Cellular and Cordless Telephones
- Handheld Organizers, PDAs

3 Description

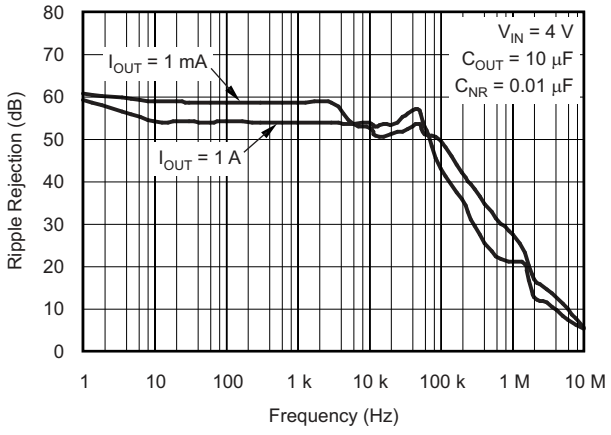
The TPS796 family of low-dropout (LDO) low-power linear voltage regulators features high power-supply rejection ratio (PSRR), ultralow-noise, fast start-up, and excellent line and load transient responses in small outline, 3 × 3 VSON, SOT223-6, and TO-263 packages. Each device in the family is stable with a small, 1-µF ceramic capacitor on the output. The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (for example, 250 mV at 1 A). Each device achieves fast start-up times (approximately 50 µs with a 0.001-µF bypass capacitor) while consuming very low quiescent current (265 µA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 µA. The TPS79630 exhibits approximately 40 μV_{RMS} of output voltage noise at 3.0-V output, with a 0.1-µF bypass capacitor. Applications with analog components that are noise sensitive, such as portable RF electronics, benefit from the high PSRR, low noise features, and need fast response time.

Device Information(1)

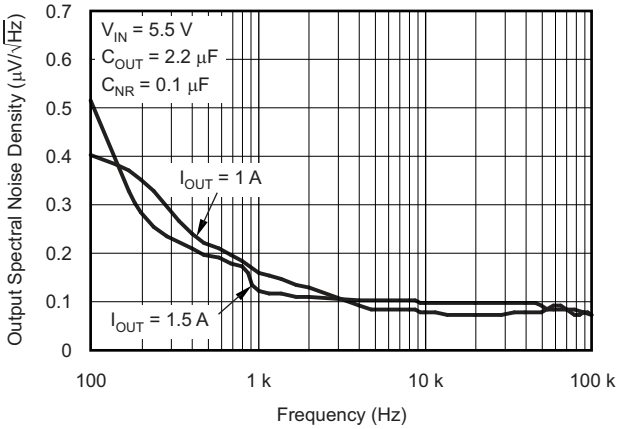
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS796	VSON (8)	3.00 mm × 3.00 mm
	SOT-223 (6)	6.50 mm × 3.50 mm
	TO-263 (5)	10.16 mm × 8.42 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Ripple Rejection vs Frequency
TPS79630



Output Spectral Noise Density vs Frequency
TPS79630



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (November 2013) to Revision P — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed front-page figure; updated graph style, replaced device pinouts with application circuits ... 1
- Changed *Pin Configuration and Functions* section; updated table format and added pinout drawings ... 3
- Changed "free-air" to "junction" temperature in condition statement for *Absolute Maximum Ratings* ... 4
- Changed V_{OUT} accuracy for TPS79601, test conditions and specified values ... 6
- Deleted Start-up time symbol ... 6
- Added *Thermal shutdown temperature* specification to *Electrical Characteristics* ... 6
- Added *Operating junction temperature* specification to *Electrical Characteristics* ... 6
- Added condition statement to *Typical Characteristics* ... 7

Changes from Revision N (January 2011) to Revision O — **Page**

- Changed Power-Supply Ripple Rejection 3rd test condition from "f = 10 Hz" to "f = 10 kHz" (typo) ... 6
- Changed Power-Supply Ripple Rejection 4th test condition from "f = 100 Hz" to "f = 100 kHz" (typo) ... 6

Changes from Revision M (October 2010) to Revision N — **Page**

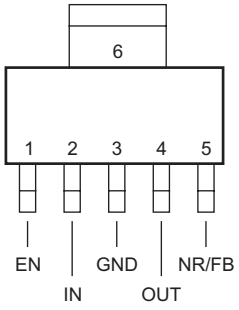
- Corrected typo in front-page figure ... 1

Changes from Revision L (August 2010) to Revision M — **Page**

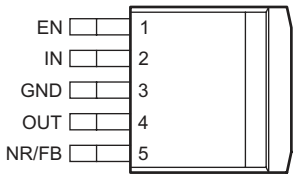
- Corrected typo in Figure 32 ... 21

5 Pin Configuration and Functions

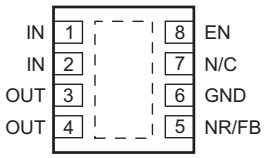
DCQ Package
6-Pin SOT-223
Top View



KTT Package
5-Pin TO-263
Top View



DRB Package
8-Pin VSON
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT223 TO-263	VSON		
EN	1	8	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
FB	5	5	I	This terminal is the feedback input voltage for the adjustable device.
GND	3, Tab	6, PowerPAD	—	Regulator ground
IN	2	1, 2	I	Unregulated input to the device.
N/C	—	7	—	Not internally connected. This pin must either be left open, or tied to GND.
NR	5	5	—	Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This improves power-supply rejection and reduces output noise.
OUT	4	3, 4	O	Output of the regulator.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	IN	–0.3	6	V
	EN	–0.3	V_{IN} + 0.3	
	OUT		6	
Current	Peak output	Internally limited		
Power dissipation	Continuous total	See *Thermal Information*		
Temperature	Junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		5.5	V
I_{OUT}	Output current	0		1	A
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1] [2]		TPS796xx[3]			UNIT
		DRB (VSON)	DCQ (SOT-223)	KTT (TO-263)	
		8 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.8	70.4	25	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	83	70	35	
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	N/A	N/A	
ψ_{JT}	Junction-to-top characterization parameter	2.1	6.8	1.5	
ψ_{JB}	Junction-to-board characterization parameter	17.8	30.1	8.52	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.1	6.3	0.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
(3) Thermal data for the DRB, DCQ, and DRV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
  (a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2 × 2 thermal via array.
  ii. DCQ: The exposed pad is connected to the PCB ground layer through a 3 × 2 thermal via array.
  iii. KTT: The exposed pad is connected to the PCB ground layer through a 5 × 4 thermal via array.
  (b) i. DRB: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
  ii. DCQ: Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
  iii. KTT: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
  (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area. To understand the effects of the copper area on thermal performance, see *Power Dissipation* and *Estimating Junction Temperature*.

6.5 Electrical Characteristics

Over recommended operating temperature range (T_J = –40°C to 125°C), $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)}$ + 1 V(1), I_{OUT} = 1 mA, C_{OUT} = 10 µF, and C_{NR} = 0.01 µF, unless otherwise noted. Typical values are at 25°C.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage(1)				2.7		5.5	V
V_{FB}	Internal reference (TPS79601)				1.2	1.225	1.25	V
I_{OUT}	Continuous output current				0		1	A
V_{OUT}	Output voltage range	TPS79601			1.225		5.5 – V_{DO}	V
	Accuracy	TPS79601(2)	0 µA ≤ I_{OUT} ≤ 1 A, $V_{OUT(nom)}$ + 1 V ≤ V_{IN} ≤ 5.5 V(1)		0.98$V_{OUT(nom)}$	$V_{OUT(nom)}$	1.02$V_{OUT(nom)}$	V
		Fixed V_{OUT} < 5 V	0 µA ≤ I_{OUT} ≤ 1 A, $V_{OUT(nom)}$ + 1 V ≤ V_{IN} ≤ 5.5 V(1)		–2%		2%	
		Fixed V_{OUT} = 5 V	0 µA ≤ I_{OUT} ≤ 1 A, $V_{OUT(nom)}$ + 1 V ≤ V_{IN} ≤ 5.5 V(1)		–3%		3%	
$\Delta V_{O(\Delta VI)}$	Line regulation(1)		V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V			0.05	0.12	%/V
$\Delta V_{O(\Delta IO)}$	Load regulation		0 µA ≤ I_{OUT} ≤ 1 A			5		mV
V_{DO}	Dropout voltage(3) (V_{IN} = $V_{OUT(nom)}$ – 0.1 V)	TPS79628	I_{OUT} = 1 A			270	365	mV
		TPS79628DRB	I_{OUT} = 250 mA			52	90	
		TPS79630	I_{OUT} = 1 A			250	345	
		TPS79633	I_{OUT} = 1 A			220	325	
		TPS79650	I_{OUT} = 1 A			200	300	
I_{CL}	Output current limit		V_{OUT} = 0 V		2.4		4.2	A
I_{GND}	Ground pin current		0 µA ≤ I_{OUT} ≤ 1 A			265	385	µA
I_{SHDN}	Shutdown current(4)		V_{EN} = 0 V, 2.7 V ≤ V_{IN} ≤ 5.5 V			0.07	1	µA
I_{FB}	Feedback pin current		V_{FB} = 1.225 V				1	µA
PSRR	Power-supply rejection ratio (TPS79630)		f = 100 Hz. I_{OUT} = 10 mA			59		dB
			f = 100 Hz, I_{OUT} = 1 A			54		
			f = 10 kHz, I_{OUT} = 1A			53		
			f = 100 kHz, I_{OUT} = 1 A			42		
V_n	Output noise voltage (TPS79630)		BW = 100 Hz to 100 kHz, I_{OUT} = 1 A	C_{NR} = 0.001 µF		54		µV_{RMS}
				C_{NR} = 0.0047 µF		46		
				C_{NR} = 0.01 µF		41		
				C_{NR} = 0.1 µF		40		
	Start-up time (TPS79630)		R_L = 3 Ω, C_{OUT} = 1 µF	C_{NR} = 0.001 µF		50		µs
				C_{NR} = 0.0047 µF		75		
				C_{NR} = 0.01 µF		110		
$V_{EN(HI)}$	Enable high (enabled)		2.7 V ≤ V_{IN} ≤ 5.5 V		1.7		V_{IN}	V
$V_{EN(LO)}$	Enable low (shutdown)		2.7 V ≤ V_{IN} ≤ 5.5 V		0		0.7	V
$I_{EN(HI)}$	Enable pin current, enabled		V_{EN} = 0 V		–1		1	µA
UVLO	Undervoltage lockout		V_{CC} rising		2.25		2.65	V
	Hysteresis					100		mV
T_{sd}	Thermal shutdown temperature		Shutdown, temperature increasing			165		°C
			Reset, temperature decreasing			140		
T_J	Operating junction temperature				–40		125	°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.7 V, whichever is greater. TPS79650 is tested at V_{IN} = 5.5 V.
(2) Tolerance of external resistors not included in this specification.
(3) V_{DO} is not measured for TPS79618 and TPS79625 because minimum V_{IN} = 2.7 V.
(4) For adjustable version, this applies only after V_{IN} is applied; then V_{EN} transitions high to low.

6.6 Typical Characteristics

At $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1$ V, $I_{OUT} = 1$ mA, $C_{OUT} = 10$ µF, $C_{NR} = 0.01$ µF, $C_{IN} = 2.2$ µF, and $T_J = 25°C$, unless otherwise noted.

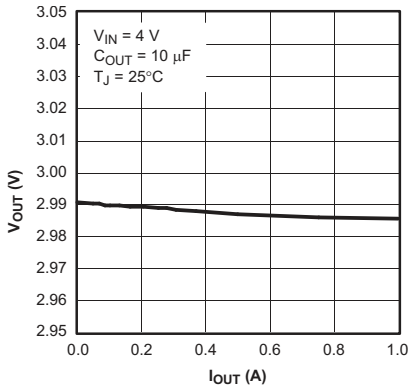


Figure 1. TPS79630 Output Voltage vs Output Current

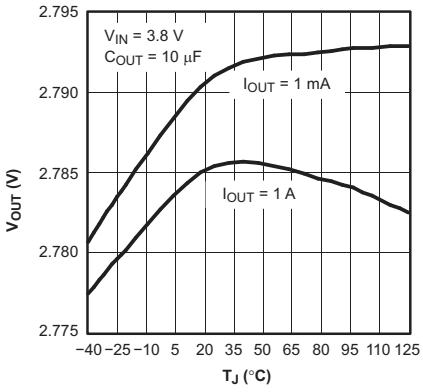


Figure 2. TPS79628 Output Voltage vs Junction Temperature

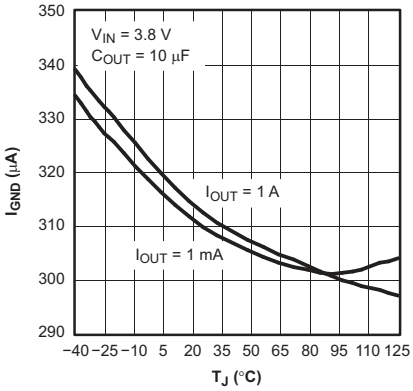


Figure 3. TPS79628 Ground Current vs Junction Temperature

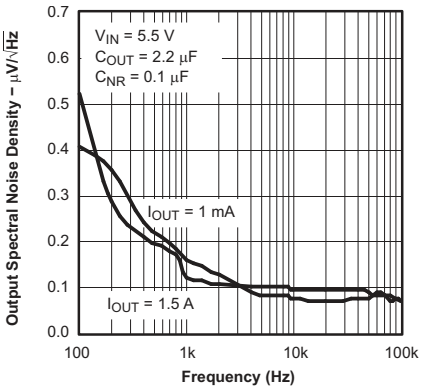


Figure 4. TPS79630 Output Spectral Noise Density vs Frequency

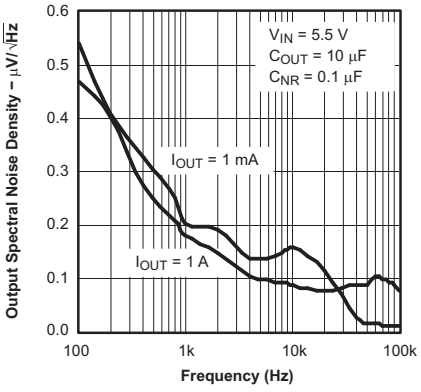


Figure 5. TPS79630 Output Spectral Noise Density vs Frequency

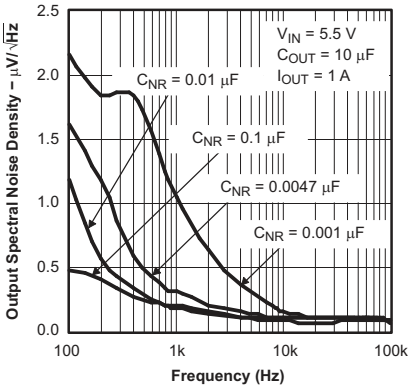


Figure 6. TPS79630 Output Spectral Noise Density vs Frequency

Typical Characteristics (continued)

At $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1$ V, $I_{OUT} = 1$ mA, $C_{OUT} = 10$ µF, $C_{NR} = 0.01$ µF, $C_{IN} = 2.2$ µF, and $T_J = 25°C$, unless otherwise noted.

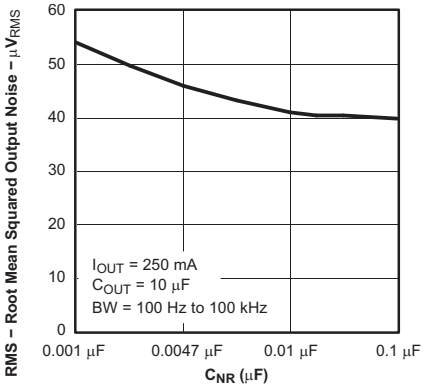


Figure 7. TPS79630 Root Mean Squared Output Noise vs Bypass Capacitance

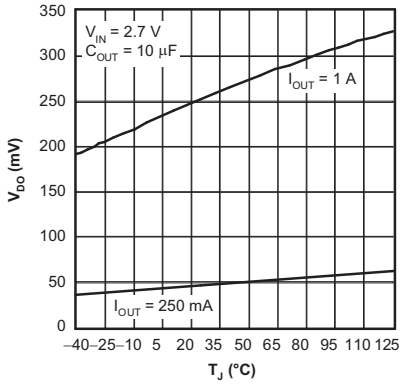


Figure 8. TPS79628 Dropout Voltage vs Junction Temperature

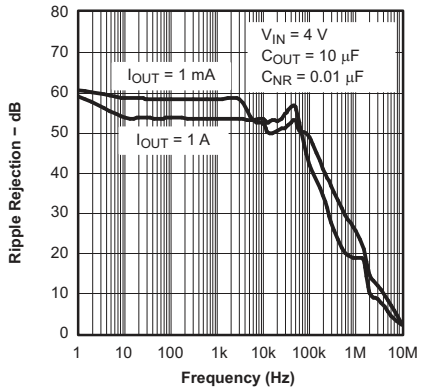


Figure 9. TPS79630 Ripple Rejection vs Frequency

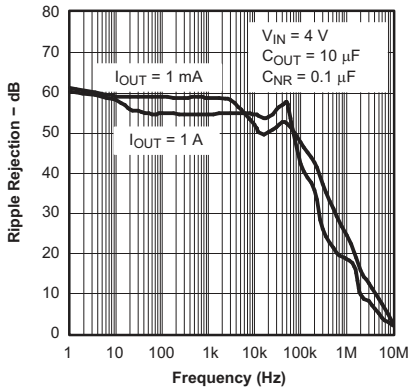


Figure 10. TPS79630 Ripple Rejection vs Frequency

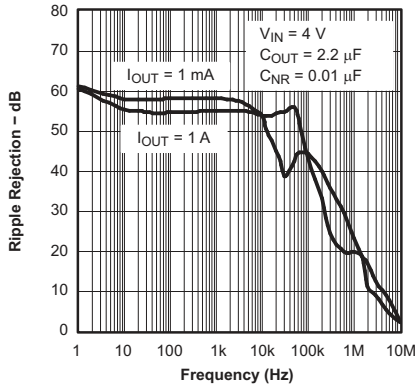


Figure 11. TPS79630 Ripple Rejection vs Frequency

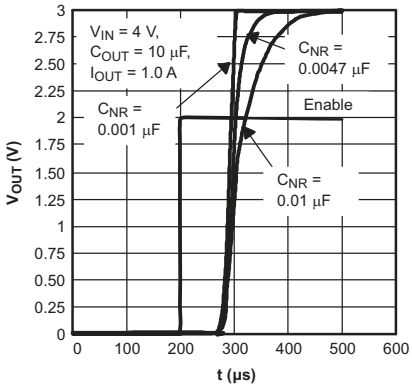


Figure 12. Start-Up Time

Typical Characteristics (continued)

At $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1$ V, $I_{OUT} = 1$ mA, $C_{OUT} = 10$ µF, $C_{NR} = 0.01$ µF, $C_{IN} = 2.2$ µF, and $T_J = 25°C$, unless otherwise noted.

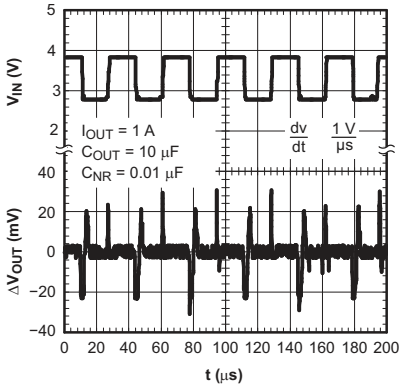


Figure 13. TPS79618 Line Transient Response

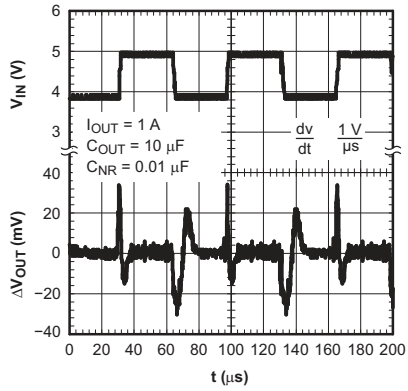


Figure 14. TPS79630 Line Transient Response

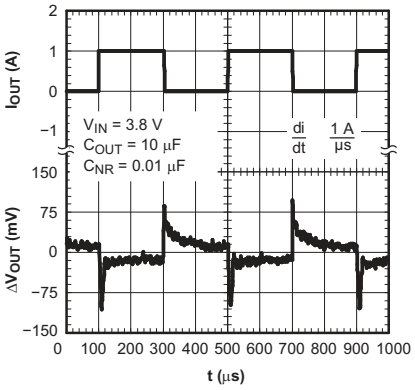


Figure 15. TPS79628 Load Transient Response

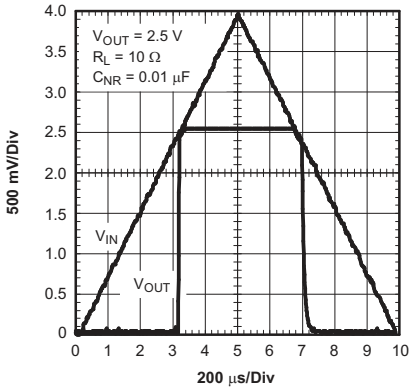


Figure 16. TPS79625 Power Up/Power Down

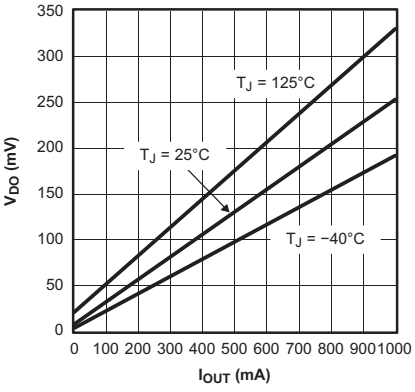


Figure 17. TPS79630 Dropout Voltage vs Output Current

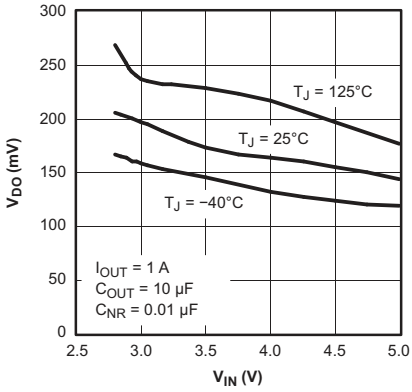


Figure 18. TPS79601 Dropout Voltage vs Input Voltage

Typical Characteristics (continued)

At $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1$ V, $I_{OUT} = 1$ mA, $C_{OUT} = 10$ µF, $C_{NR} = 0.01$ µF, $C_{IN} = 2.2$ µF, and $T_J = 25°C$, unless otherwise noted.

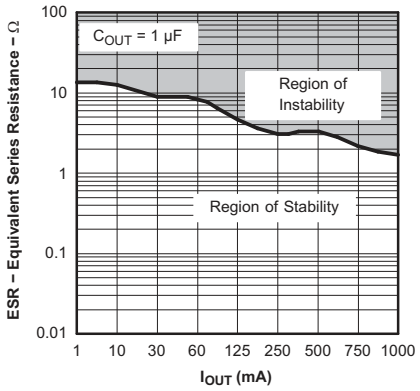


Figure 19. TPS79630 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

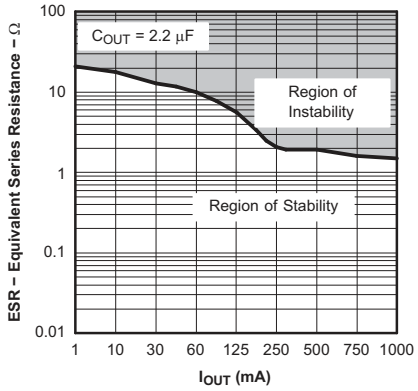


Figure 20. TPS79630 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

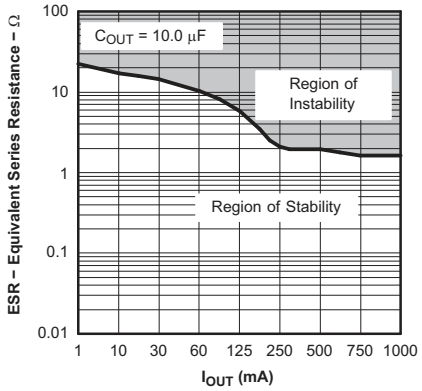


Figure 21. TPS79630 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

7 Detailed Description

7.1 Overview

The TPS796 family of low-dropout (LDO) regulators combines the high performance required of many RF and precision analog applications with low current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection at very low headroom (V_{IN} – V_{OUT}). A noise-reduction pin is provided to bypass noise generated by the band-gap reference and to improve PSRR, while a quick-start circuit quickly charges this capacitor at start-up. All versions have thermal and overcurrent protection, and are fully specified from –40°C to 125°C.

7.2 Functional Block Diagrams

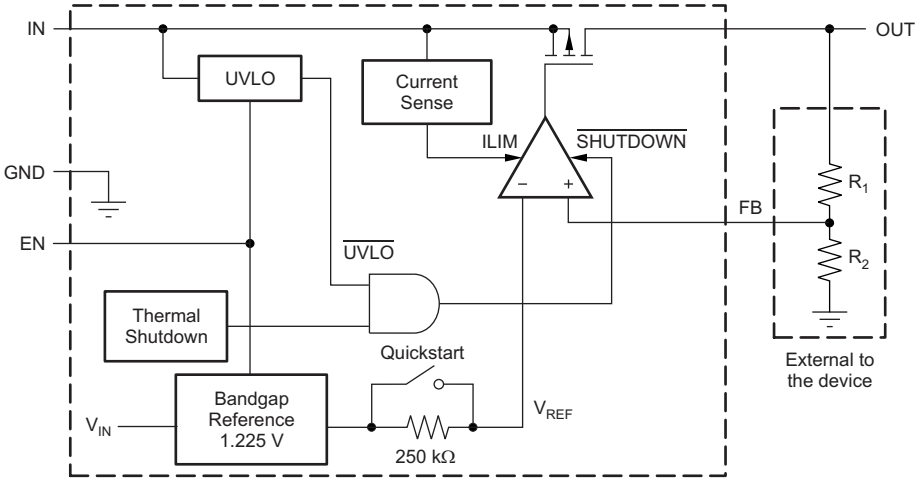


Figure 22. Functional Block Diagram—Adjustable Version

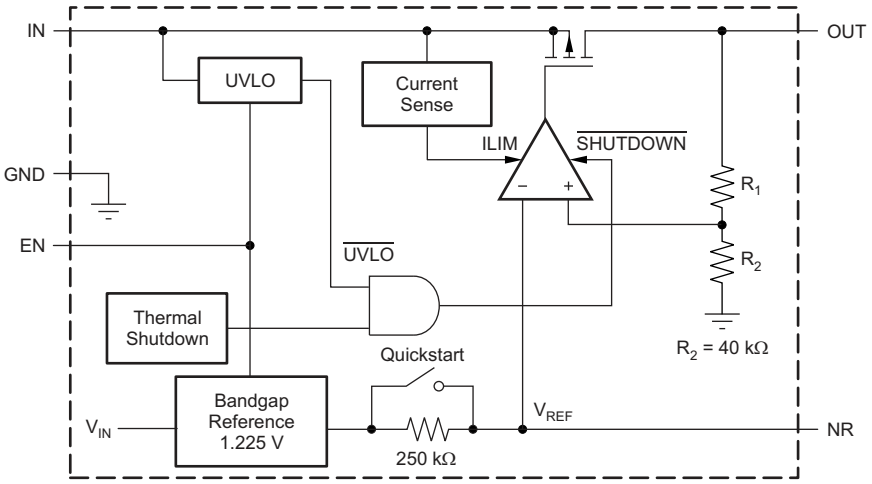


Figure 23. Functional Block Diagram—Fixed Version

7.3 Feature Description

7.3.1 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

7.3.2 Start-Up

The TPS796 uses a start-up circuit to quickly charge the noise reduction capacitor, C_{NR}, if present (see the *Functional Block Diagrams*). This circuit allows for the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate for this configuration.

For the fastest start-up, apply V_{IN} first, and then drive the enable pin (EN) high. If EN is tied to IN, start-up is somewhat slower. To ensure that C_{NR} is fully charged during start-up, use a 0.1-µF or smaller capacitor.

7.3.3 Undervoltage Lockout (UVLO)

The TPS796 uses an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has approximately 100 mV of hysteresis to help reject input voltage drops when the regulator first turns on.

7.3.4 Regulator Protection

The TPS796xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS796xx features internal current limiting and thermal protection. During normal operation, the TPS796xx limits output current to approximately 2.8 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C (T_{sd}), thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

7.4 Device Functional Modes

Table 1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Disabled	—	$V_{EN} < V_{EN(LO)}$	—	$T_J > T_{SD}$

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$).
- The enable voltage has previously exceeded the enable rising threshold voltage and not yet decreased below the enable falling threshold.
- The output current is less than the current limit ($I_{OUT} < I_{CL}$).
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$).

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature ($T_J > T_{SD}$).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS796xx family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (265 µA typically), and enable input to reduce supply currents to less than 1 µA when the regulator is turned off.

8.2 Typical Application

A typical application circuit is shown in Figure 24.

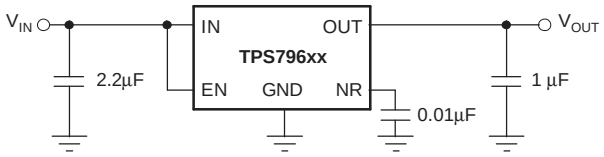


Figure 24. Typical Application Circuit

8.2.1 Design Requirements

Table 2 lists the design parameters.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.3V
Output voltage	2.5 V
Maximum output current	700 mA

8.2.2 Detailed Design Procedure

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND terminal current, and power the load.

8.2.2.1 Input and Output Capacitor Requirements

A 2.2-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS796xx, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like most low dropout regulators, the TPS796xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitor is 1 µF. Any 1-µF or larger ceramic capacitor is suitable.

8.2.2.2 Output Noise

The internal voltage reference is a key source of noise in an LDO regulator. The TPS796xx has an NR pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1 µF in order to ensure that it is fully charged during the quickstart time provided by the internal switch shown in the functional block diagram.

For example, the TPS79630 exhibits 40 μV_{RMS} of output voltage noise using a 0.1-µF ceramic bypass capacitor and a 10-µF ceramic output capacitor. The output starts up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 250-kΩ resistor and external capacitor.

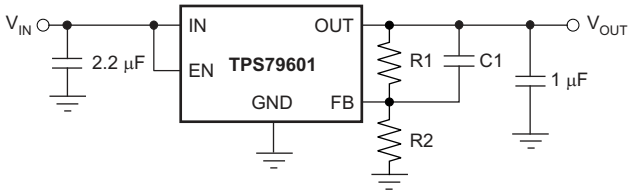
8.2.2.3 Dropout Voltage

The TPS796 uses a PMOS pass transistor to achieve a low dropout voltage. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and $r_{DS(on)}$ of the PMOS pass element is the input-to-output resistance. Because the PMOS device behaves like a resistor in dropout, V_{DO} approximately scales with the output current.

As with any linear regulator, PSRR degrades as (V_{IN} – V_{OUT}) approaches dropout. This effect is illustrated in Figure 9 through Figure 11 in *Typical Characteristics*.

8.2.2.4 Programming the TPS79601 Adjustable LDO Regulator

The output voltage of the TPS79601 adjustable regulator is programmed using an external resistor divider, as Figure 25 shows.



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	C1
1.8 V	14.0 kΩ	30.1 kΩ	33 pF
3.6 V	57.9 kΩ	30.1 kΩ	15 pF

Figure 25. Typical Application, Adjustable Output

The output voltage is calculated using Equation 1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

where

- V_{REF} = 1.2246 V typical (the internal reference voltage)

Resistors R_1 and R_2 should be chosen for approximately 40-µA divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Higher values should be avoided, as leakage current at FB increases the output voltage error.

The recommended design procedure is to choose R_2 = 30.1 kΩ to set the divider current at 40 µA, C_1 = 15 pF for stability, and then calculate R_1 using Equation 2:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \quad (2)$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB. The approximate value of this capacitor can be calculated as Equation 3:

$$C1 = \frac{\left(3 \times 10^{-7}\right) \times (R1 + R2)}{(R1 \times R2)} \quad (3)$$

The suggested value of this capacitor for several resistor ratios is shown in the table in Figure 25. If this capacitor is not used (such as in a unity-gain configuration) then the minimum recommended output capacitor is 2.2 µF instead of 1 µF.

8.2.3 Application Curves

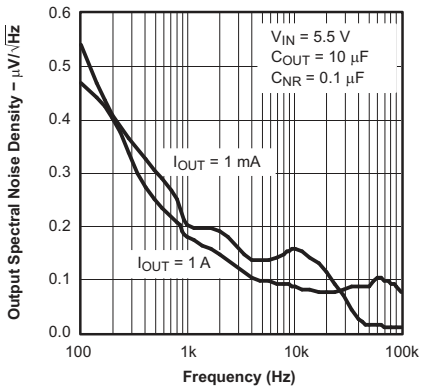


Figure 26. TPS79630 Output Spectral Noise Density vs Frequency

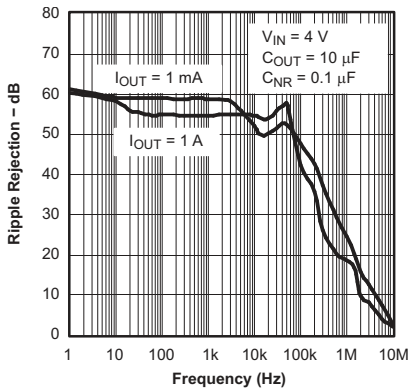


Figure 27. TPS79630 Ripple Rejection vs Frequency

8.3 Do's and Don'ts

Place at least one 1-µF ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Connect a 2.2-µF low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator.

Do not exceed the absolute maximum ratings.

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between 2.7 V and 5.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply is well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendation to Improve PSRR and Noise Performance

To improve AC measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.

10.1.2 Regulator Mounting

The tab of the SOT223-6 package is electrically connected to ground. For best thermal performance, the tab of the surface-mount version should be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation.

Solder pad footprint recommendations for the devices are presented in an application bulletin *Solder Pad Recommendations for Surface-Mount Devices*, SBFA015, available from the TI website (www.ti.com).

10.2 Layout Examples

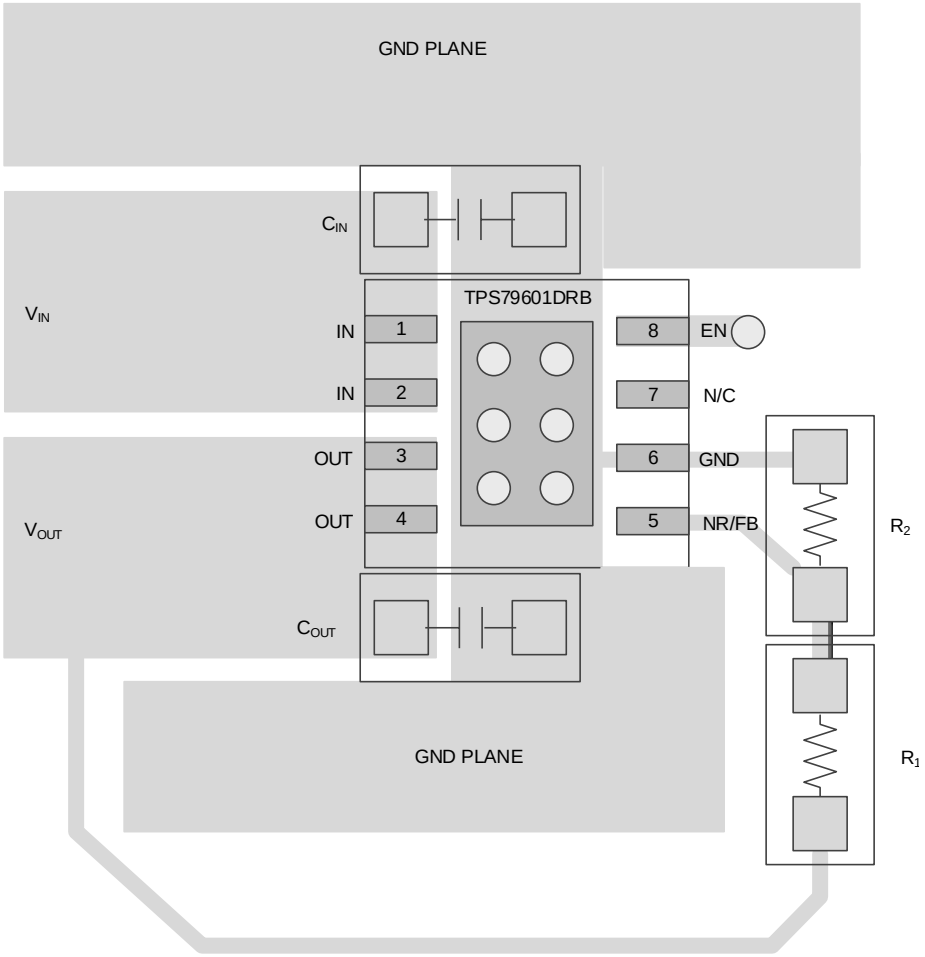


Figure 28. TPS79601 (Adjustable Voltage Version)—DRB Layout Example

Layout Examples (continued)

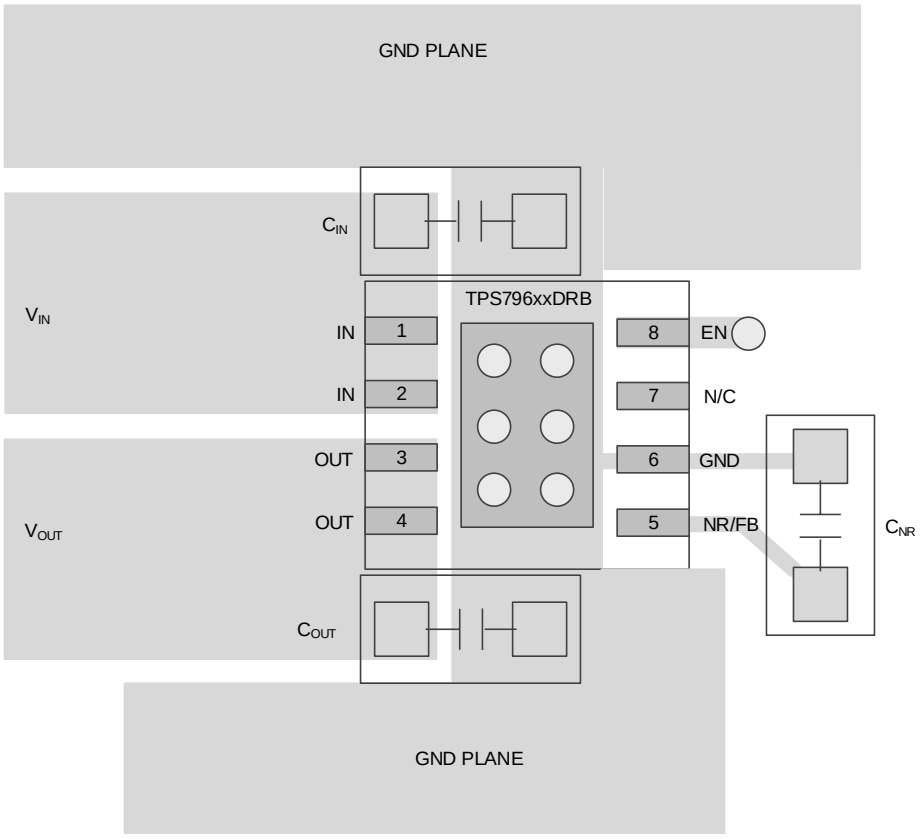


Figure 29. TPS796xx (Fixed Voltage Versions)—DRB Layout Example

10.3 Thermal Considerations

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 4:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

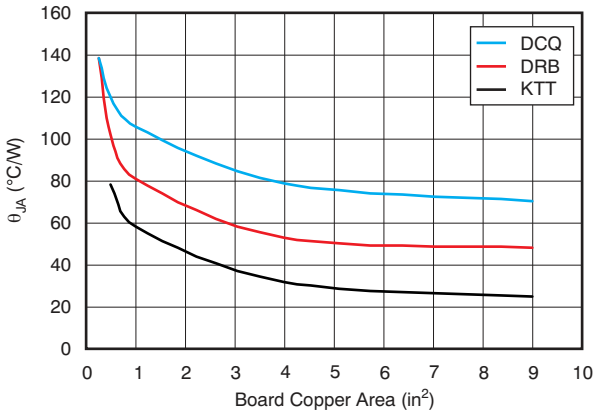
Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the VSON (DRB) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. On both SOT-223 (DCQ) and TO-263 (KTT) packages, the primary conduction path for heat is through the tab to the PCB. That tab should be connected to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 5:

$$R_{\theta JA} = \frac{(+125°C - T_A)}{P_D}, \quad (5)$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 30.

Thermal Considerations (continued)



θ_{JA} value at board size of $9in^2$ (that is, 3in × 3in) is a JEDEC standard.

Figure 30. Θ_{JA} vs Board Size

Figure 30 shows the variation of θ_{JA} as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

NOTE

When the device is mounted on an application PCB, it is strongly recommended to use Ψ_{JT} and Ψ_{JB}, as explained in *Estimating Junction Temperature*.

10.4 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in *Thermal Information*, the junction temperature can be estimated with corresponding formulas (given in Equation 6). For backwards compatibility, an older $\theta_{JC,Top}$ parameter is listed as well.

Ψ_{JT}: $T_J = T_T + \Psi_{JT} \bullet P_D$

Ψ_{JB}: $T_J = T_B + \Psi_{JB} \bullet P_D$

where

- P_D is the power dissipation shown by Equation 5
- T_T is the temperature at the center-top of the IC package
- T_B is the PCB temperature measured 1mm away from the IC package *on the PCB surface* (as Figure 32 shows). (6)

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note SBVA025, *Using New Thermal Metrics*, available at www.ti.com.

By looking at Figure 31, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have very little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with Equation 6 is a good way to estimate T_J by simply measuring T_T or T_B, regardless of the application board size.

Estimating Junction Temperature (continued)

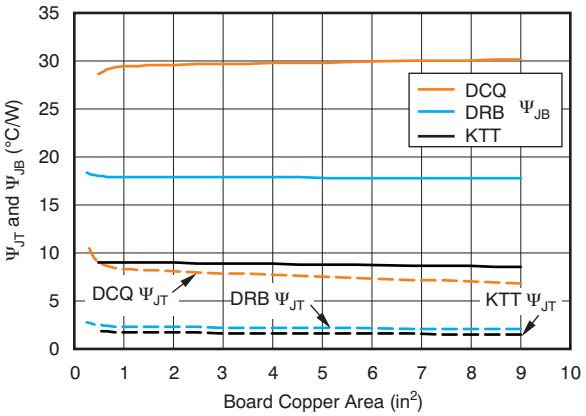
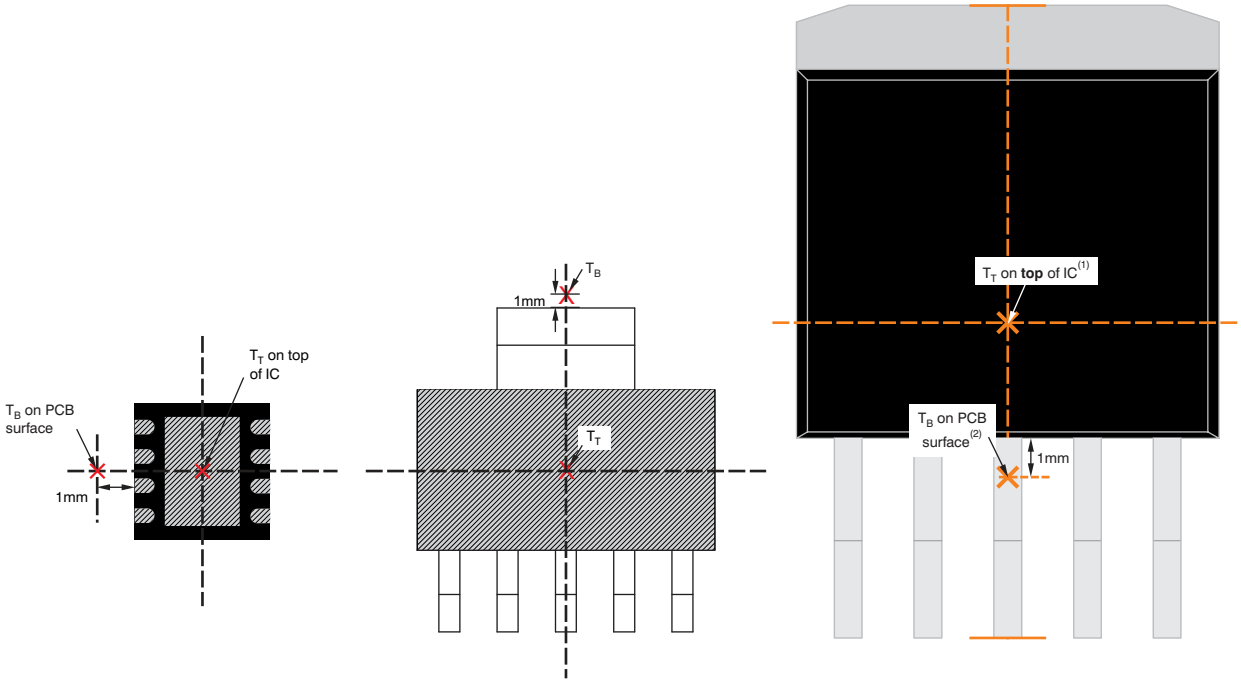


Figure 31. Ψ_{JT} And Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, refer to application report SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com. For further information, refer to application report SPRA953, *IC Package Thermal Metrics*, also available on the TI website.



(a) Example DRB (VSON) Package Measurement (b) Example DCQ (SOT-223) Package Measurement (c) Example KTT (TO-263) Package Measurement

(1) T_T is measured at the center of both the X- and Y-dimensional axes.

(2) T_B is measured ***below*** the package lead on the PCB surface.

Figure 32. Measuring Points For T_T and T_B

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS796. The TPS79601DRBEVM evaluation module can be requested at the TI website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS796 is available through the product folders under simulation models.

11.1.2 Device Nomenclature

Table 3. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS796**xx(x)** ***yyy z***	**xx(x)** is nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). **yyy** is package designator. **z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *Using New Thermal Metrics*, SBVA025
- *IC Package Thermal Metrics*, SPRA953
- *TPS79601DRBEVM User's Guide*, SLVU130
- *Solder Pad Recommendations for Surface-Mount Devices*, SBFA015

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS79601	Click here	Click here	Click here	Click here	Click here
TPS79613	Click here	Click here	Click here	Click here	Click here
TPS79618	Click here	Click here	Click here	Click here	Click here
TPS79625	Click here	Click here	Click here	Click here	Click here
TPS79628	Click here	Click here	Click here	Click here	Click here
TPS79630	Click here	Click here	Click here	Click here	Click here
TPS79633	Click here	Click here	Click here	Click here	Click here
TPS79650	Click here	Click here	Click here	Click here	Click here
TPS79601	Click here	Click here	Click here	Click here	Click here
TPS79613	Click here	Click here	Click here	Click here	Click here
TPS79618	Click here	Click here	Click here	Click here	Click here

Related Links (continued)

Table 4. Related Links (continued)

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS79625	Click here	Click here	Click here	Click here	Click here
TPS79628	Click here	Click here	Click here	Click here	Click here
TPS79630	Click here	Click here	Click here	Click here	Click here
TPS79633	Click here	Click here	Click here	Click here	Click here
TPS79650	Click here	Click here	Click here	Click here	Click here

11.4 Trademarks

PowerPAD is a trademark of Texas Instruments Inc.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79601DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	PS79601	Samples
TPS79601DCQG4	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79601	Samples
TPS79601DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	PS79601	Samples
TPS79601DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CES	Samples
TPS79601DRBRG4	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CES	Samples
TPS79601DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CES	Samples
TPS79601DRBTG4	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CES	Samples
TPS79601KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TPS 79601	Samples
TPS79601KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TPS 79601	Samples
TPS79613DRBR	NRND	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CCT	
TPS79618DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79618	Samples
TPS79618DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	PS79618	Samples
TPS79618KTTR	NRND	DDPAK/ TO-263	KTT	5	500	RoHS & Green	SN	Level-2-260C-1 YEAR		TPS 79618	
TPS79625DCQ	NRND	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79625	
TPS79625DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	PS79625	Samples
TPS79625KTTR	LIFEBUY	DDPAK/ TO-263	KTT	5	500	RoHS & Green	SN	Level-2-260C-1 YEAR		TPS 79625	
TPS79628DCQ	NRND	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79628	
TPS79628DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79628	Samples
TPS79628DRBT	LIFEBUY	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AMI	
TPS79630DCQ	LIFEBUY	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79630	
TPS79630DCQG4	LIFEBUY	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79630	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79630DCQR	LIFEBUY	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79630	
TPS79630KTTR	NRND	DDPAK/ TO-263	KTT	5	500	RoHS & Green	SN	Level-2-260C-1 YEAR		TPS 79630	
TPS79633DCQ	NRND	SOT-223	DCQ	6	78	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	PS79633	
TPS79633DCQG4	LIFEBUY	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79633	
TPS79633DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	PS79633	Samples
TPS79633DCQRG4	NRND	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79633	
TPS79633KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS & Green	SN	Level-2-260C-1 YEAR		TPS 79633	Samples
TPS79633KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TPS 79633	Samples
TPS79650DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79650	Samples
TPS79650DCQG4	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79650	Samples
TPS79650DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79650	Samples
TPS79650DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BYZ	Samples
TPS79650DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BYZ	Samples
TPS79650DRBTG4	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BYZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

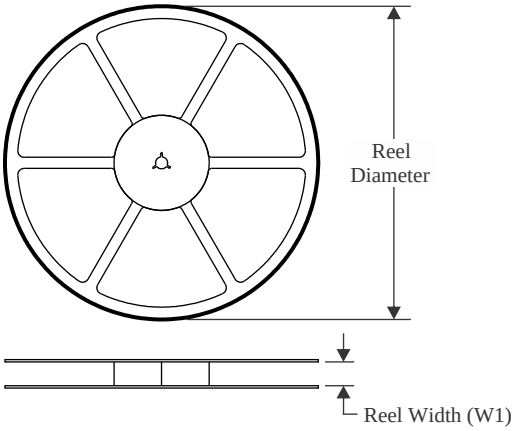
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

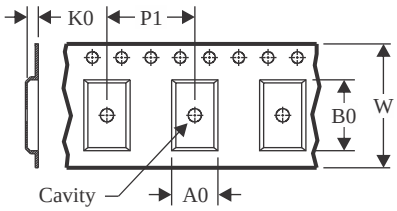
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

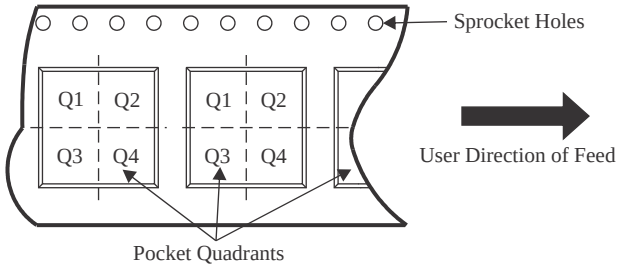


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

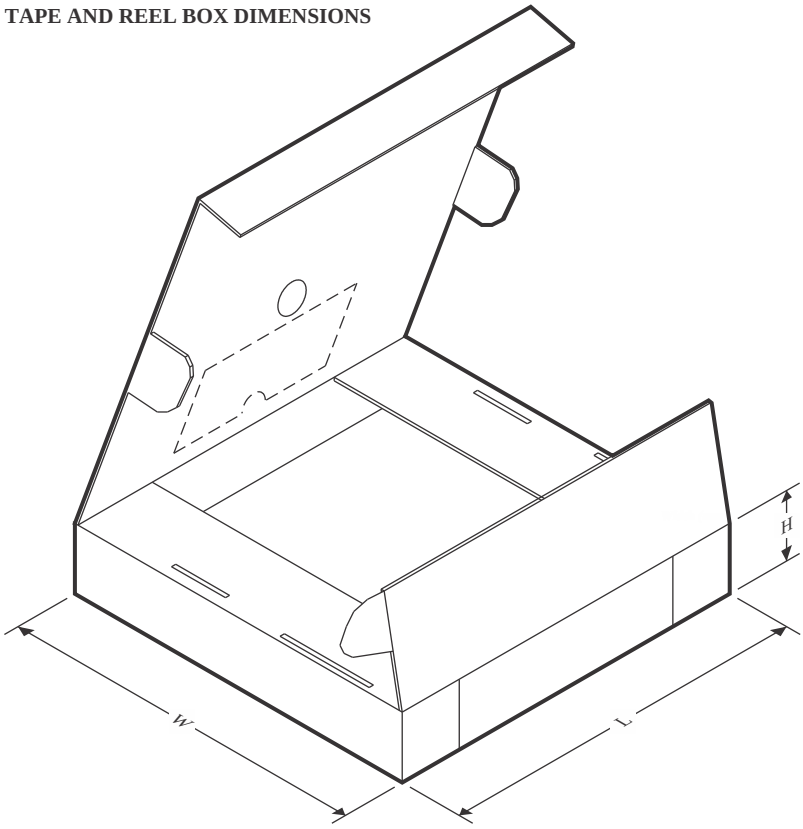


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79601DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS79601DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79601DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79601KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS79613DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79618DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS79618KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS79625DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS79625KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS79628DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79628DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79630DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79630KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79633DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS79633DCQRG4	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79633KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS79650DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79650DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79650DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

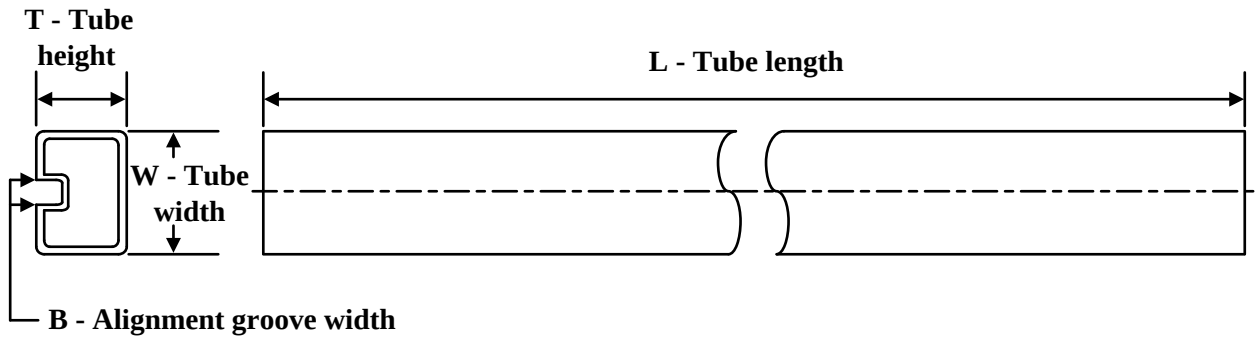


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79601DCQR	SOT-223	DCQ	6	2500	356.0	356.0	35.0
TPS79601DRBR	SON	DRB	8	3000	356.0	356.0	35.0
TPS79601DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS79601KTTR	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
TPS79613DRBR	SON	DRB	8	3000	356.0	356.0	35.0
TPS79618DCQR	SOT-223	DCQ	6	2500	356.0	356.0	35.0
TPS79618KTTR	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
TPS79625DCQR	SOT-223	DCQ	6	2500	356.0	356.0	35.0
TPS79625KTTR	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
TPS79628DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS79628DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS79630DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS79630KTTR	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
TPS79633DCQR	SOT-223	DCQ	6	2500	356.0	356.0	35.0
TPS79633DCQRG4	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS79633KTTR	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
TPS79650DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS79650DRBR	SON	DRB	8	3000	356.0	356.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79650DRBT	SON	DRB	8	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

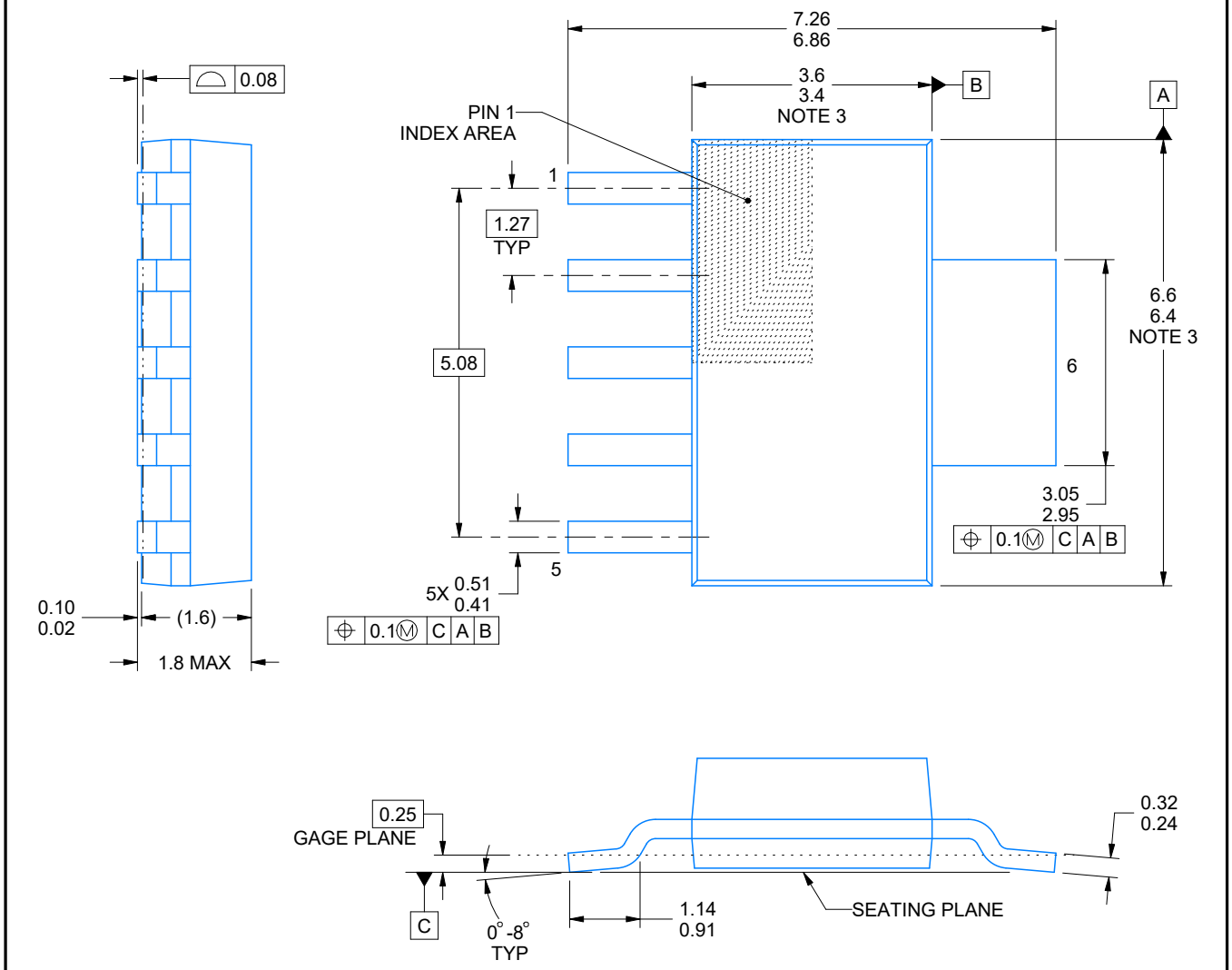
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS79601DCQ	DCQ	SOT-223	6	78	543	8.6	3606.8	2.67
TPS79601DCQG4	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79618DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79625DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79628DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79630DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79630DCQG4	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79633DCQ	DCQ	SOT-223	6	78	543	8.6	3606.8	2.67
TPS79633DCQG4	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79650DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79650DCQG4	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68

PACKAGE OUTLINE

DCQ0006A

SOT - 1.8 mm max height

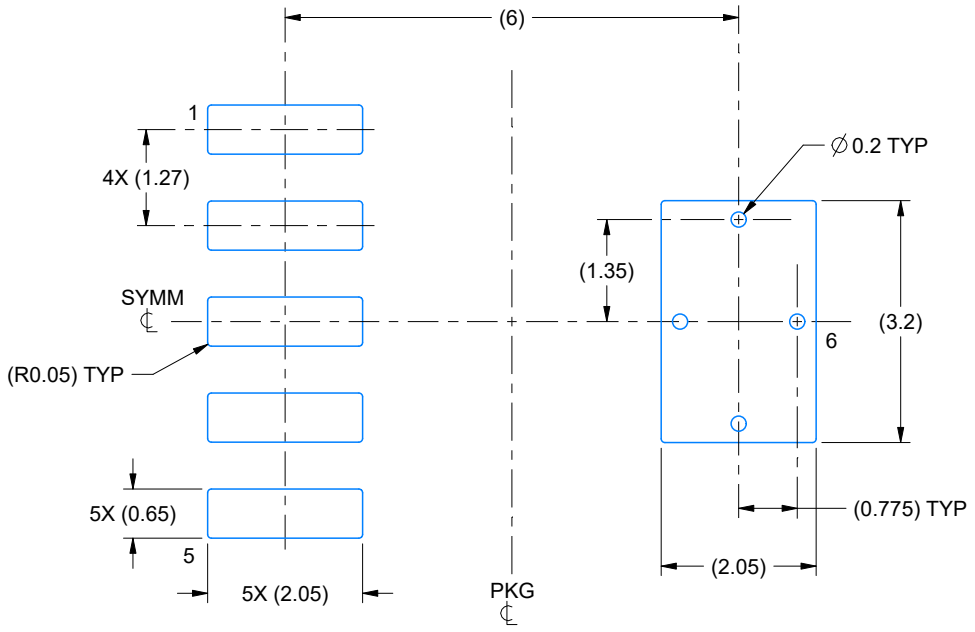
PLASTIC SMALL OUTLINE



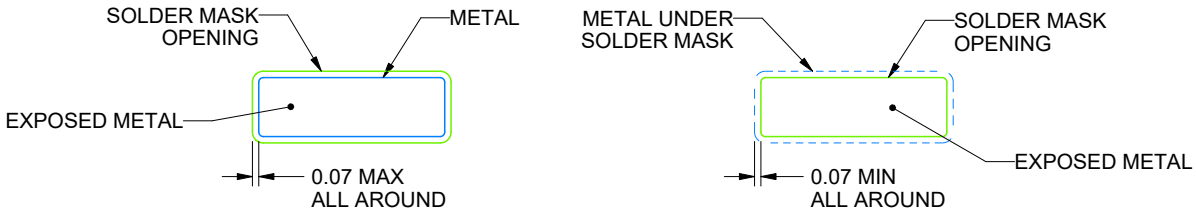
4214845/C 11/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

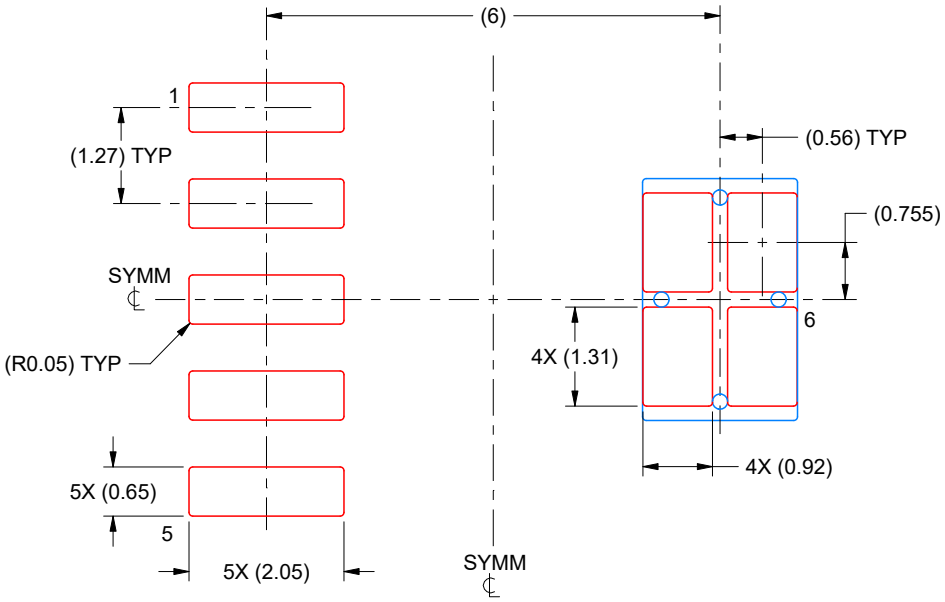


SOLDER MASK DETAILS

4214845/C 11/2021

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

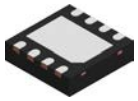
DRB 8 VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

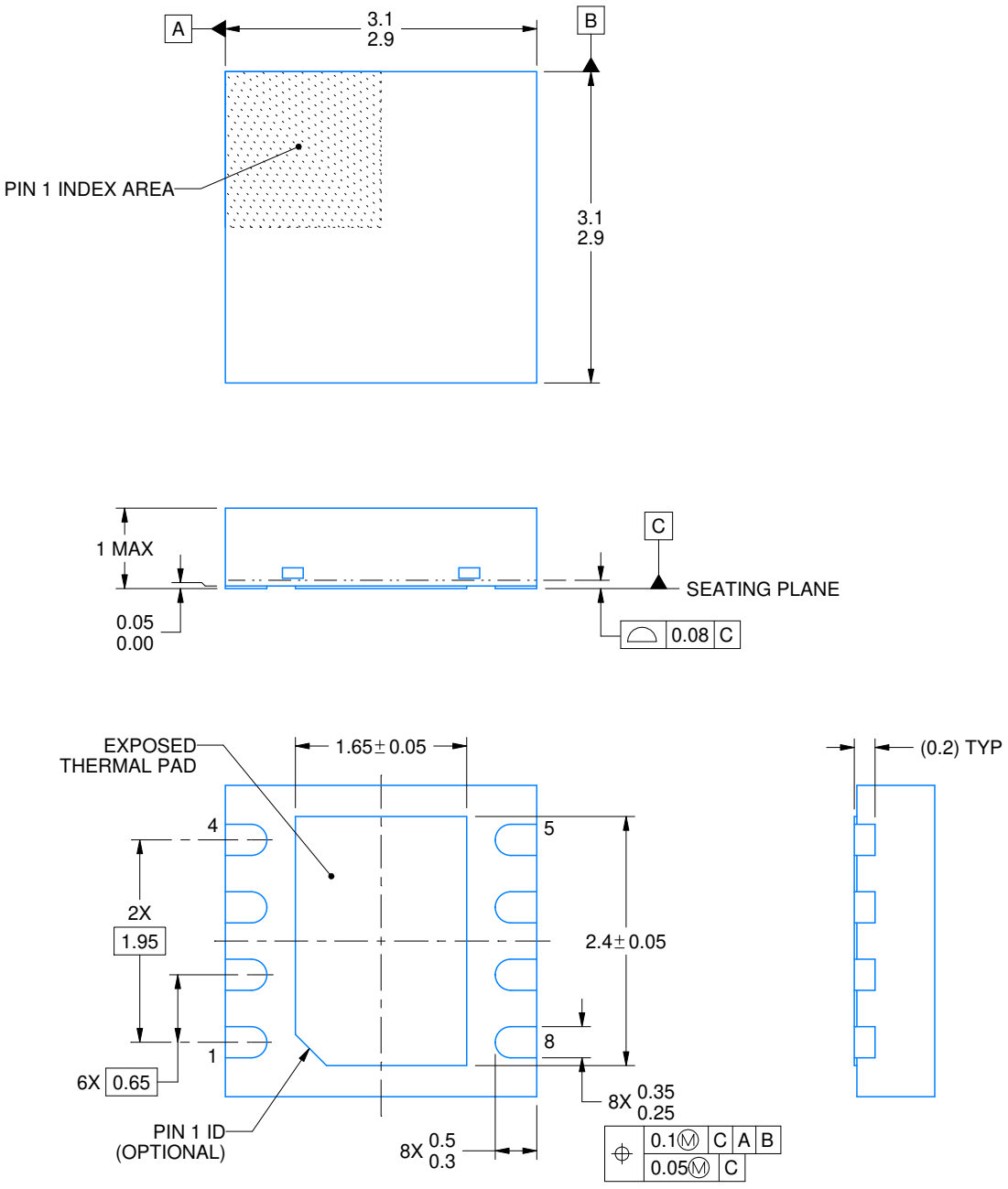
DRB0008B



PACKAGE OUTLINE

VSON - 1 mm max height

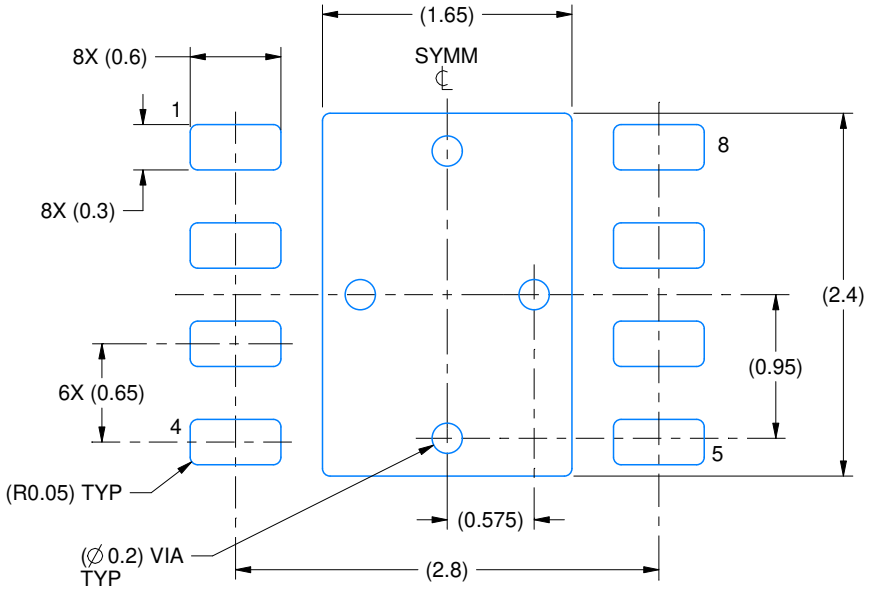
PLASTIC SMALL OUTLINE - NO LEAD



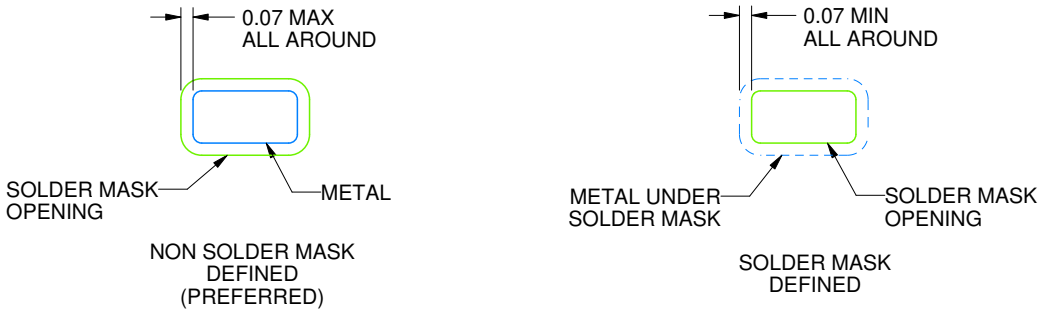
4218876/A 12/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

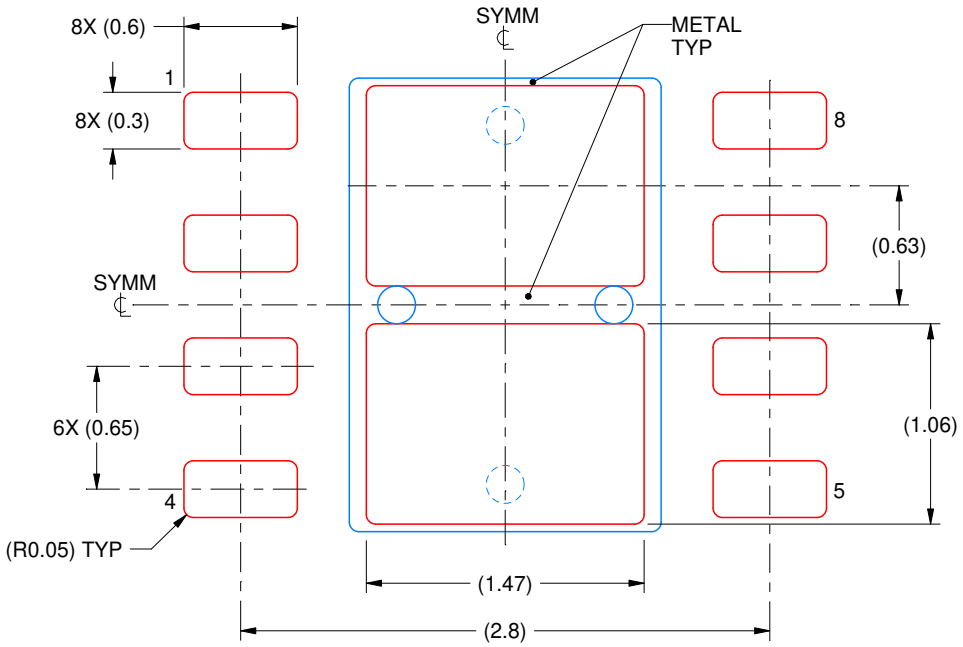


SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

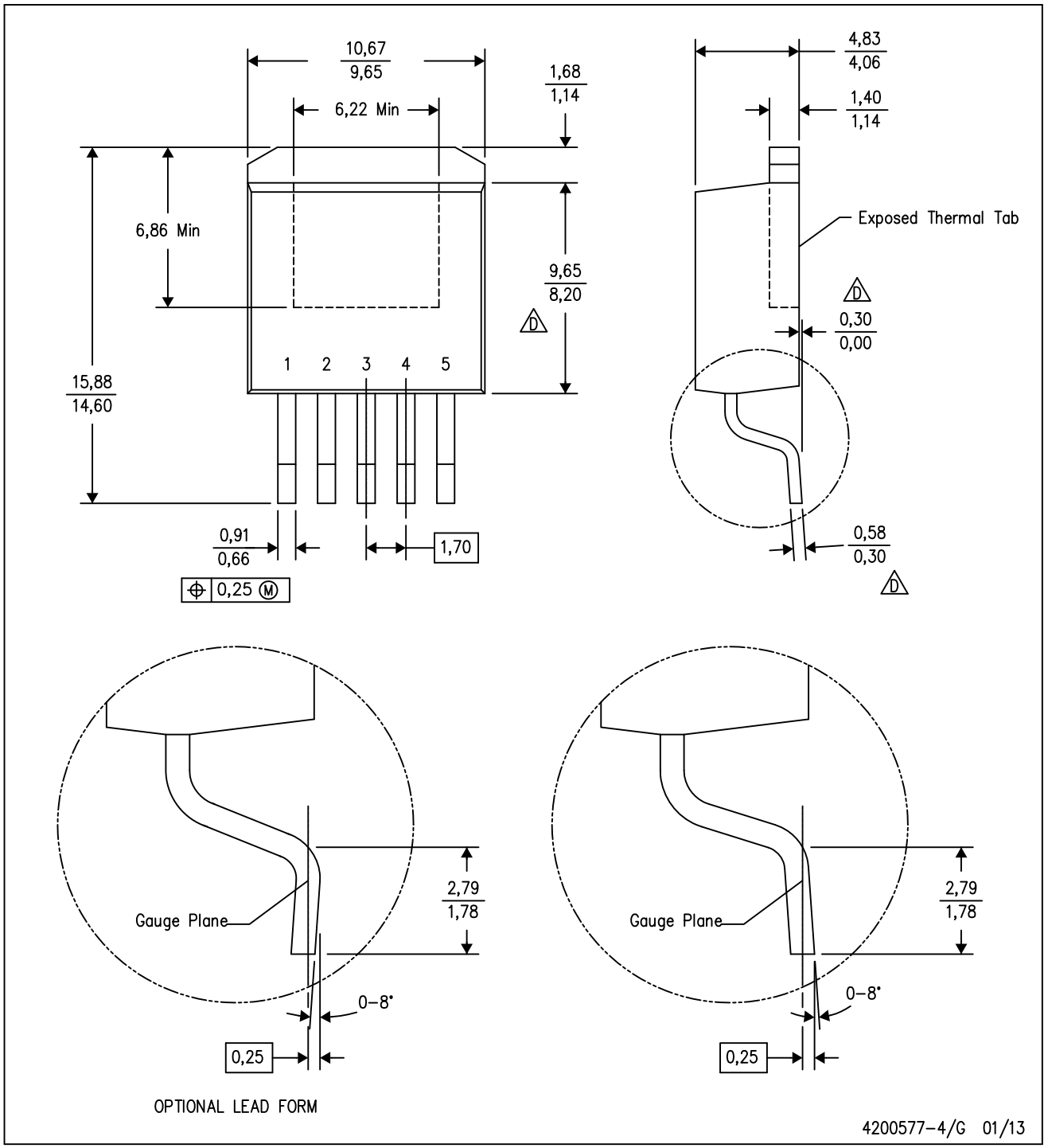
EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

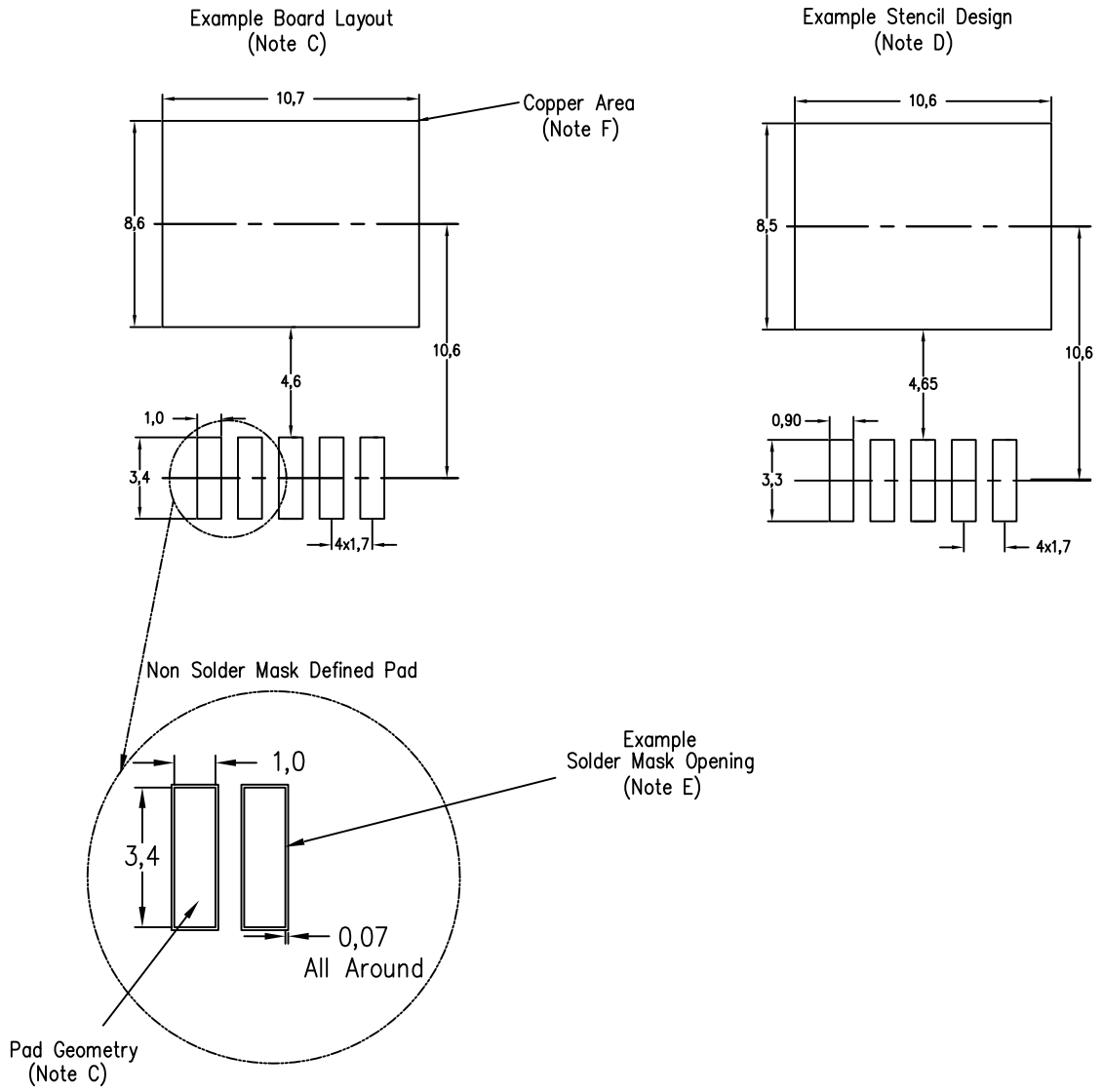
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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