User's Guide

TPS568215 SWIFT™ Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPS568215EVM-762 evaluation module (PWR762) as well as for the TPS568215 dc/dc converter. Also included are the performance specifications, board layouts, schematic, and the bill of materials for the TPS568215EVM-762.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

1.1 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the TPS568215EVM-762. Observe all safety precautions.

Warning The TPS568215EVM-762 circuit module may become hot during operation due to dissipation of heat. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory.

Caution Do not leave the EVM powered when unattended.

WARNING

The circuit module has signal traces, components, and component leads on the bottom of the board. This may result in exposed voltages, hot surfaces or sharp edges. Do not reach under the board during operation.

CAUTION

The circuit module may be damaged by over temperature. To avoid damage, monitor the temperature during evaluation and provide cooling, as needed, for your system environment.

CAUTION

Some power supplies can be damaged by application of external voltages. If using more than 1 power supply, check your equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to your equipment.

CAUTION

The communication interface is not isolated on the EVM. Be sure no ground potential exists between the computer and the EVM. Also be aware that the computer is referenced to the Battery- potential of the EVM.

1.2 Background

The TPS568215 dc/dc converter is a synchronous buck converter designed to provide up to a 8-A output. The input (V_{IN}) is rated for 4.5 V to 17 V. The TPS568215 uses a proprietary DCAP3 Control mode and a MODE pin is used to select output current limit, switching frequency, and *Forced Continuous Conduction Mode* (FCCM)/*Discontinuous Conduction Mode* (DCM) operation. Rated input voltage and output current range for the evaluation module are given in Table 1-1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS568215 regulator. The MODE pin is configured for 1.2-MHz switching frequency, 8-A and DCM operation. The high-side and low-side MOSFETs are incorporated inside the TPS568215 package along with the gate-drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS568215 to achieve high efficiencies and helps keep the junction temperature low at high output currents. An external divider allows for an adjustable output voltage. Additionally, the TPS568215 provides adjustable slow start and undervoltage lockout inputs and a power good output.

Table 1-1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS568215EVM-762	V_{IN} = 4.5 V to 17 V	0 A to 8 A

1.3 Performance Specification Summary

A summary of the TPS568215EVM-762 performance specifications is provided in Table 1-2. Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 1.2 V, unless otherwise specified. The TPS568215EVM-762 is designed and tested for V_{IN} = 4.5 V to 17 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 1-2. TPS568215EVM-762 Performance Specification Summary

Specification	Test Conditions		MIN	TYP	MAX	Unit
V_{IN} voltage range			4.5	12	17	V
V_{IN} start voltage				Internal UVLO		V
V_{IN} stop voltage				Internal UVLO		V
Output voltage setpoint				1.2		V
Output current range	V_{IN} = 4.5 V to 14 V		0		8	A
Line regulation	I_O = 4 A, V_{IN} = 4.5 V to 17 V			–0.02%, +0.08%		
Load regulation	V_{IN} = 12 V, I_O = 0 A to 8 A			–0.02%, +0.15%		
Load transient response	I_O = 2 A to 6 A	Voltage change		–25		mV
		Recovery time		50		µs
	I_O = 6 A to 2 A	Voltage change		25		mV
		Recovery time		50		µs
Loop bandwidth	V_{IN} = 12 V, I_O = 4 A			170		kHz
Phase margin	V_{IN} = 12 V , I_O = 4 A			70		degree
Input ripple voltage	I_O = 8 A			80		mVPP
Output ripple voltage	I_O = 8 A			10		mVPP
Output rise time				6		ms
Operating frequency				1.2		MHz
Maximum efficiency	TPS568215EVM-762, V_{IN} = 5 V, I_O = 2.4 A			90.47%		

1.4 Modifications

These evaluation modules are designed to provide access to the features of the TPS568215. Some modifications can be made to this module.

1.4.1 Output Voltage Setpoint

The output voltage is set by the resistor divider network of R7 ($R_{(TOP)}$) and R9 ($R_{(BOT)}$). R9 is fixed at 10.0 kΩ. To change the output voltage of the EVM, it is necessary to change the value of resistor R7. Changing the value of R9 can change the output voltage above the 0.6-V reference voltage V_{REF}. The value of R7 for a specific output voltage can be calculated using Equation 1.

$$R_{(TOP)} = \frac{R_{(BOT)} \times (V_{OUT} - V_{REF})}{V_{REF}} \quad (1)$$

1.4.2 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using R1 ($R_{EN(TOP)}$) and R2 ($R_{EN(BOT)}$). R1 and R2 are not populated on the EVM, which uses the internal UVLO default settings. See the TPS568215 datasheet (SLVSDI8) for detailed instructions for setting the external UVLO.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS568215EVM-762 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input/Output Connections

The TPS568215EVM-762 is provided with input/output connectors and test points as shown in Table 2-1. A power supply capable of supplying greater than 4 A must be connected to J1 through a pair of 20-AWG wires or better. The load must be connected to J2 through a pair of 20-AWG wires or better. The maximum load current capability is 8 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP9 is used to monitor the output voltage with TP10 as the ground reference.

Table 2-1. EVM Connectors and Test Points

Reference Designator	Function
J1	VIN input voltage connector. (See Table 1-1 for V_{IN} range)
J2	1.2 V at 8 A maximum
J3	2-pin header for enable. Connect EN to ground to disable, open to enable V_{OUT}.
TP1	VIN test point
TP2	GND test point at VIN connector
TP3	Slow Start (SS) test point
TP4	PGOOD test point
TP5	VREG5 test point
TP6	AGND test point
TP7	SW node test point
TP8	Test point between voltage divider network and output. Used for loop response measurements
TP9	VOUT test point
TP10	GND test point

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 2.4 A and then decreases as the load current increases toward full load. Figure 2-1 shows the efficiency for the TPS568215EVM-762 at an ambient temperature of 25°C.

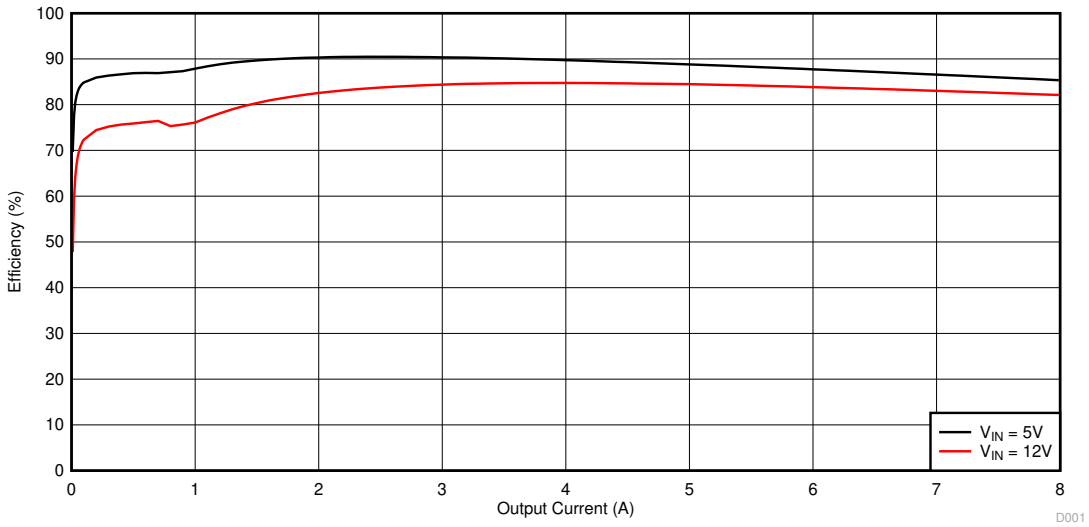

Figure 2-1. TPS568215EVM-762 Efficiency

Figure 2-2 shows the efficiency for the TPS568215EVM-762 using a semi-log scale to more easily show efficiency at lower output currents. The ambient temperature is 25°C.

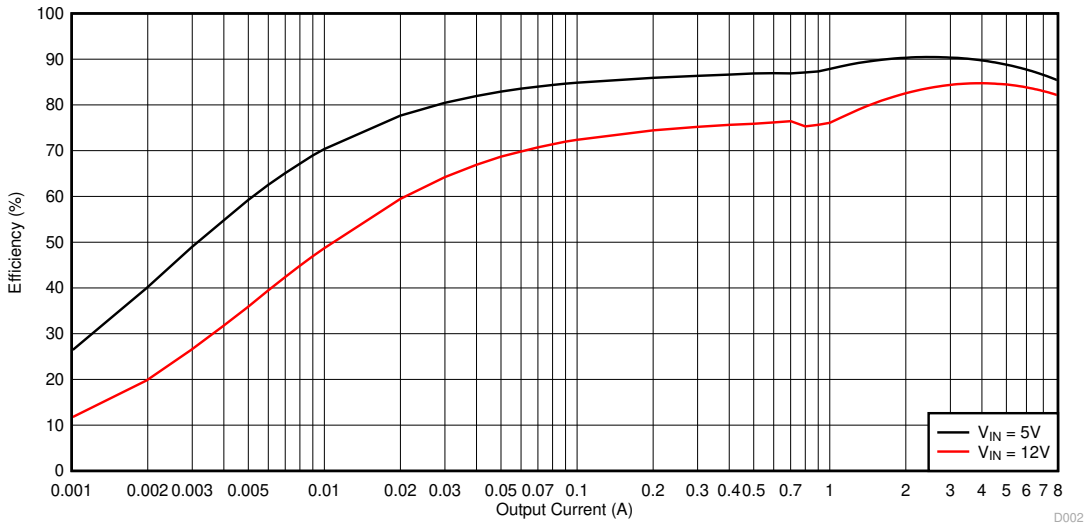

Figure 2-2. TPS568215EVM-762 Low Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

Figure 2-3 and Figure 2-4 show the load regulation for the TPS568215EVM-762.

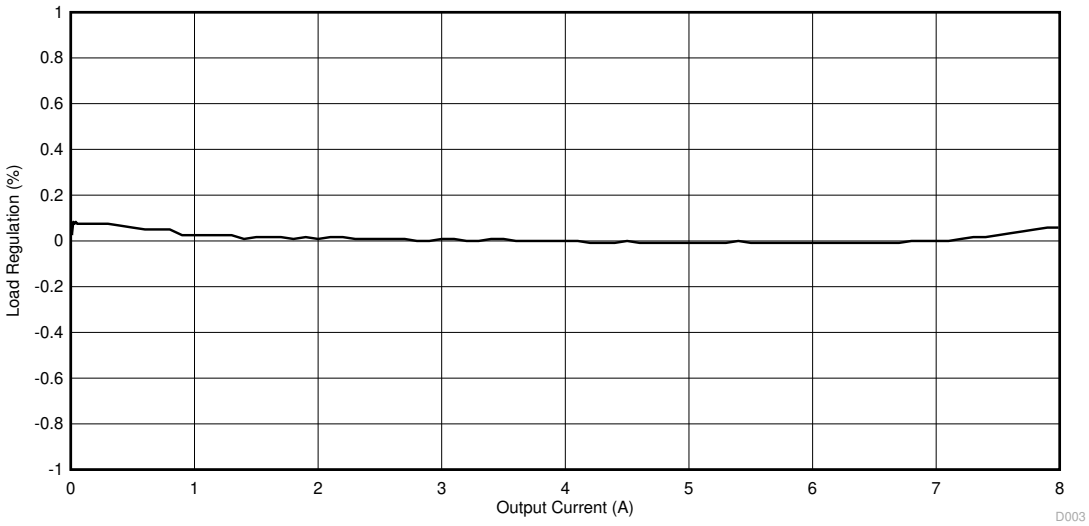

Figure 2-3. TPS568215EVM-762 Load Regulation, V_{IN} = 5 V

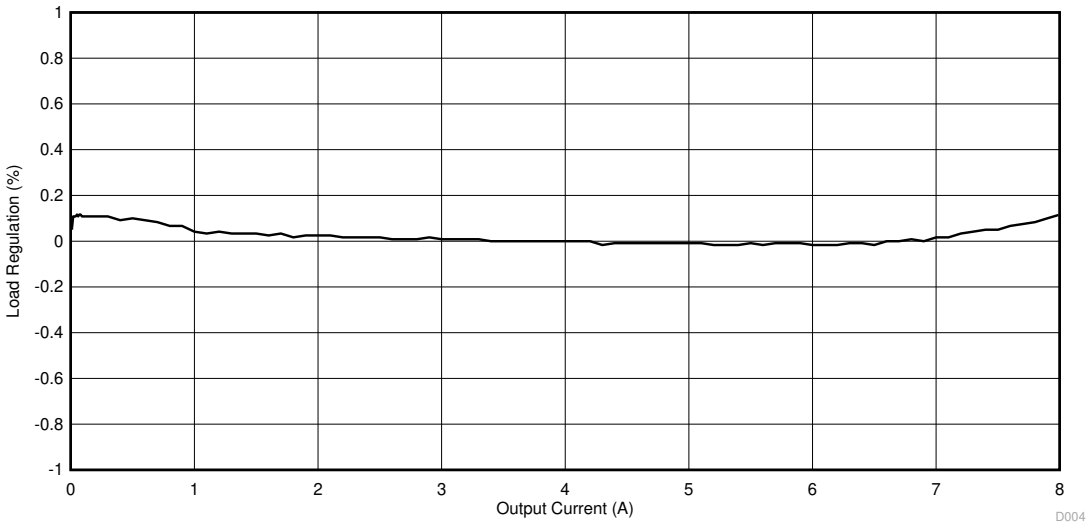

Figure 2-4. TPS568215EVM-762 Load Regulation, V_{IN} = 12 V

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

Figure 2-5 shows the line regulation for the TPS568215EVM-762.

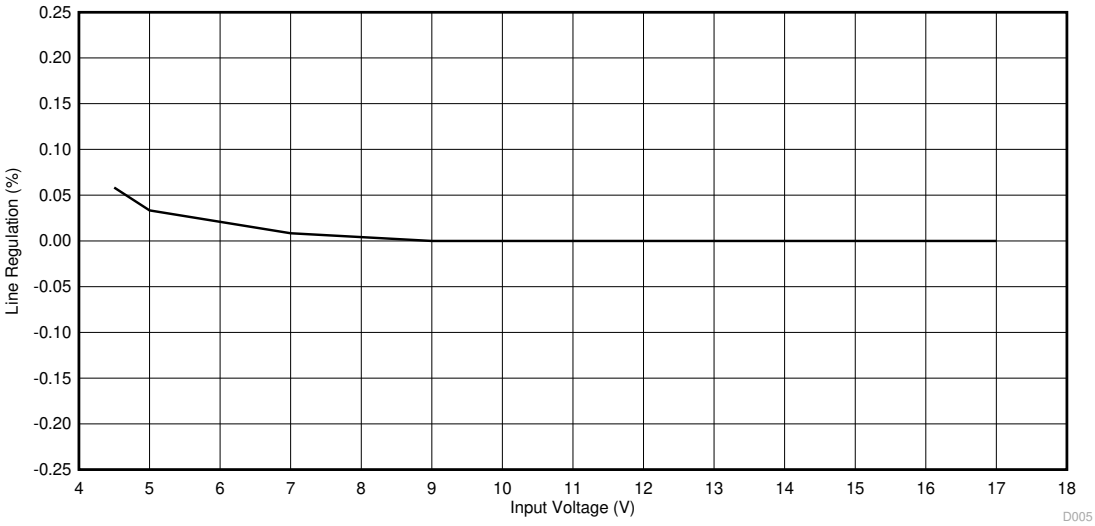

Figure 2-5. TPS568215EVM-762 Line Regulation

2.5 Load Transients

Figure 2-6 shows the TPS568215EVM-762 response to load transients. The current step is from 2 A to 6 A. The current step slew rate is 500 mA/µs. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output. The transient waveform is measured using the on-board fast transient circuit.

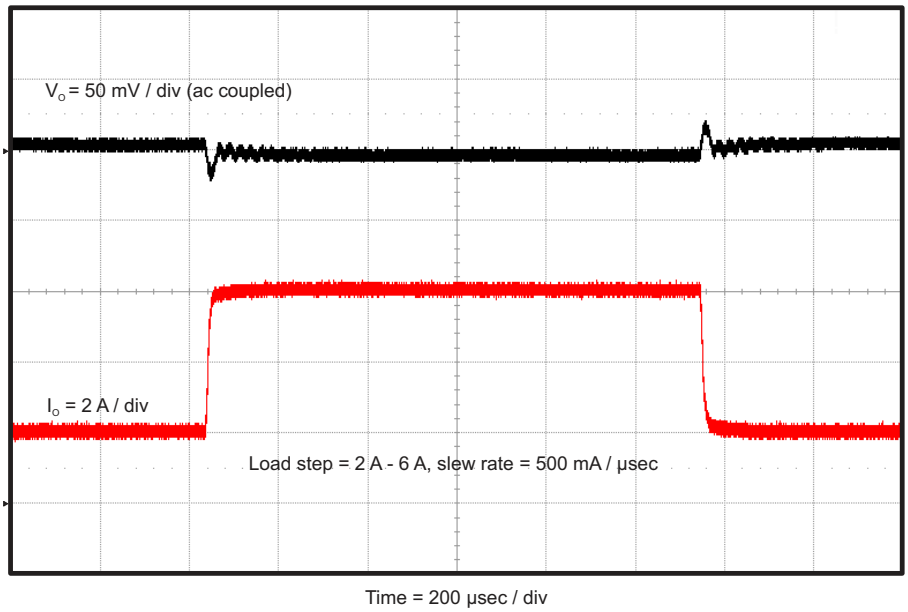

Figure 2-6. TPS568215EVM-762 Transient Response

2.6 Loop Characteristics

Figure 2-7 shows the TPS568215EVM-762 loop-response characteristics. Gain and phase plots are shown for V_{IN} voltage of 12 V. Load current for the measurement is 4 A.

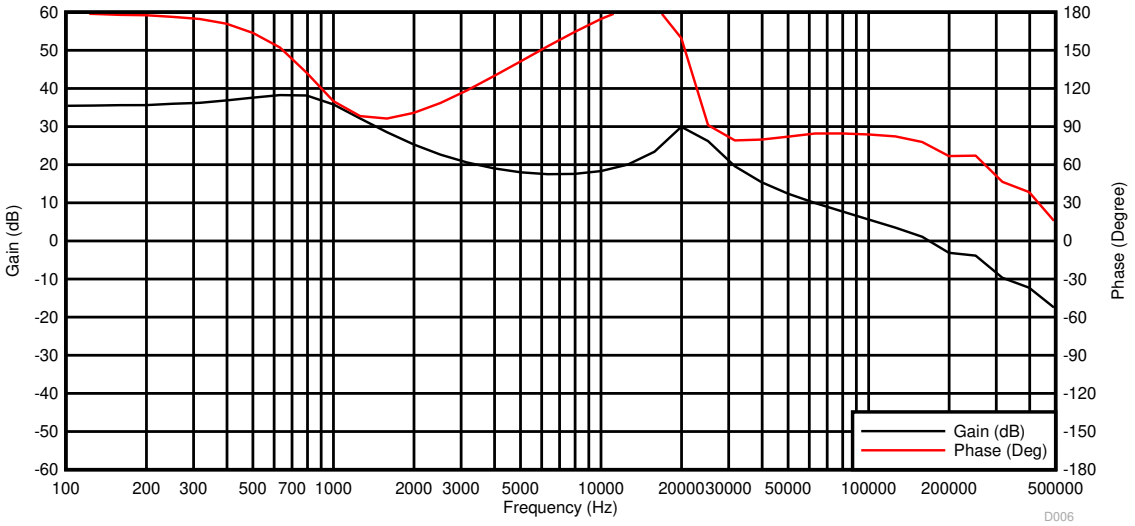

Figure 2-7. TPS568215EVM-762 Loop Response

2.7 Output Voltage Ripple

Figure 2-8, Figure 2-9, and Figure 2-10 show the TPS568215EVM-762 output voltage ripple. The load currents are 10 mA, 700 mA, and 8 A. V_{IN} = 12 V. The ripple voltage is measured directly across TP9 and TP10.

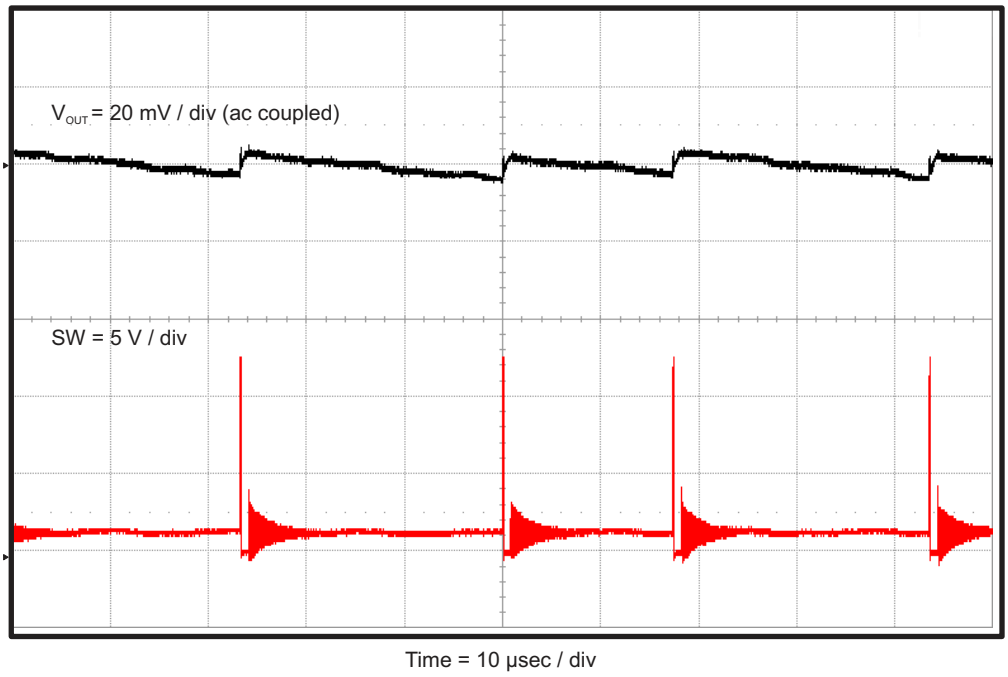

Figure 2-8. TPS568215EVM-762 Output Ripple, 10-mA Load

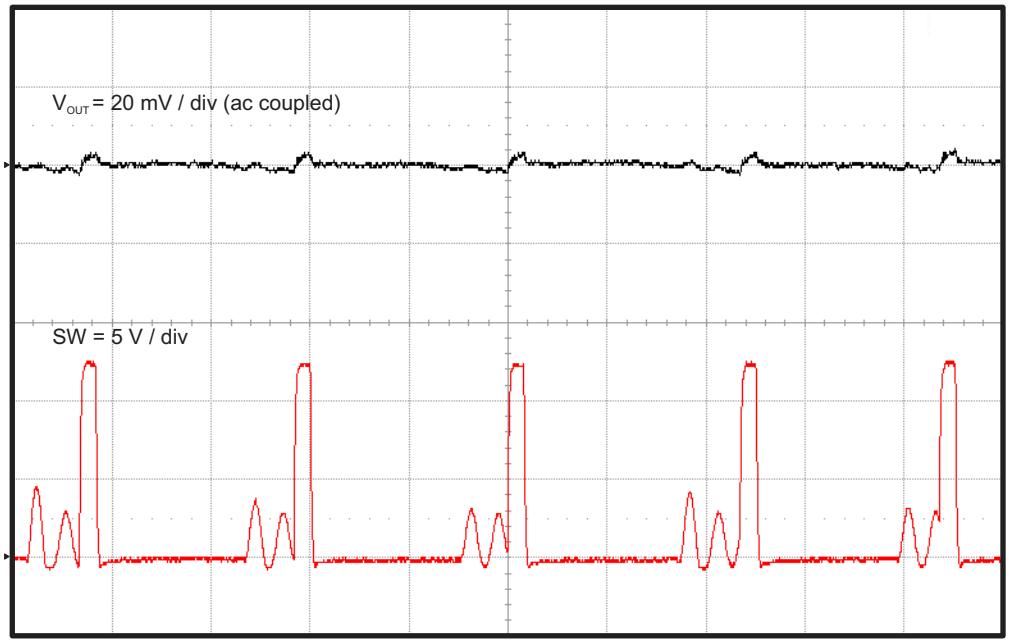

Figure 2-9. TPS568215EVM-762 Output Ripple, 700-mA Load

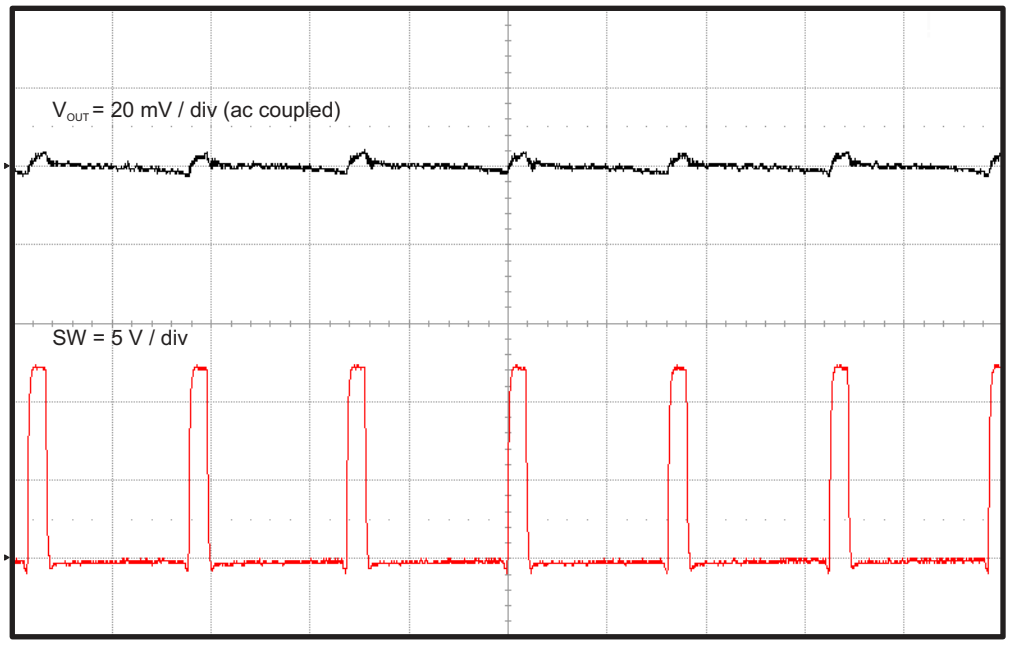

Figure 2-10. TPS568215EVM-762 Output Ripple, 8-A Load

2.8 Input Voltage Ripple

Figure 2-11, Figure 2-12, and Figure 2-13 show the TPS568215EVM-762 input voltage ripple. The load currents are 10 mA, 700 mA and 8 A. V_{IN} = 12 V. The ripple voltage is measured directly across TP1 and TP2.

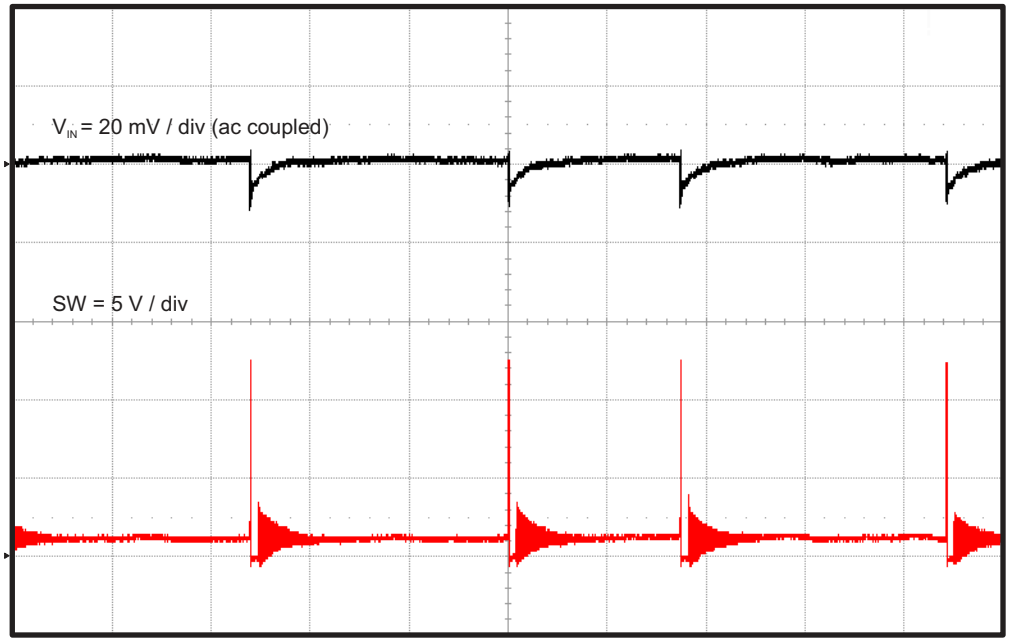

Figure 2-11. TPS568215EVM-762 Input Ripple, 10-mA Load

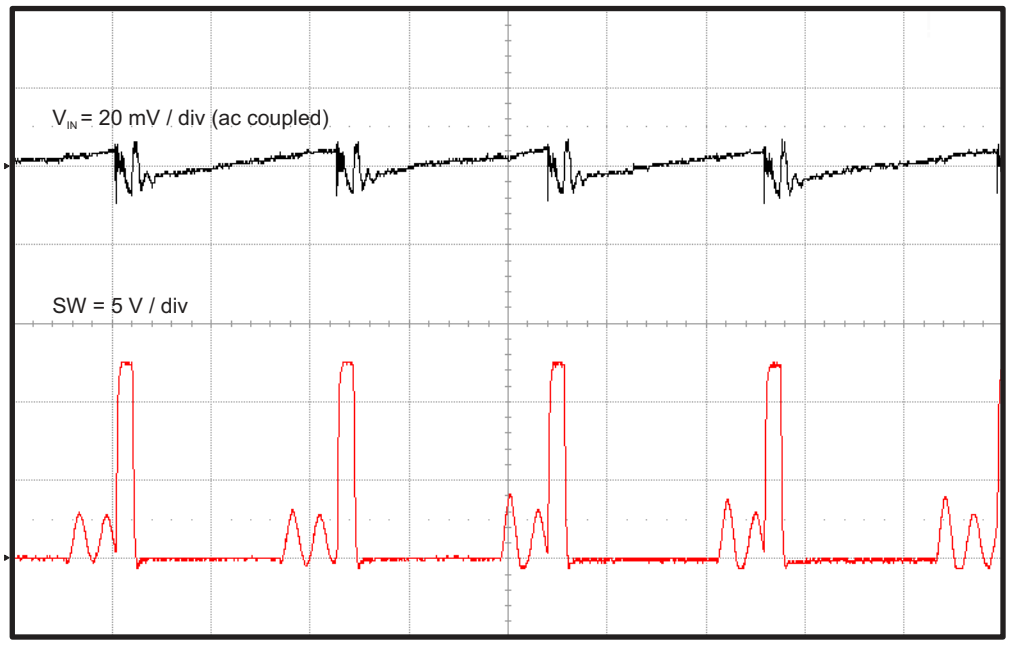

Figure 2-12. TPS568215EVM-762 Input Ripple, 700-mA Load

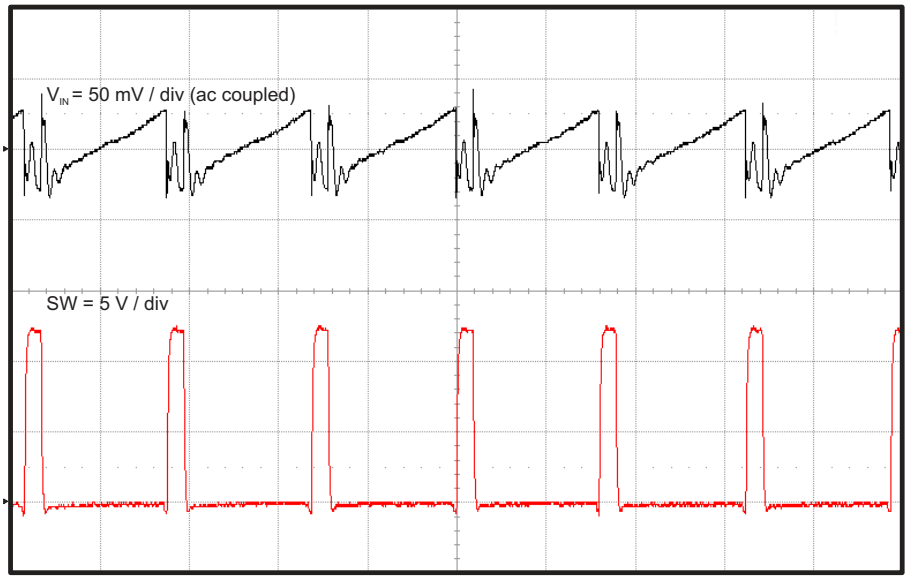

Figure 2-13. TPS568215EVM-762 Input Ripple, 8-A Load

2.9 Powering Up

Figure 2-14 and Figure 2-15 show the start-up waveforms for the TPS568215EVM-762. In Figure 2-14, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold. In Figure 2-15, the input voltage is initially applied and the output is inhibited by using a jumper at J3 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally-set value of 1.2 V. The input voltage for these plots is 12 V and the load is 1 Ω.

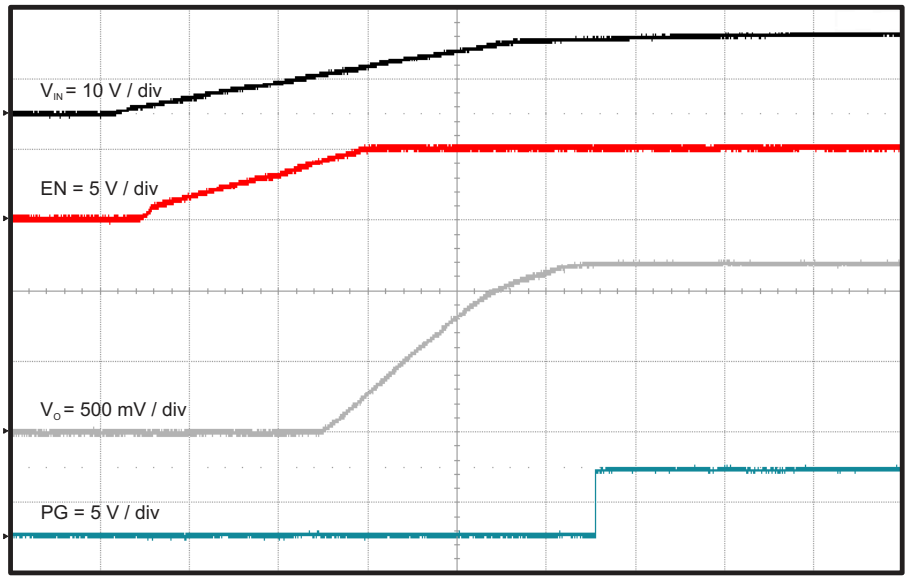

Figure 2-14. TPS568215EVM-762 Start-Up Relative to V_{IN}

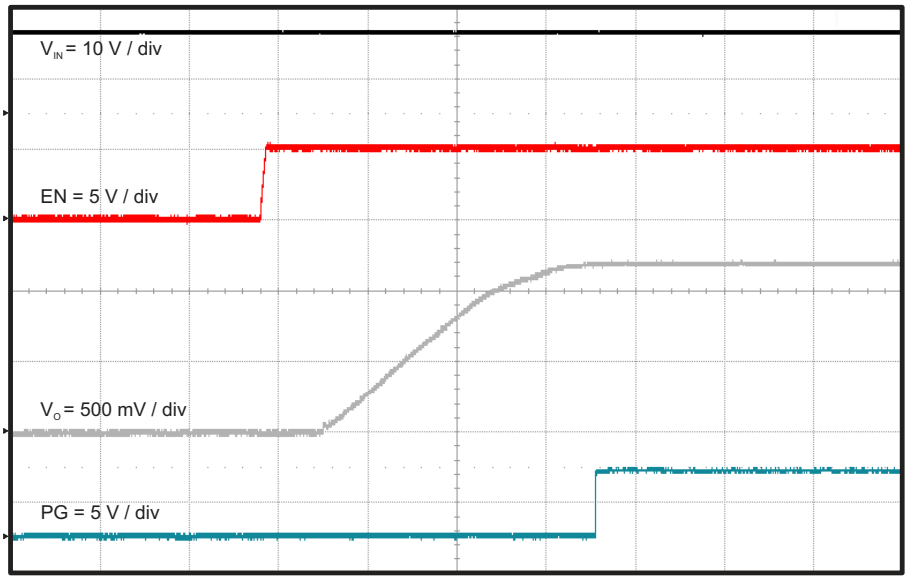

Figure 2-15. TPS568215EVM-762 Start-Up Relative to Enable

2.10 Powering Down

Figure 2-16 and Figure 2-17 show the shutdown waveforms for the TPS568215EVM-762. The input voltage for these plots is 12 V and the load is 1 Ω.

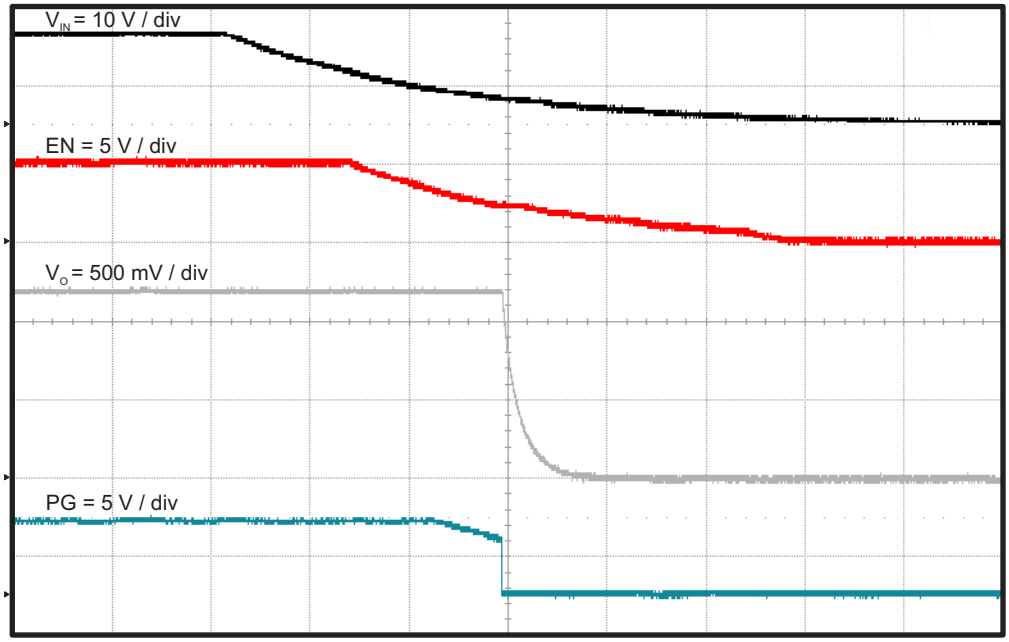

Figure 2-16. Shutdown Relative to V_{IN}

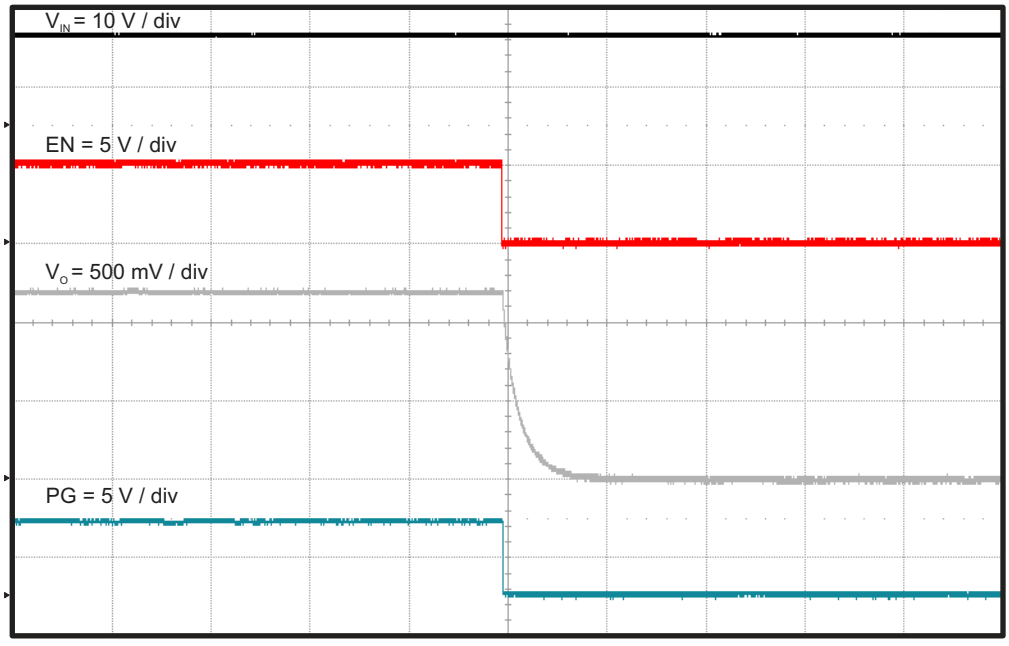

Figure 2-17. Shutdown Relative to Enable

2.11 Thermal Image

The thermal image in Figure 2-18 shows the EVM with 12-V input and full load of 8 A.

Figure 2-18. Thermal Image

3 Board Layout

This section provides a description of the TPS568215EVM-762 board layout and layer illustrations.

3.1 Layout

The board layout for the TPS568215EVM-762 is shown in Figure 3-1 through Figure 3-5. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper.

The top layer contains the main power traces for VIN, VOUT, and SW. Also on the top layer are connections for the remaining pins of the TPS568215 and the majority of the signal traces. There is a large area filled with ground. The internal layer-1 is dedicated ground plane with an island for quiet analog ground that is connected to the main power ground plane at a single point. The internal layer-2 contains an additional large ground copper area as well as an additional VIN and VOUT copper fill. The bottom layer is another ground plane with two additional traces for the output voltage feedback and BST capacitor connection. The top-side ground traces are connected to the bottom and internal ground planes with multiple vias placed around the board.

The input decoupling capacitors and bootstrap capacitor are all located as close to the IC as possible. Additionally, the voltage setpoint resistor divider components are kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace at the TP9 test point. For the TPS568215, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply. Critical analog circuits such as the voltage set point divider, EN resistor, SS capacitor, MODE resistor, and AGND pin are terminated to quiet analog ground island on the internal layer-1.

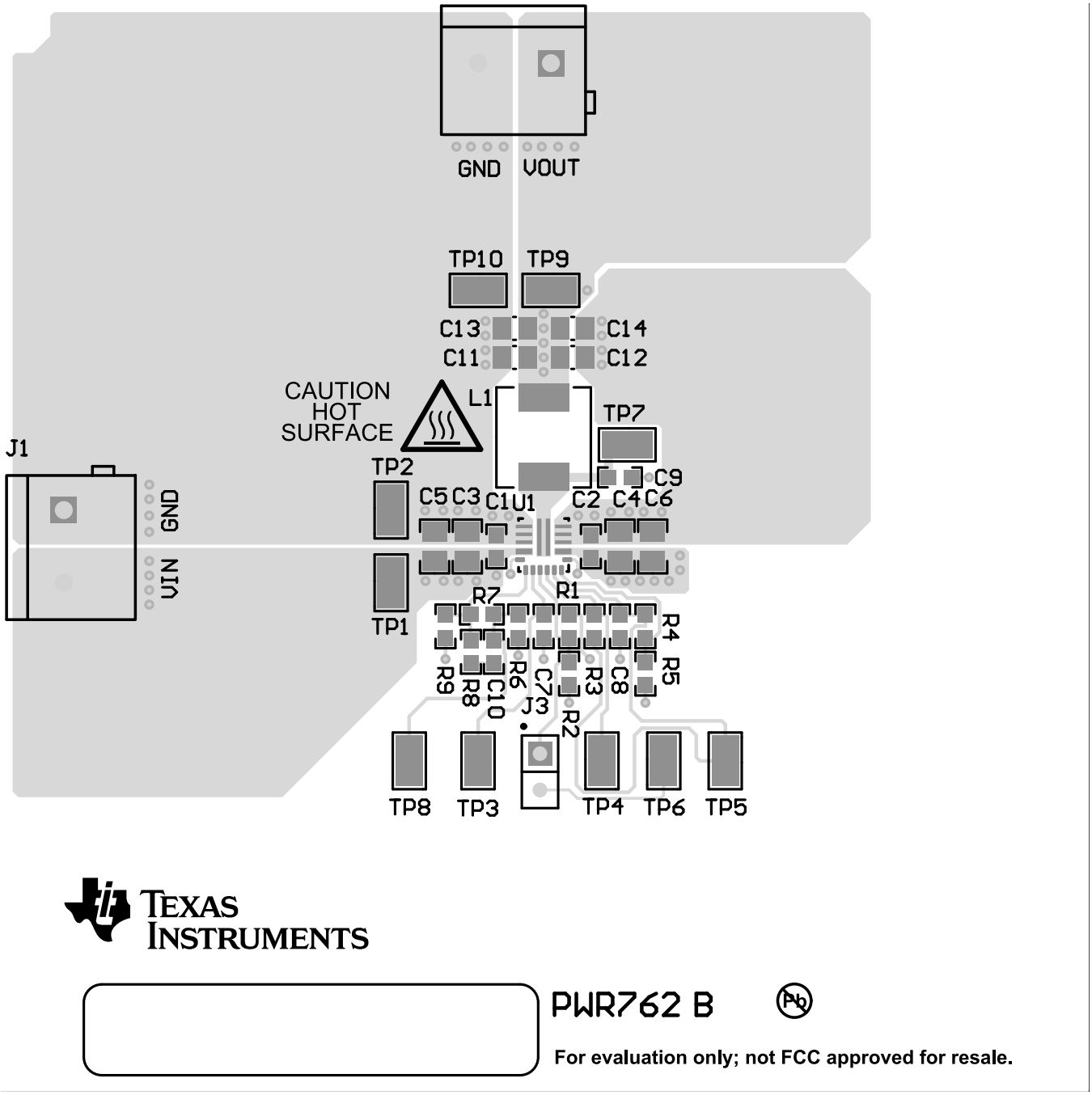

Figure 3-1. TPS568215EVM-762 Top-Side Assembly

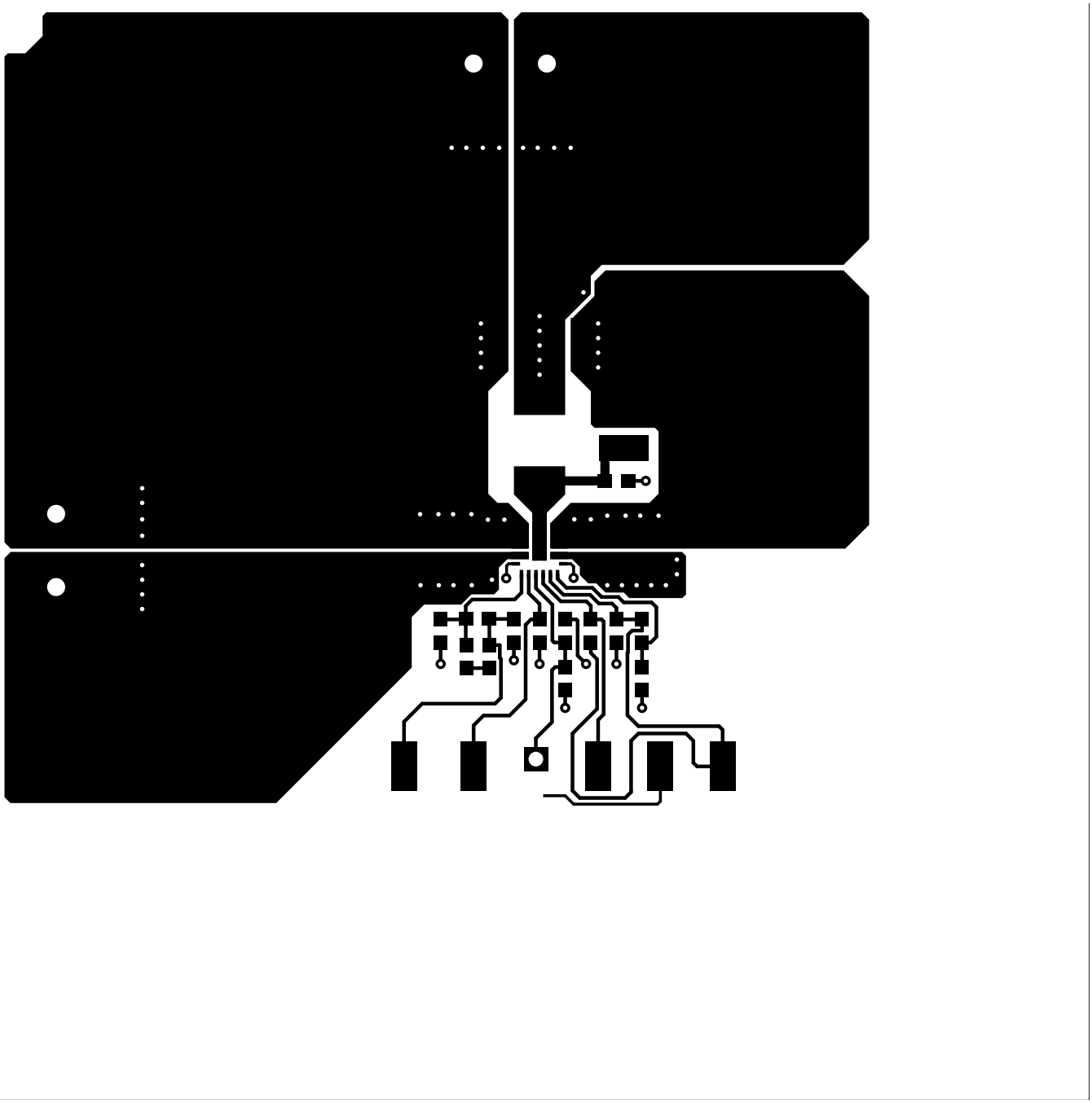

Figure 3-2. TPS568215EVM-762 Top-Side Layout

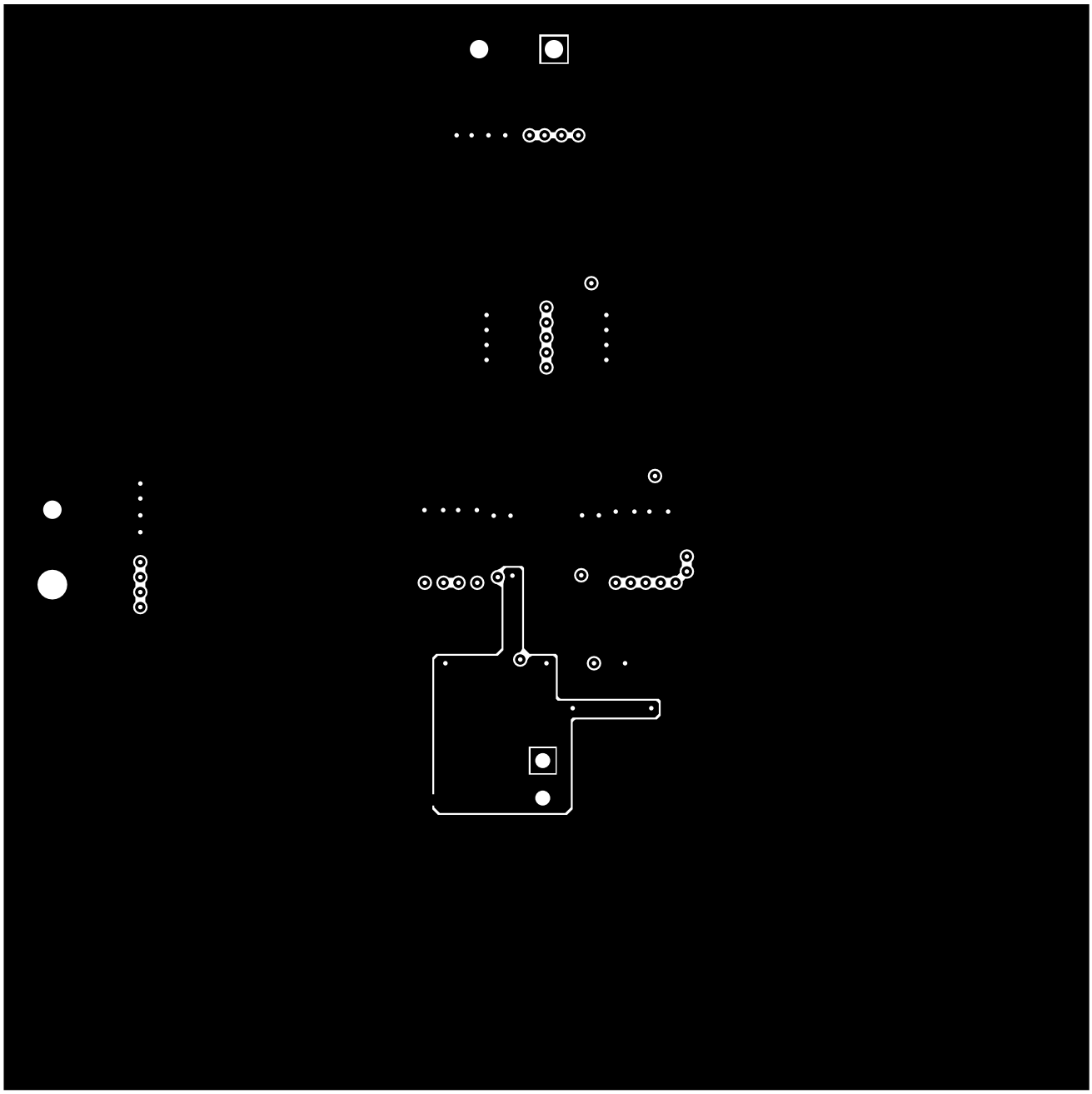

Figure 3-3. TPS568215EVM-762 Internal Layer-1 Layout

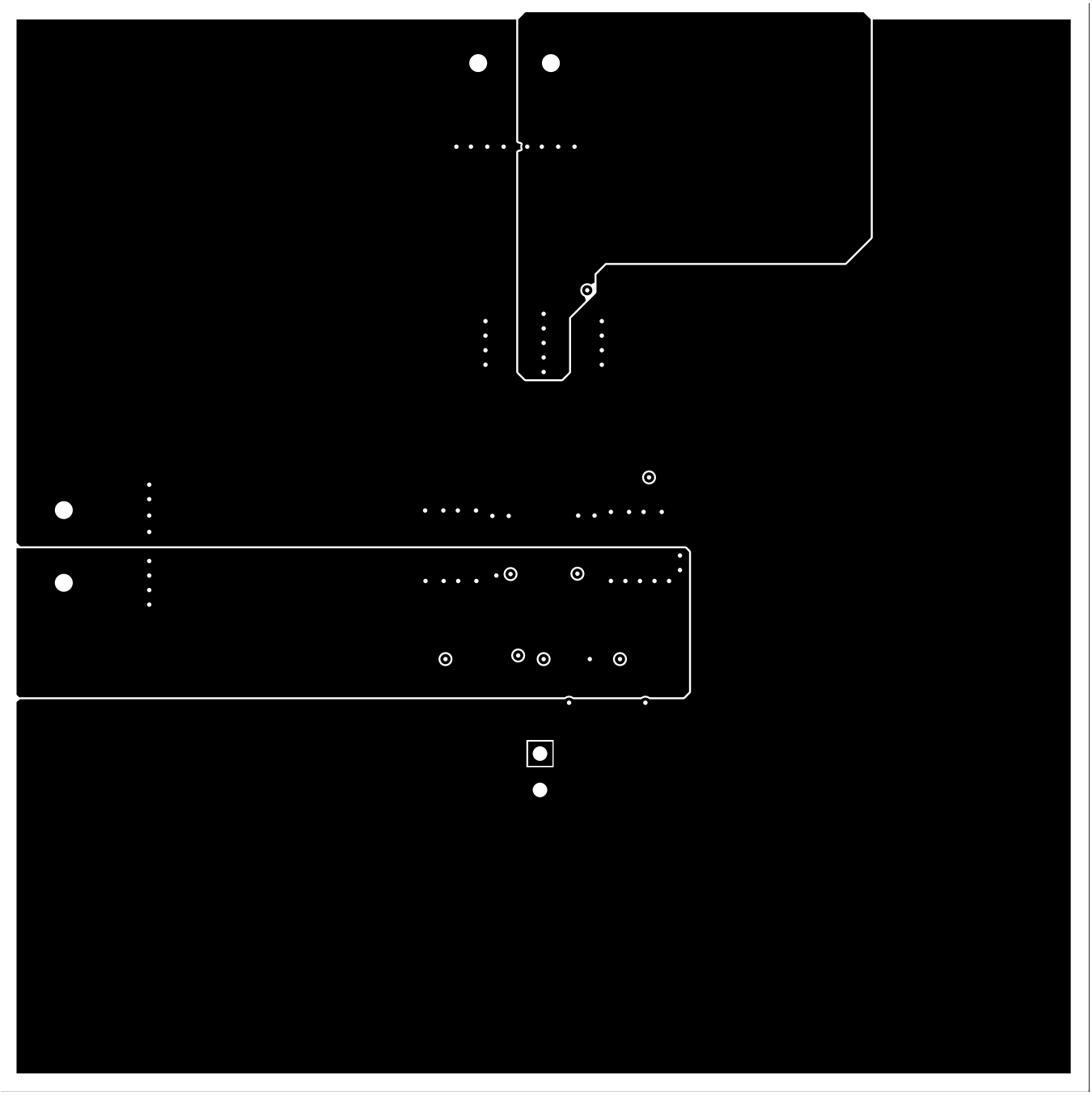

Figure 3-4. TPS568215EVM-762 Internal Layer-2 Layout

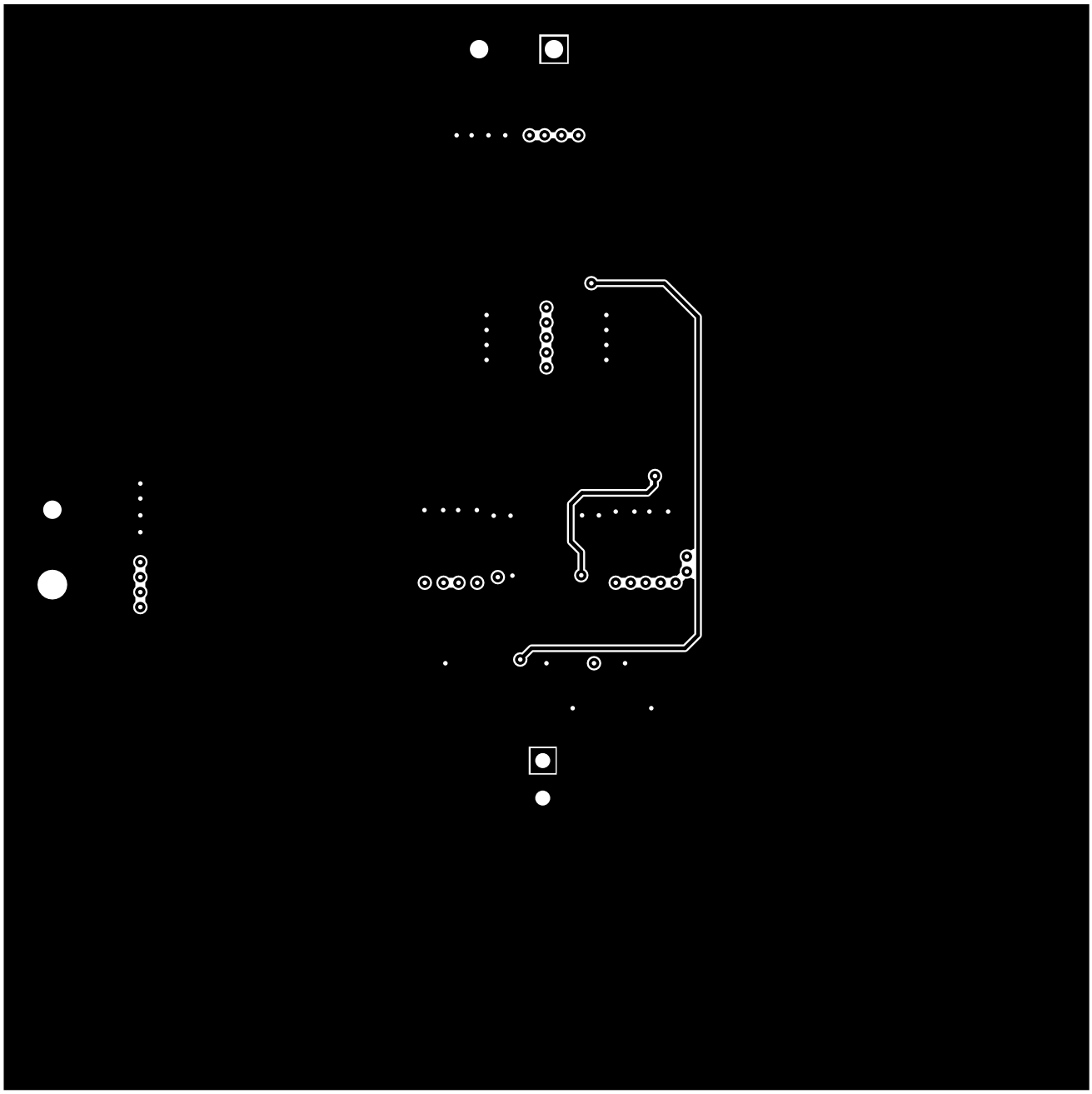

Figure 3-5. TPS568215EVM-762 Bottom-Side Layout

4 Schematic and Bill of Materials

This section presents the TPS568215EVM-762 schematic and bill of materials.

4.1 Schematic

Figure 4-1 is the schematic for the TPS568215EVM-762.

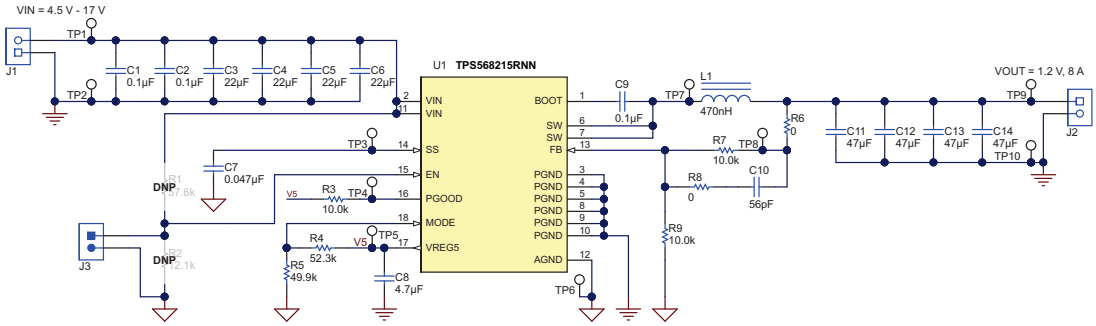

Figure 4-1. TPS568215EVM-762 Schematic

4.2 Bill of Materials

Table 4-1 presents the bill of materials for the TPS568215EVM-762.

Table 4-1. TPS568215EVM-762 Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		PWR762	Any
C1, C2, C9	3	0.1uF	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X7R, 0603	0603	GRM188R71E104KA01D	Murata
C3, C4, C5, C6	4	22uF	CAP, CERM, 22 µF, 35 V, +/- 20%, X5R, 0805	0805	C2012X5R1V226M125AC	TDK
C7	1	0.047uF	CAP, CERM, 0.047 µF, 50 V, +/- 10%, X7R, 0603	0603	GRM188R71H473KA61D	Murata
C8	1	4.7uF	CAP, CERM, 4.7 µF, 10 V, +/- 20%, X5R, 0603	0603	GRM188R61A475ME15	Murata
C10	1	56pF	CAP, CERM, 56 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H560JA01D	Murata
C11, C12, C13, C14	4	47uF	CAP, CERM, 47 µF, 10 V, +/- 20%, X5R, 0805	0805	GRM21BR61A476ME15	Murata
J1, J2	2		TERMINAL BLOCK 5.08MM VERT 2POS, TH		ED120/2DS	On-Shore Technology
J3	1		Header, 100mil, 2x1, Gold, TH		HTSW-102-07-G-S	Samtec
L1	1	470nH	Inductor, Shielded Drum Core, Powdered Iron, 470 nH, 17.5 A, 0.004 ohm, SMD	IHLP-2525CZ	IHLP2525CZERR47M01	Vishay-Dale
LBL1	1		Thermal Transfer Printable Labels, 1.250" W x 0.250" H - 10,000 per roll	PCB Label 1.25"H x 0.250"W	THT-13-457-10	Brady
R3, R7, R9	3	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R4	1	52.3k	RES, 52.3 k, 1%, 0.1 W, 0603	0603	CRCW060352K3FKEA	Vishay-Dale
R5	1	49.9k	RES, 49.9 k, 1%, 0.1 W, 0603	0603	CRCW060349K9FKEA	Vishay-Dale
R6, R8	2	0	RES, 0, 5%, 0.1 W, 0603	0603	MCR03EZPJ000	Rohm
SH-J3	1	1x2	Shunt, 100mil, Gold plated, Black	Shunt	969102-0000-DA	3M
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10	10	SMT	Test Point, Miniature, SMT	Testpoint_Keystone_Miniature	5015	Keystone
U1	1		4.5V to 17V Input, 8A Synchronous Step-Down Converter, RNN0017A	RNN0017A	TPS568215RNN	Texas Instruments
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A
R1	0	57.6k	RES, 57.6 k, 1%, 0.1 W, 0603	0603	CRCW060357K6FKEA	Vishay-Dale
R2	0	12.1k	RES, 12.1 k, 1%, 0.1 W, 0603	0603	CRCW060312K1FKEA	Vishay-Dale

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2016) to Revision A (June 2021)	Page
• Updated user's guide title	2
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2

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