

9014

QUAD EXCLUSIVE-OR GATE

DESCRIPTION — The 9014 consists of four Exclusive-OR gates, useful in a large number of code conversion, parity generation/checking, and comparison applications. The Exclusive-OR gate produces an output when the inputs are complementary. Two gates have an additional inverted output which provides directly a compare capability. The Boolean expressions for the gates are: $Z = A\bar{B} + \bar{A}B$; $\bar{Z} = AB + \bar{A}\bar{B}$.

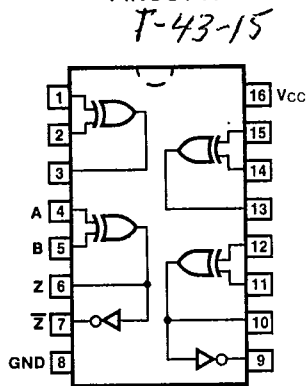
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0 V \pm 5\%$, $T_A = 0^\circ C$ to $+75^\circ C$	$V_{CC} = +5.0 V \pm 10\%$, $T_A = -55^\circ C$ to $+125^\circ C$	
Ceramic DIP (D)	A	9014DC	9014DM	6B
Flatpak (F)	A	9014FC	9014FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	9XXX Series HIGH/LOW
Inputs	2.25/1.5
Outputs Pins 3, 7, 9, 13	30/8.8 (33)/(8.5)
Pins 6, 10	28.5/7.9 (30)/(7.75)

CONNECTION DIAGRAM
PINOUT A



$V_{CC} = \text{Pin } 16$
 $GND = \text{Pin } 8$

TRUTH TABLE

INPUTS		OUTPUTS	
A	B	Z	\bar{Z}
L	L	L	H
L	H	H	L
H	L	H	L
H	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

DC AND AC CHARACTERISTICS OVER COMMERCIAL TEMPERATURE RANGE: $V_{CC} = +5.0 V \pm 5\%$

SYMBOL	PARAMETER	0°C		25°C		75°C		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
V_{IH}	Input HIGH Voltage	1.9		1.8		1.6		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage		0.85		0.85		0.85	V	Guaranteed Input LOW Threshold
V_{OL}	Output LOW Voltage		0.45		0.45		0.45	V	$V_{CC} = 5.25 V$, $I_{OL} = 16 mA$ $I_{OL} = 14.4 mA$ (Pins 6 & 10) Inputs = 5.25 V or 0 V per Truth Table

9XXX Series

7-43-15

DC AND AC CHARACTERISTICS OVER COMMERCIAL TEMPERATURE RANGE: $V_{CC} = +5.0\text{ V} \pm 5\%$											
SYMBOL	PARAMETER	0°C		25°C		75°C		UNITS	CONDITIONS		
		Min	Max	Min	Max	Min	Max				
V_{OL}	Output LOW Voltage	0.45		0.45		0.45		V	$V_{CC} = 4.75\text{ V}$, $I_{OL} = 14.1\text{ mA}$ $I_{OL} = 12.7\text{ mA}$ (Pins 6 & 10) Inputs = 5.25 V or 0 V per Truth Table		
I_{IL}	Input LOW Current	-2.4		-2.4		-2.4		mA	$V_{CC} = 5.25\text{ V}$, $V_{IN} = .45\text{ V}$ Other Inputs = 5.25 V		
		-2.1		-2.1		-2.1			$V_{CC} = 4.75\text{ V}$, $V_{IN} = .45\text{ V}$ Other Inputs = 5.25 V		
I_{CC}	Power Supply Current, each gate	ON	4.5		4.5		4.5		mA	One Input = 5.5 V, One Input = Gnd	
		OFF	8.7		8.7		8.7		mA	Inputs = Gnd	
	Power Supply Current Per Inverter	ON	6.1		6.1		6.1		mA	Inputs = 5.5 V	
		OFF	1.7		1.7		1.7			Input Node HIGH	
$t_{PLH\ 1}$ $t_{PHL\ 1}$ $t_{PHH\ 1}$ $t_{PLL\ 1}$	Switching Tests			3.0	13			ns	$C_L = 15\text{ pF}$, $V_{IN1} = 5.0\text{ V}$ Fig. a, Fig. b		
$t_{PHH\ 2}$ $t_{PLL\ 2}$ $t_{PLH\ 2}$ $t_{PHL\ 2}$				7.0	17					ns	$C_L = 15\text{ pF}$, $V_{IN1} = 0\text{ V}$ Fig. a, Fig. c
		3.0	15								
		6.0	28								
		6.0	28								
				7.0	19						
				7.0	32						
				10	32						
				10	32						

DC AND AC CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE: $V_{CC} = +5.0\text{ V} \pm 10\%$

SYMBOL	PARAMETER	-55°C		25°C		125°C		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
V_{IH}	Input HIGH Voltage	2.0		1.7		1.4		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage	0.8		0.9		0.8		V	Guaranteed Input LOW Threshold
V_{OL}	Output LOW Voltage	0.4		0.4		0.4		V	$V_{CC} = 5.5\text{ V}$, $I_{OL} = 17.6\text{ mA}$ $I_{OL} = 16\text{ mA}$ (Pins 6 & 10) Inputs = 5.5 V or 0 V per Truth Table
		0.4		0.4		0.4			$V_{CC} = 4.5\text{ V}$, $I_{OL} = 13.6\text{ mA}$ $I_{OL} = 12.4\text{ mA}$ (Pins 6 & 10) Inputs = 5.5 V or 0 V per Truth Table

DC AND AC CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE: $V_{CC} = +5.0\text{ V} \pm 10\%$

SYMBOL	PARAMETER	-55°C		25°C		125°C		UNITS	CONDITIONS		
		Min	Max	Min	Max	Min	Max				
I_{IL}	Input LOW Current	-2.4		-2.4		-2.4		mA	$V_{CC} = 5.5\text{ V}$, $V_{IN} = 0.4\text{ V}$ Other Inputs = 5.5 V		
		-1.86		-1.86		-1.86			$V_{CC} = 4.5\text{ V}$, $V_{IN} = 0.4\text{ V}$ Other Inputs = 5.5 V		
I_{CC}	Power Supply Current, each gate	ON	4.2		4.2		4.2		mA	One Input = 5.5 V One Input = Gnd	
		OFF	8.1		8.1		8.1		mA	Inputs = Gnd	
	Power Supply Current Per Inverter	ON	5.5		5.5		5.5		mA	Input Node HIGH	
		OFF	1.6		1.6		1.6			Input Node LOW	
$t_{PLH 1}$ $t_{PHL 1}$ $t_{PLH 1}$ $t_{PLL 1}$	Switching Tests			3.0	10			ns	$C_L = 15\text{ pF}$, $V_{IN1} = 5.0\text{ V}$ Fig. a, Fig. b		
$t_{PHH 2}$ $t_{PLL 2}$ $t_{PLH 2}$ $t_{PHL 2}$				7.0	14					ns	$C_L = 15\text{ pF}$, $V_{IN1} = 0\text{ V}$ Fig. a, Fig. c
		3.0	12								
		6.0	22								

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SWITCHING TEST CIRCUIT

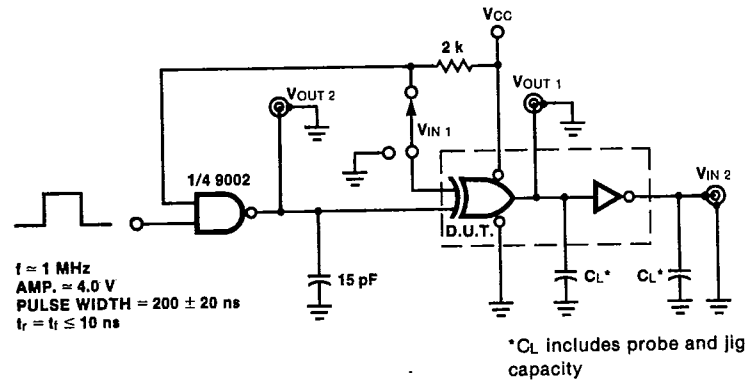


Fig. a

WAVEFORMS

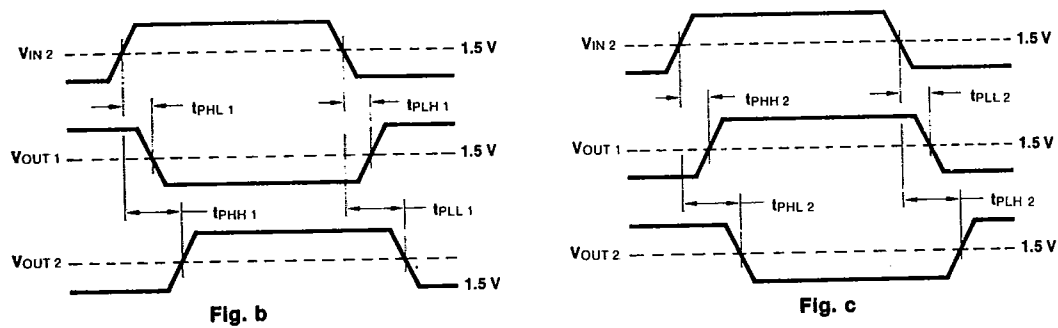


Fig. b

Fig. c