

Using the TPS40140EVM-002, A 20-A Dual-Output Synchronous Buck Converter

The TPS40140EVM-002 evaluation module (EVM) is a dual-output synchronous buck converter. The EVM delivers 3.3V at 20A and 1.5V at 20A. The module uses the TPS40140 dual, or 2-phase stackable synchronous buck controller.

Contents

1	Description.....	2
2	TPS40140EVM-002 Electrical Performance Specifications.....	3
3	Schematic	4
4	Test Set Up.....	5
5	TPS40140EVM-002 Typical Performance Data and Characteristic Curves.....	12
6	EVM Assembly Drawings and Layout	14
7	List of Materials.....	21

List of Figures

1	TPS40140EVM-002 Power Stage/Control Schematic	4
2	TPS40140EVM-002 Schematic.....	5
3	TPS40140EVM-002 Recommended Test Set-Up.....	8
4	Output Ripple Measurement	9
5	Default Configuration	10
6	Output Enable/Disable Configuration.....	10
7	Configure CH1 as Slave and CH2 as Independent Channel.....	10
8	Configure CH2 as Slave and CH1 as Independent Channel.....	11
9	Master and Slave Connection (this EVM is the slave)	11
10	TPS40140EVM-002 Efficiency	13
11	TPS40140EVM-002 Efficiency	13
12	TPS40140EVM-002 $V_{OUT1}=1.5V$ Line and Load Regulation	14
13	TPS40140EVM-002 $V_{OUT2}=3.3V$ Line and Load Regulation	14
14	TPS40140EVM-002 Component Placement (Viewed from Top)	15
15	TPS40140EVM-002 Silkscreen (Viewed from Top)	16
16	TPS40140EVM-002 Top Copper (Viewed from Top)	17
17	TPS40140EVM-002 Layer 2 Copper (X-Ray View from Top).....	18
18	TPS40140EVM-002 Layer 3 Copper (X-Ray View from Top).....	19
19	TPS40140EVM-002 Bottom Copper (X-Ray View from Top)	20

List of Tables

1	TPS40140EVM-002 Electrical and Performance Specifications	3
2	List of Test Points	12
3	TPS40140EVM-002 Bill of Materials	21

1 Description

TPS40140EVM-002 is designed to use a regulated 10.8V to 13.2V bus to produce two high-current, regulated outputs. Both outputs are capable of supplying up to 20A of load current. The TPS40140EVM-002 is design to demonstrate the TPS40140 in a typical regulated bus to low-voltage application while providing a number of test points to evaluate the performance of the TPS40140 in a given application.

1.1 Features

- 10.8V – 13.2V input range
- 3.3V and 1.5V fixed output
- 20A DC steady-state current per output
- 500kHz switching frequency per phase
- Single main switch N-channel MOSFET and two synchronous rectifier N-channel MOSFETs per phase
- Convenient test points for probing critical waveforms and non-invasive loop response testing

1.2 Applications

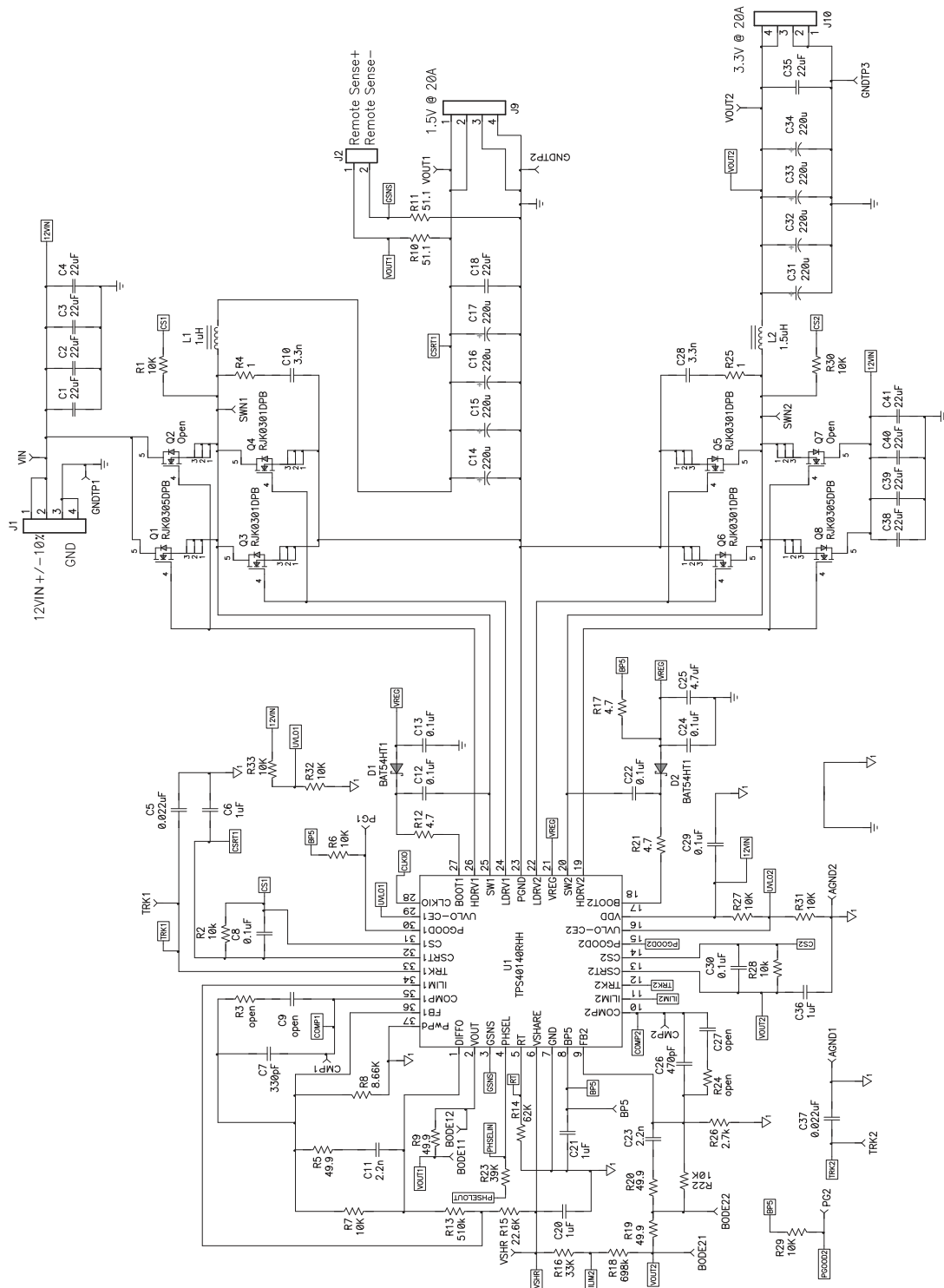
- Graphics cards
- Internet servers
- Networking equipment
- Telecommunications equipment
- DC-Power distributed systems

2 TPS40140EVM-002 Electrical Performance Specifications
Table 1. TPS40140EVM-002 Electrical and Performance Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Input voltage range		10.8		13.2	V
Max input current	$V_{IN} = 10.8V, I_{OUT1} = I_{OUT2} = 20A$		10		A
No-load input current	$V_{IN} = 13.2V, I_{OUT1} = I_{OUT2} = 0A$		170		mA
OUTPUT CHARACTERISTICS					
OUTPUT1 (V_{OUT1})					
Output voltage			1.5		V
Output voltage regulation	Line Regulation ($10.8V < V_{IN} < 13.2V, I_{OUT1} = 10A$)			0.1%	
	Load Regulation ($0A < I_{OUT1} < 20A, V_{IN} = 12V$)			0.1%	
Output voltage ripple	$V_{IN} = 13.2V, I_{OUT1} = 20A$		25		mVpp
Output load current	I_{OUT1}	0		20	A
Output over current				30	A
OUTPUT1 (V_{OUT2})					
Output voltage			3.3		V
Output voltage regulation	Line Regulation ($10.8V < V_{IN} < 13.2V, I_{OUT2} = 10A$)			0.1%	
	Load Regulation ($0A < I_{OUT2} < 20A, V_{IN} = 12V$)			0.1%	
Output voltage ripple	$V_{IN} = 13.2V, I_{OUT2} = 20A$		25		mVpp
Output load current	I_{OUT2}	0		20	A
Output over current				30	A
SYSTEM CHARACTERISTICS					
Switching frequency			500		kHz
Peak efficiency	$V_{OUT1} = 1.5V, 8A < I_{OUT1} < 12A, V_{IN} = 12V$		89%		
	$V_{OUT2} = 3.3V, 8A < I_{OUT2} < 12A$		93%		
Full load efficiency	$V_{OUT1} = 1.5V, I_{OUT1} = 20A, V_{IN} = 12V$		87%		
	$V_{OUT2} = 3.3V, I_{OUT2} = 20A$		91%		

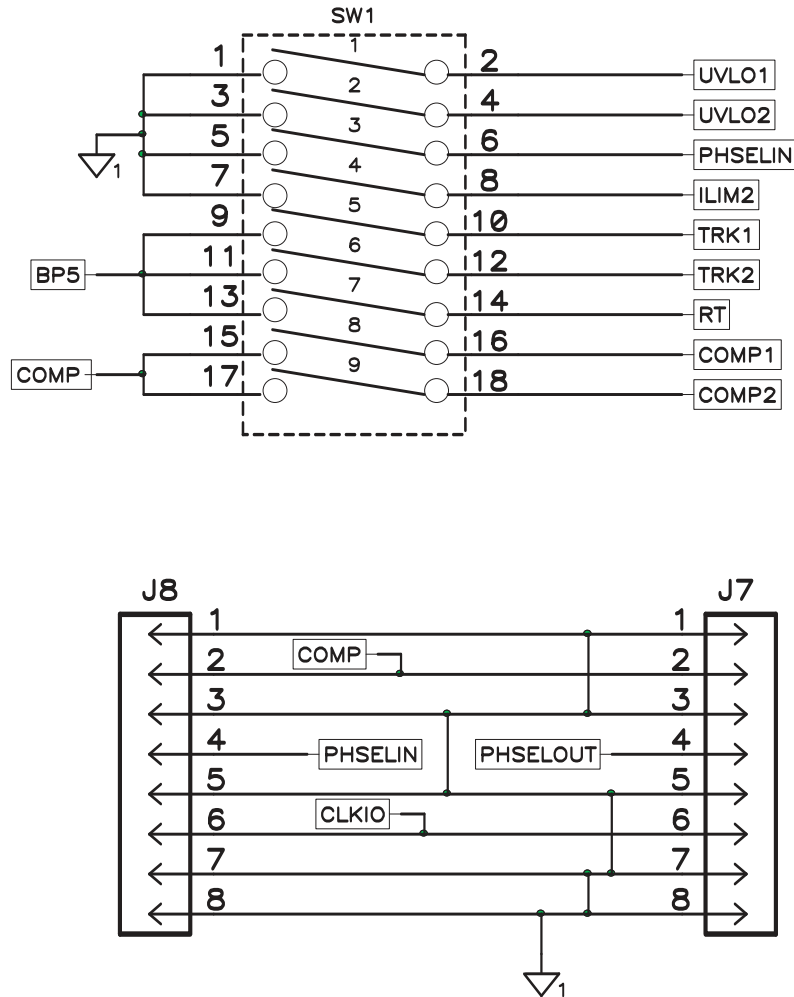
Schematic

3 Schematic



NOTE: For Reference Only, See [Table 3](#)

Figure 1. TPS40140EVM-002 Power Stage/Control Schematic



NOTE: For Reference Only, See [Table 3](#)

Figure 2. TPS40140EVM-002 Schematic

4 Test Set Up

4.1 Recommended Test Equipment

4.1.1 Voltage Source

V_{IN}

The input voltage source (V_{IN}) should be a 0–15V variable dc source capable of 20-Adc. Connect V_{IN} to J1 as shown in [Figure 3](#).

4.1.2 Meters and Shunts

V4: V_{OUT1} 0–5V voltmeter

V3: V_{OUT2} 0–5V voltmeter

V2: V_{IN} , 0–15V voltmeter

Optional, to improve current measurement.

V1: V_{SHUNT1} , 0–100mV voltmeter

SHUNT 1: 50A, 1mV/Amp or 2mV/Amp

4.1.3 Loads

LOAD1

The Output Load (LOAD1) should be an Electronic Constant Current Mode Load capable of 0 to 30-Adc at 1.5V

LOAD2

The Output Load (LOAD2) should be an Electronic Constant Current Mode Load capable of 0 to 30-Adc at 3.3V

4.1.4 Oscilloscope

A digital or analog oscilloscope can be used to measure the ripple voltage on V_{OUT} . The oscilloscope should be set for 1-M Ω impedance, 20-MHz Bandwidth, AC-coupling, 1- μ s/division horizontal resolution, 20-mV/division vertical resolution for taking output ripple measurements. Test points VOUT1, GNDTP2, VOUT2 and GNDTP3 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through VOUT1 or VOUT2 and holding the ground barrel to GNDTP2 or GNDTP3 as shown in [Figure 4](#). Using a leaded ground connection may induce additional noise due to the large ground loop area.

4.1.5 Recommended Wire Gauge

VIN to J1

The connection between the source voltage, V_{IN} and J1 of the EVM can carry as much as 15-Adc. The minimum recommended wire size is 2x AWG #16 per input connection, with the total length of wire less than 4 feet (2 feet input, 2 feet return).

J9 to LOAD1 (Power)

The power connection between J9 of the EVM and LOAD1 can carry as much as 25-Adc. The minimum recommended wire size is 2x AWG #16, with the total length of wire less than 4 feet (2 feet output, 2 feet return).

J10 to LOAD2 (Power)

The power connection between J10 of the EVM and LOAD2 can carry as much as 25-Adc. The minimum recommended wire size is 2x AWG #16, with the total length of wire less than 4 feet (2 feet output, 2 feet return).

4.1.6 Other

FAN

This evaluation module includes components that can get hot to the touch, because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200-400 lfm is required to reduce component surface temperatures to prevent user injury. The EVM should not be left unattended while powered. The EVM should not be probed while the fan is not running.

4.2 Equipment Setup

Shown in [Figure 3](#) is the basic test set up recommended to evaluate the TPS40140EVM-002.

Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.

4.2.1 Input Connections

1. Prior to connecting the dc input source, V_{IN} , it is advisable to limit the source current from V_{IN} to 20A maximum. Make sure V_{IN} is initially set to 0V and connected as shown in [Figure 3](#).
2. For more accurate current measurement it is recommended to use a current measuring shunt. Connect the two wires from J1 to SHUNT1 then connect SHUNT1 using two more AWG #16 wires to the positive terminal of V_{IN} dc source, as shown in [Figure 3](#).
3. Connect voltmeter V1 across the shunt.

4.2.2 Output Connections

1. Connect LOAD1 to J9, set LOAD1 to constant-current mode to sink 0-Adc before V_{IN} is applied.
2. Connect LOAD2 to J10, set LOAD2 to constant-current mode to sink 0-Adc before V_{IN} is applied.
3. Connect voltmeter, V3, across VOUT2 and GNDTP3, as shown in [Figure 3](#).
4. Connect voltmeter, V4, across VOUT1 and GNDTP2, as shown in [Figure 3](#).

4.2.3 Other Connections

1. Place a fan as shown in [Figure 3](#) and turn on, making sure air is flowing across the EVM.

4.2.4 Set Up Diagram

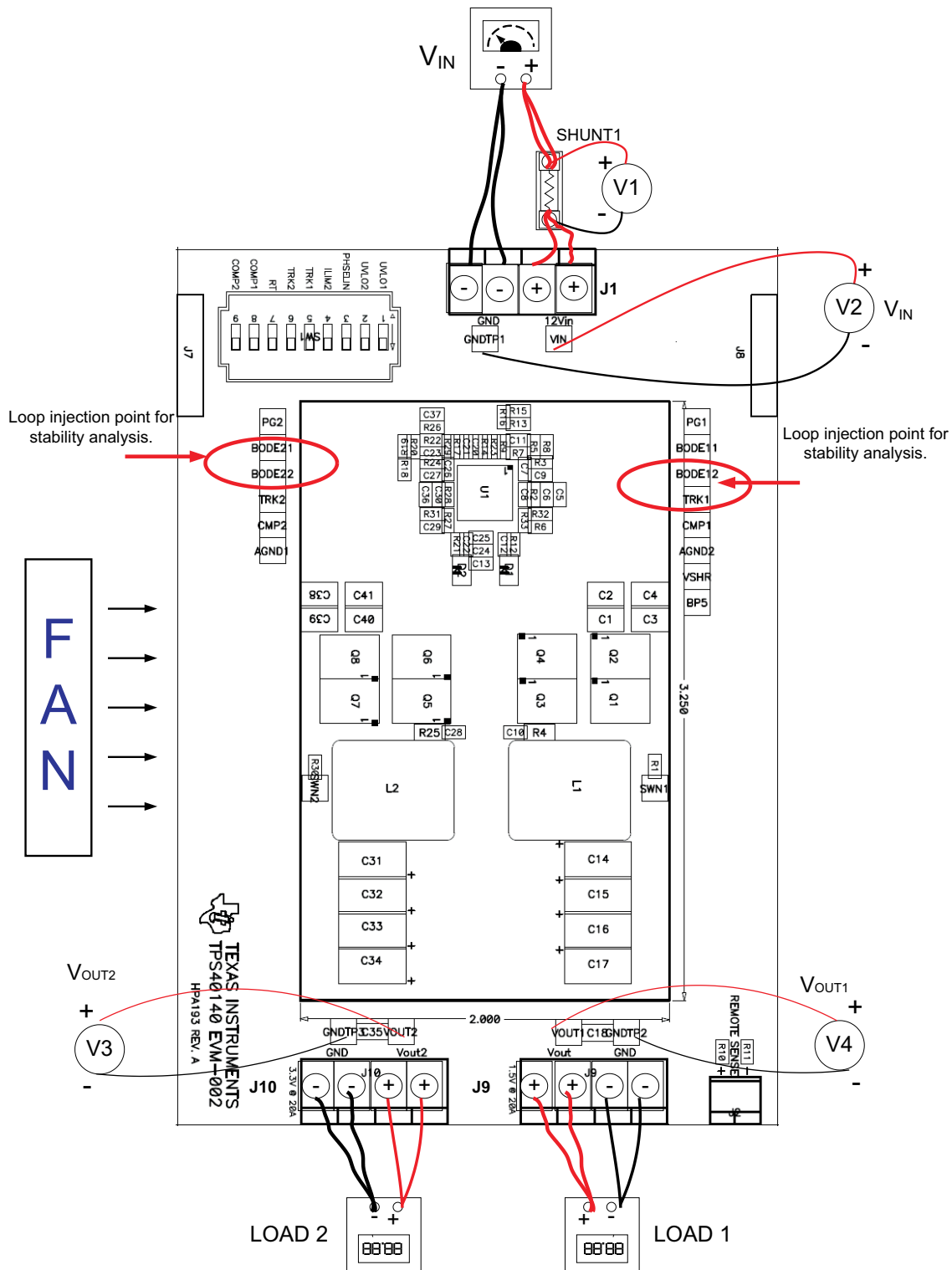


Figure 3. TPS40140EVM-002 Recommended Test Set-Up

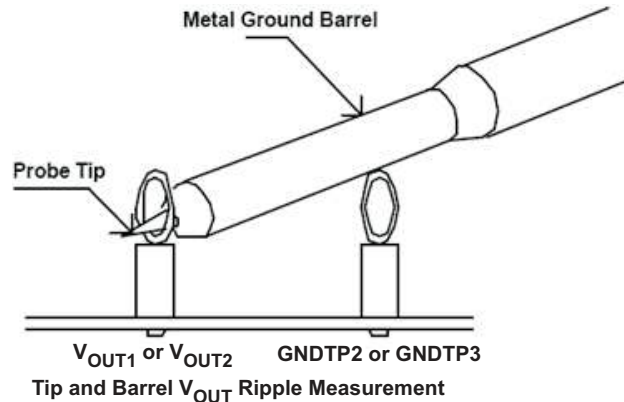


Figure 4. Output Ripple Measurement

4.3 Start Up and Test Procedure

1. Ensure LOAD1 and LOAD2 are set to constant-current mode and to sink 0-Adc.
2. Increase V_{IN} from 0V to 4.5Vdc, V_{OUT1} and V_{OUT2} should be in regulation per Table 1. Continue increasing V_{IN} to 12V.
3. Vary LOAD1 and/or LOAD2 from 0–20Adc, V_{OUT1} and V_{OUT2} should remain in regulation per Table 1, for all combinations of load on LOAD1 and LOAD2, up to 20A.
4. Vary V_{IN} from 10.8Vdc to 13.2Vdc, V_{OUT1} and V_{OUT2} should remain in regulation per Table 1, for all combinations of load on LOAD1 and LOAD2, up to 20A.
5. For various V_{IN} settings vary LOAD1 and/or LOAD2 from 0–20Adc. V_{OUT1} and V_{OUT2} should remain in regulation per Table 1, for all combinations of load on LOAD1 and LOAD2, up to 20A.

4.4 Control Loop Gain and Phase Measurement Procedure

1. Connect 1-kHz to 1-MHz isolation transformer to test points marked BODE11 (or BODE21) and BODE12 (or BODE 22).
2. Connect input signal amplitude measurement probe (Channel A) to BODE12 (or BODE 22).
3. Connect output signal amplitude measurement probe (Channel B) to BODE11 (or BODE21).
4. Connect ground lead of channel A and channel B to AGND2 (or AGND1).
5. Inject 25mV or less signal across R9 (or R19) through the isolation transformer.
6. Sweep frequency from 100Hz to 1MHz, with 10Hz or lower post filter.
7. Control-loop gain can be measured by $20 \times \text{LOG} \left(\frac{\text{ChannelB}}{\text{ChannelA}} \right)$.
8. Control-loop phase is measured by the phase difference between Channel A and Channel B.
9. Disconnect isolation transformer from the bode plot test points before making other measurements (signal injection into feedback may interfere with accuracy of other measurements).

4.5 EVM Configuration

The TPS40140EVM-002 is built in such away to allow the user to configure its operation. Basic configurations are:

1. Dual-output converter
2. Connect with the two-phase single-output EVM to construct a multiphase converter

The following sections cover the various configurations. It is recommended to power down the EVM before changing the configuration. Disable/Enable can be changed when power is present.

4.5.1 Dual Output Configuration (Default)

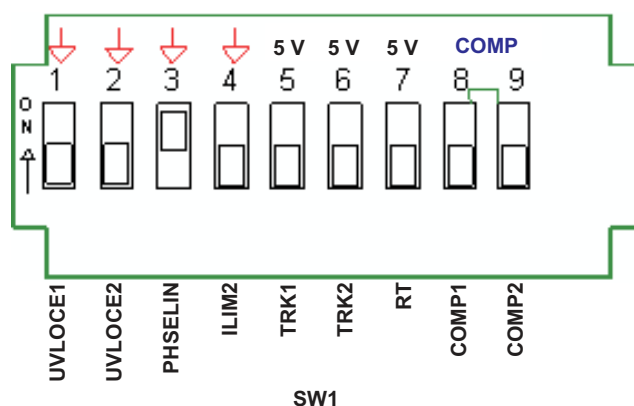


Figure 5. Default Configuration

Phase 1 and phase 2 are enabled with the default configuration.

4.5.2 Enabling/Disabling the Outputs

Switches 1 and 2 on SW1 allow the user to disable or enable each output individually. Figure 6 shows the different settings for these switches.

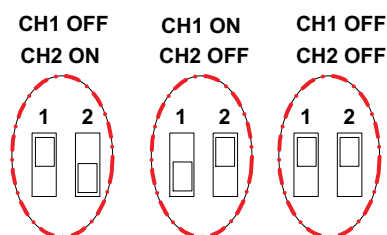


Figure 6. Output Enable/Disable Configuration

4.5.3 Multiphases Configuration

Here, in Figure 7, CH1 is configured as a slave that can construct a 3-phase converter together with a two-phase EVM. CH2 is still an independent channel.

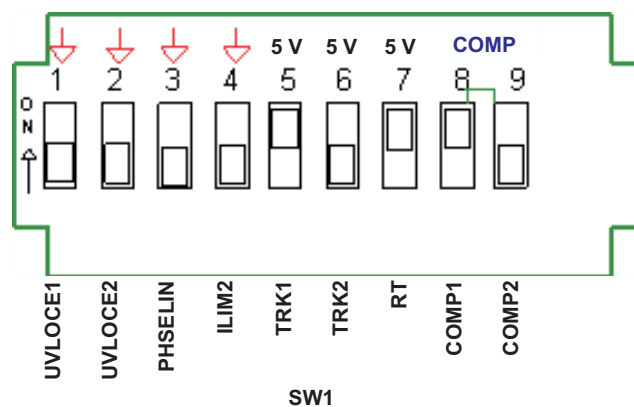


Figure 7. Configure CH1 as Slave and CH2 as Independent Channel

In Figure 8, CH2 is configured as a slave that can construct a 3-phase converter together with a two-phase EVM. CH1 is still an independent channel.

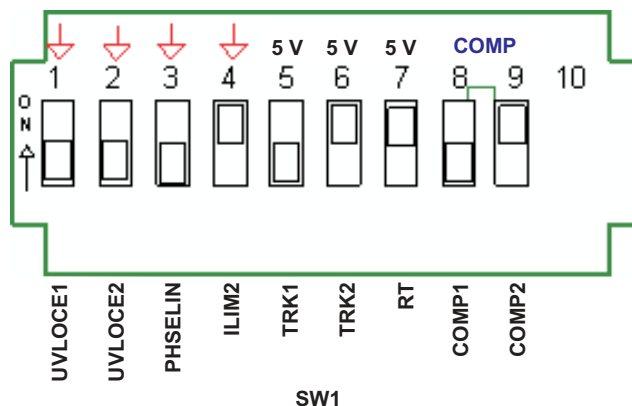


Figure 8. Configure CH2 as Slave and CH1 as Independent Channel

J7 and J8 are used to connect this EVM to the two-phase EVM board. Assume the TPS40140 on the two-phase EVM is set as the master chip; the connection between the two EVM boards is shown in Figure 9.

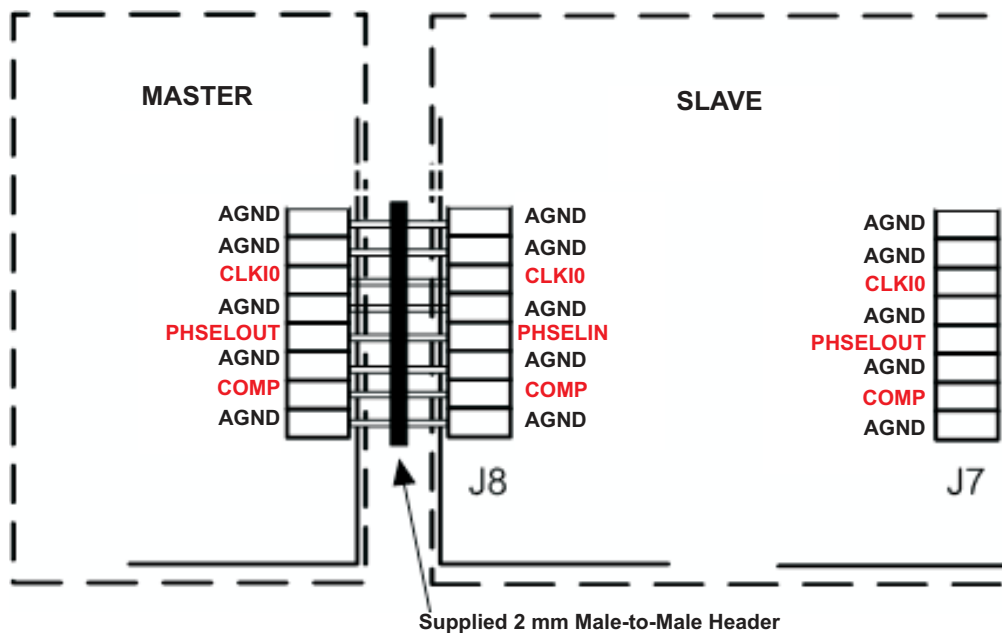


Figure 9. Master and Slave Connection (this EVM is the slave)

4.6 Test Points

Several test points are located around the board. These can be used to sense what is occurring at different points of the converter. Table 2 lists these test points and what they are used for.

Table 2. List of Test Points

NAME	DESCRIPTION
VOUT1	Output 1 positive sense point
GNNDTP2	Output 1 negative sense point
VOUT2	Output 2 positive sense point
GNNDTP3	Output 2 negative sense point
VIN	Input voltage positive sense point
GNNDTP1	Input voltage negative sense point
SWN1	Channel 1 switch node
SWN2	Channel 2 switch node
TRK1	Channel 1 track pin
TRK2	Channel 2 track pin
VSHR	Vshare sense point
CMP1	COMP1 sense point
CMP2	COMP2 sense point
PG1	Channel 1 PGOOD
PG2	Channel 2 PGOOD
BODE11	Channel 1 loop injection point
BODE12	Channel 1 loop injection point
BODE21	Channel 2 loop injection point
BODE22	Channel 2 loop injection point
BP5	BP5 sense point
AGND1	Analog ground
AGND2	Analog ground

4.7 Equipment Shutdown

1. Shut down LOAD1 and LOAD2
2. Shut down V_{IN}
3. Shut down FAN

5 TPS40140EVM-002 Typical Performance Data and Characteristic Curves

Figure 10 through Figure 13 present typical performance curves for the TPS40140EVM-002. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

5.1 Efficiency

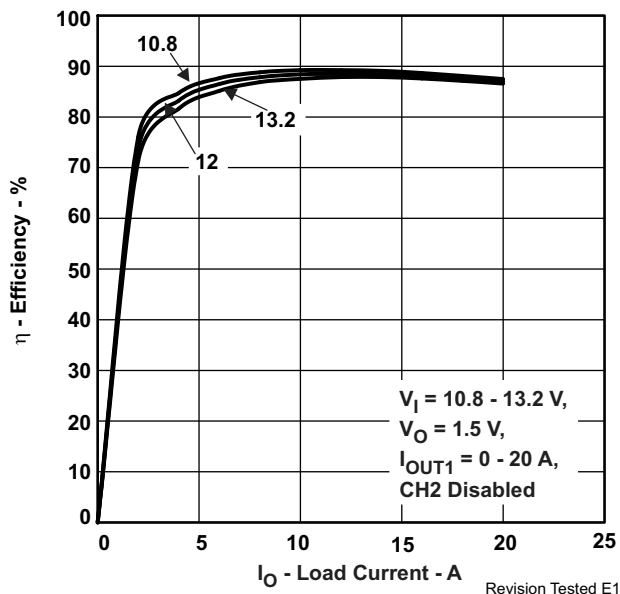


Figure 10. TPS40140EVM-002 Efficiency

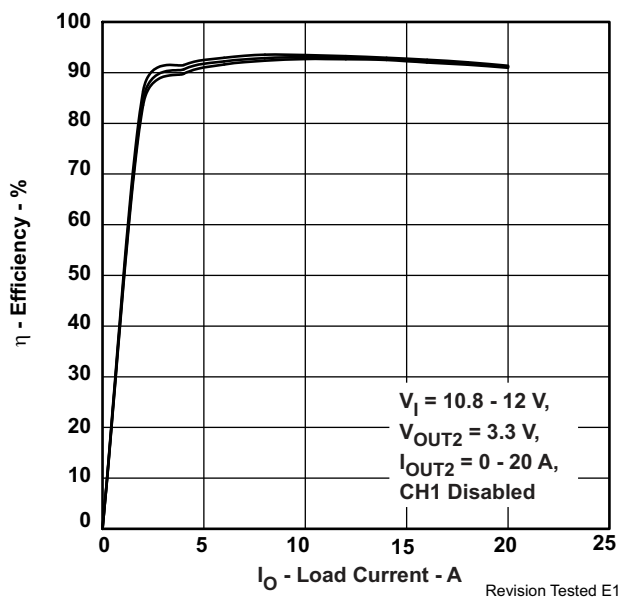


Figure 11. TPS40140EVM-002 Efficiency

5.2 Line and Load Regulation

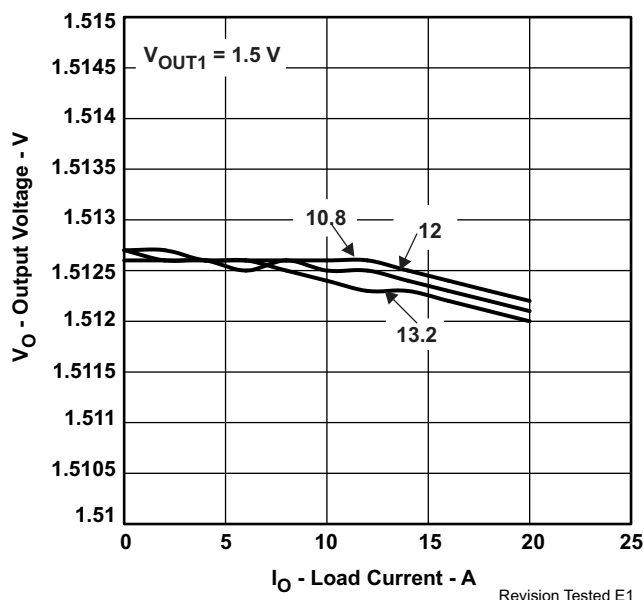


Figure 12. TPS40140EVM-002 $V_{OUT1}=1.5V$ Line and Load Regulation

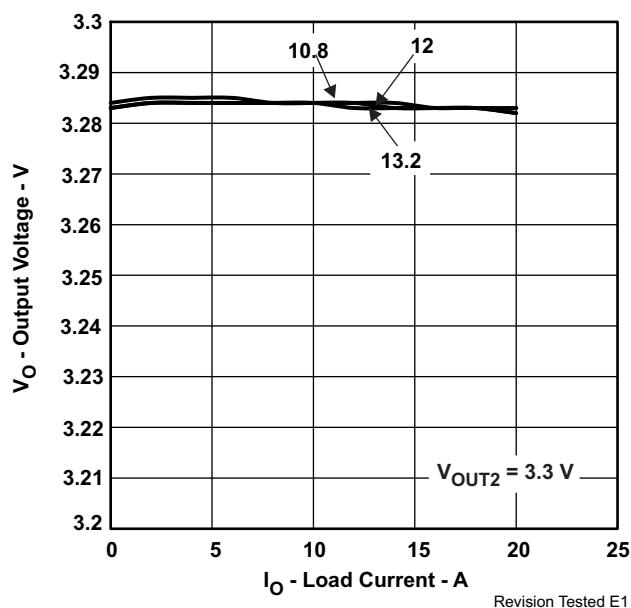


Figure 13. TPS40140EVM-002 $V_{OUT2}=3.3V$ Line and Load Regulation

6 EVM Assembly Drawings and Layout

Figure 14 through Figure 19 shows the design of the TPS40140EVM-002 printed circuit board. The EVM has been designed using a four-layer, 2-oz copper-clad circuit board with all components on the top side to allow the user to easily view, probe and evaluate the TPS40140 control IC in a practical application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems.

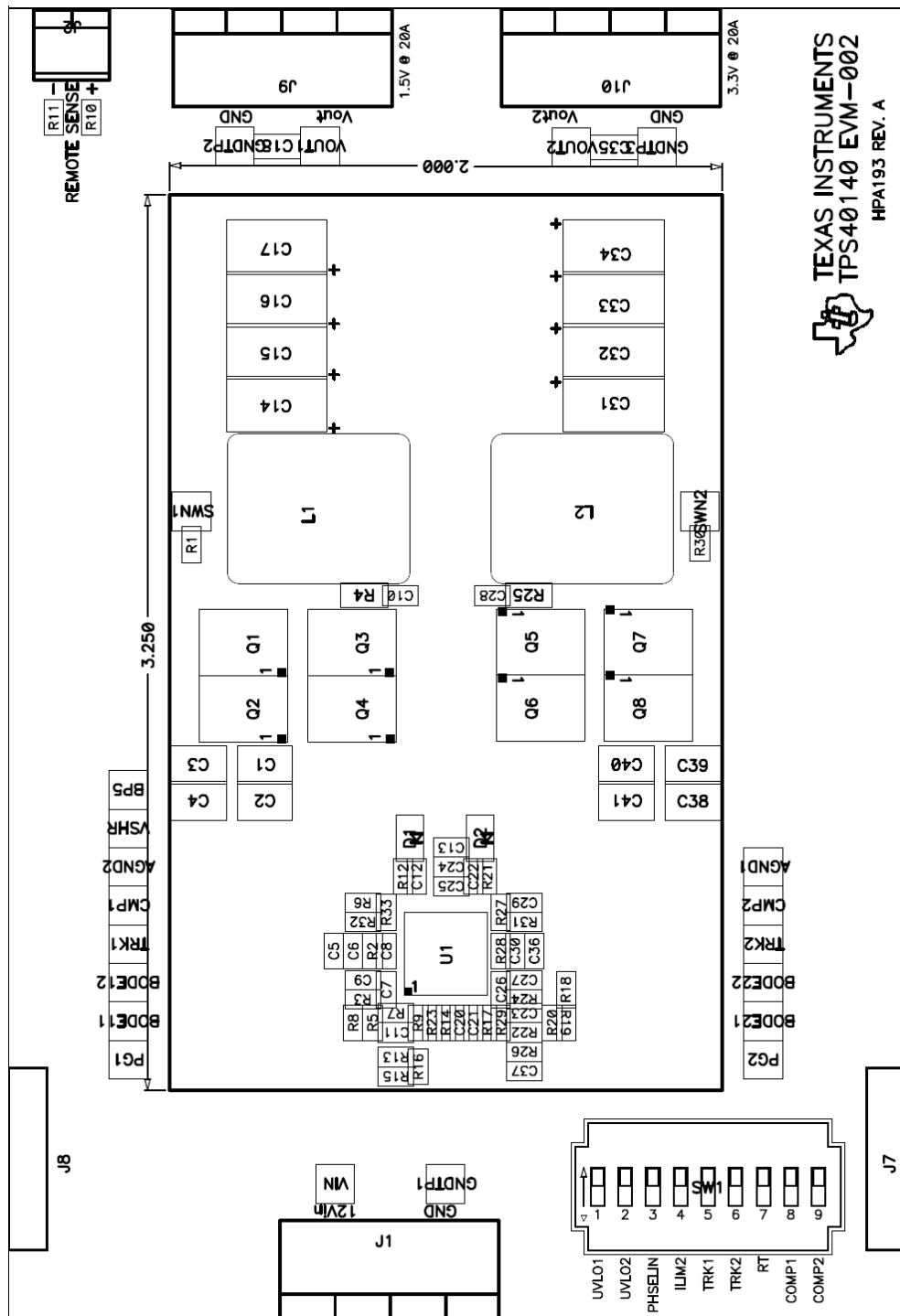


Figure 14. TPS40140EVM-002 Component Placement (Viewed from Top)

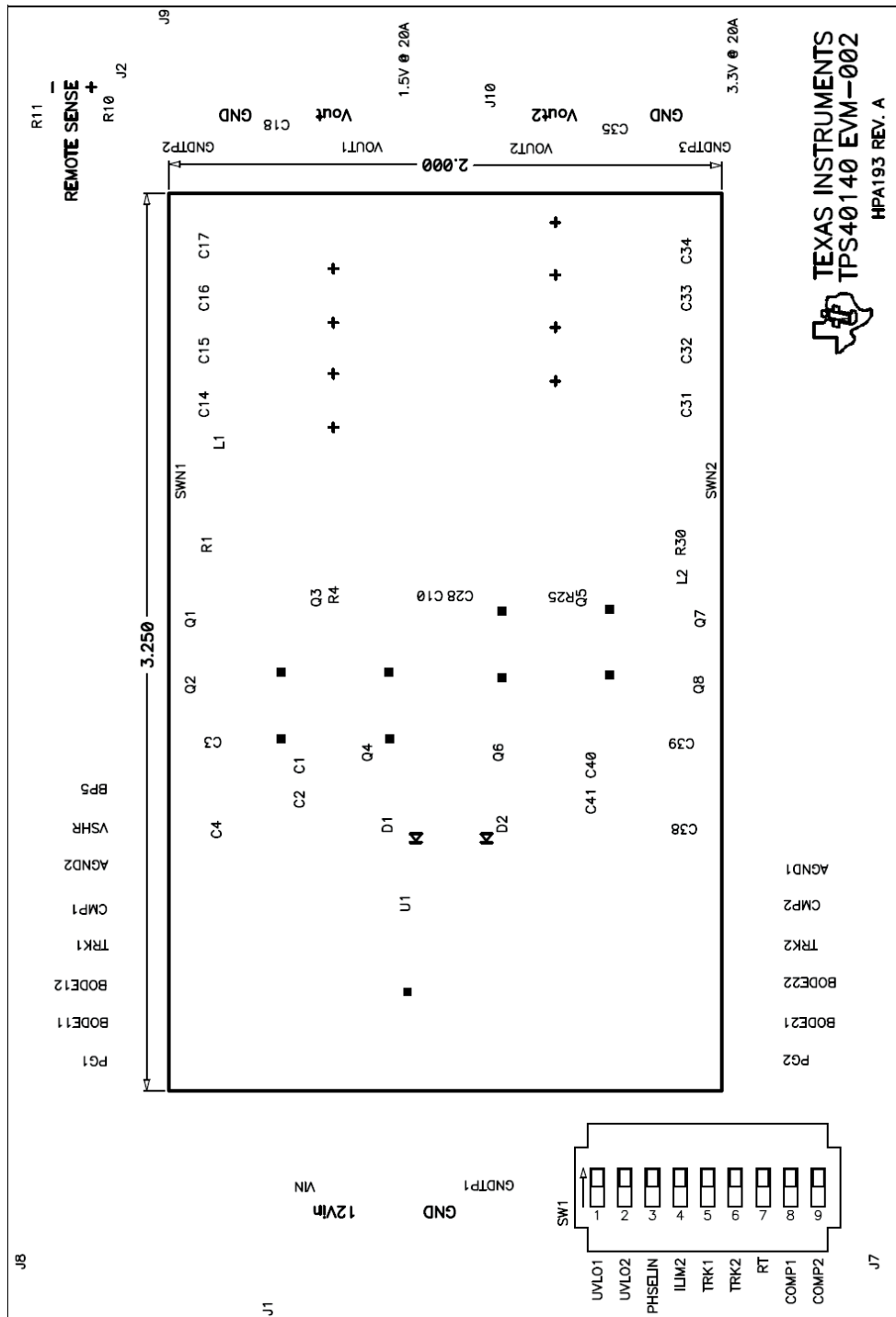


Figure 15. TPS40140EVM-002 Silkscreen (Viewed from Top)

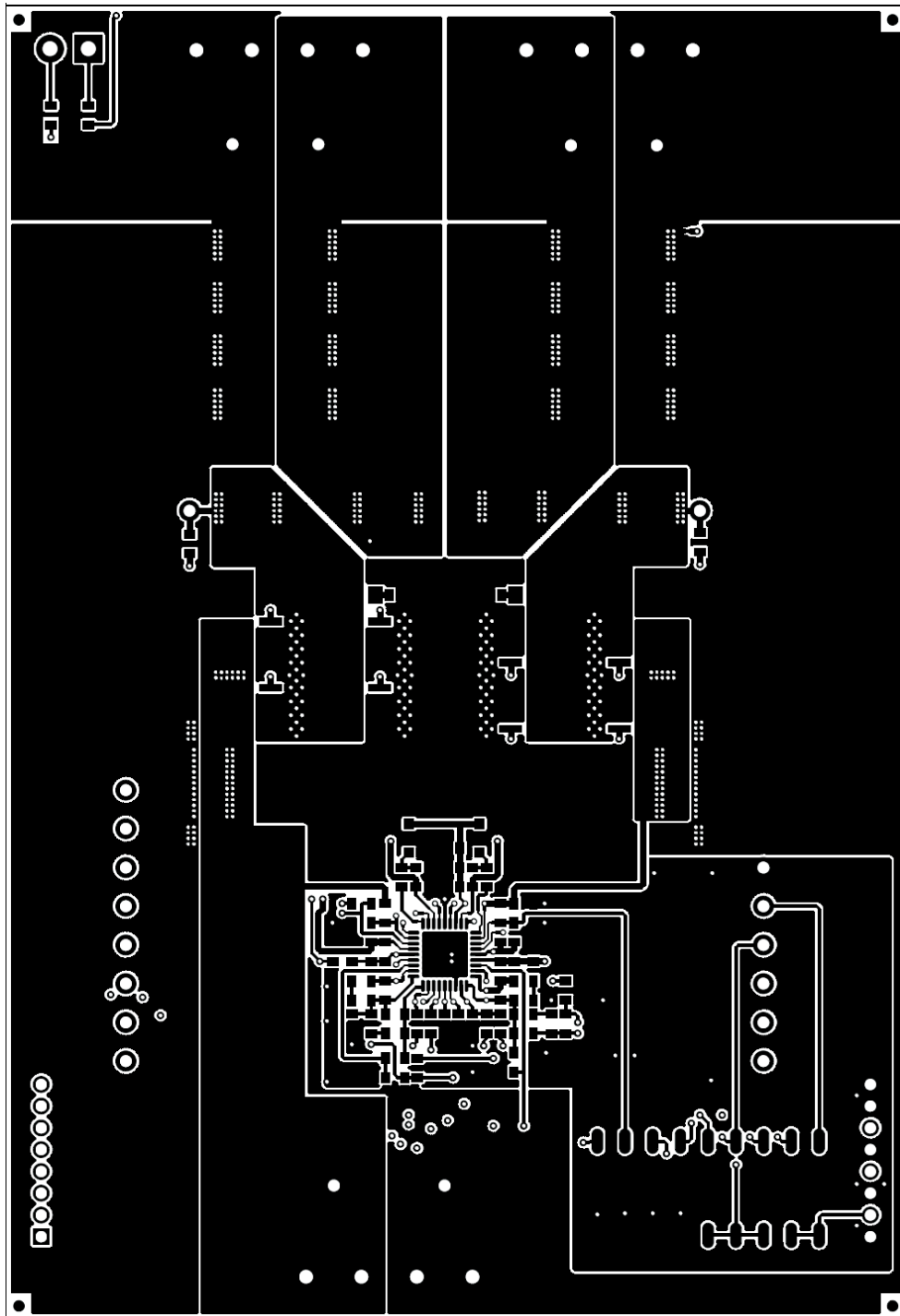


Figure 16. TPS40140EVM-002 Top Copper (Viewed from Top)

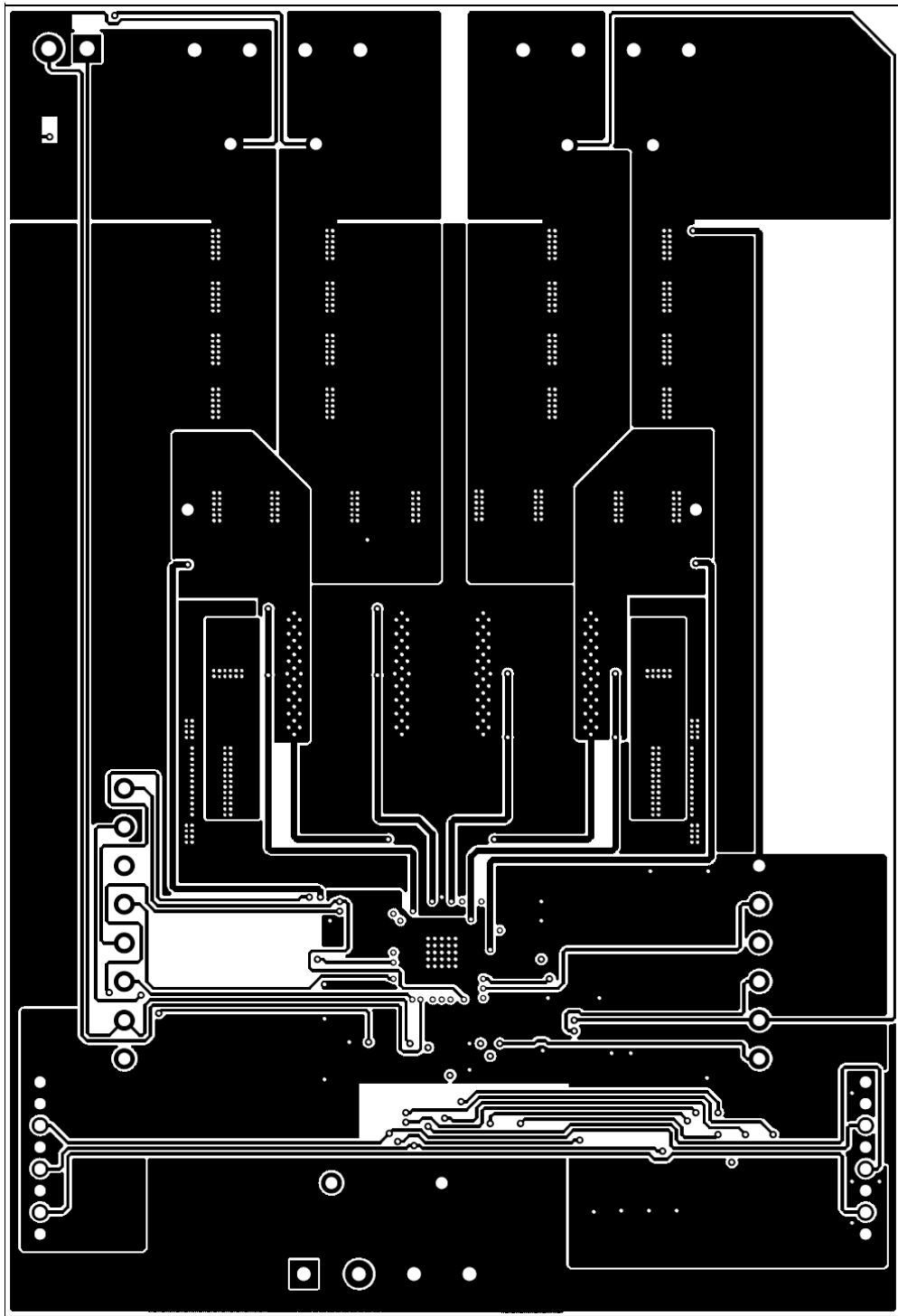


Figure 17. TPS40140EVM-002 Layer 2 Copper (X-Ray View from Top)

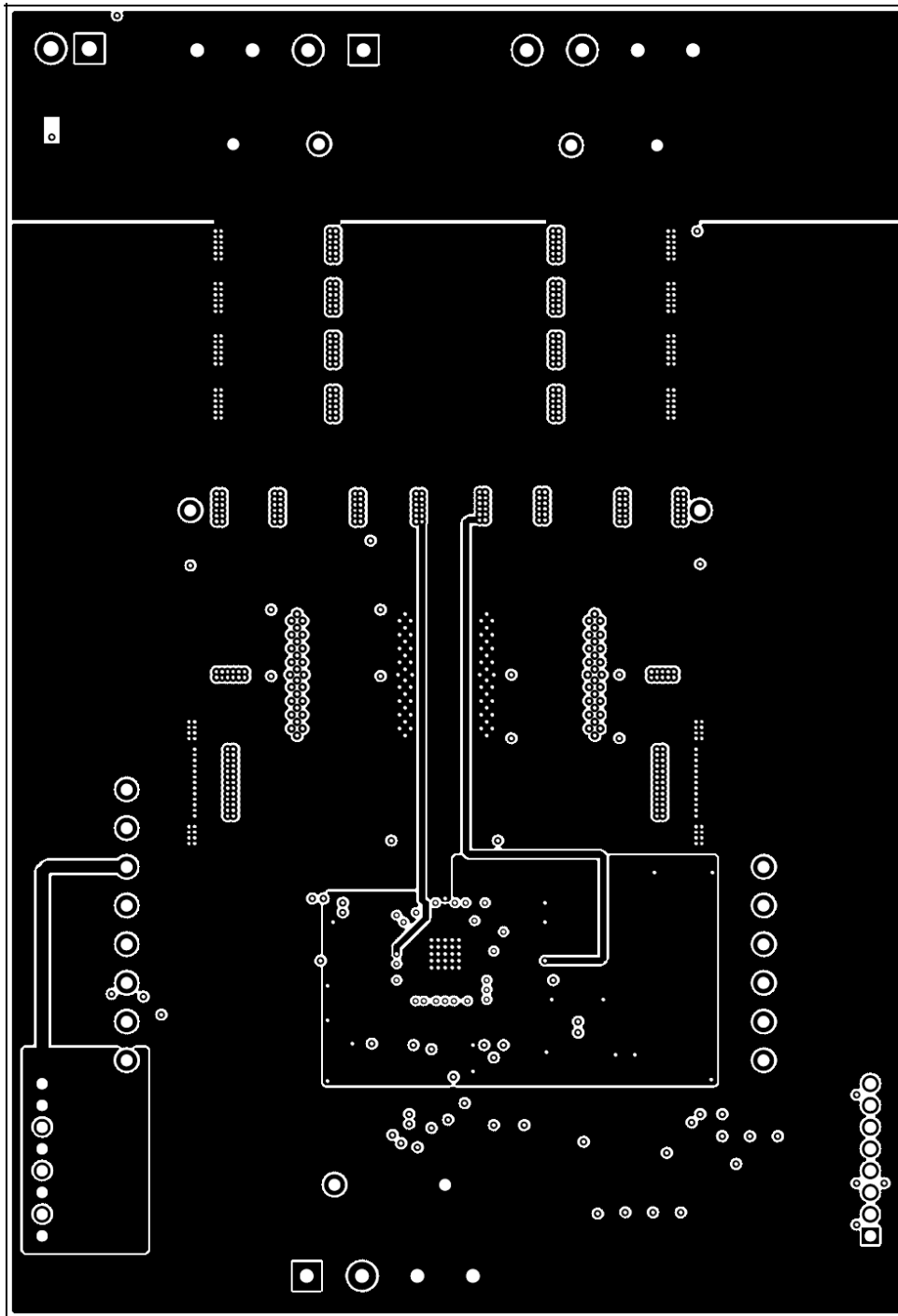


Figure 18. TPS40140EVM-002 Layer 3 Copper (X-Ray View from Top)

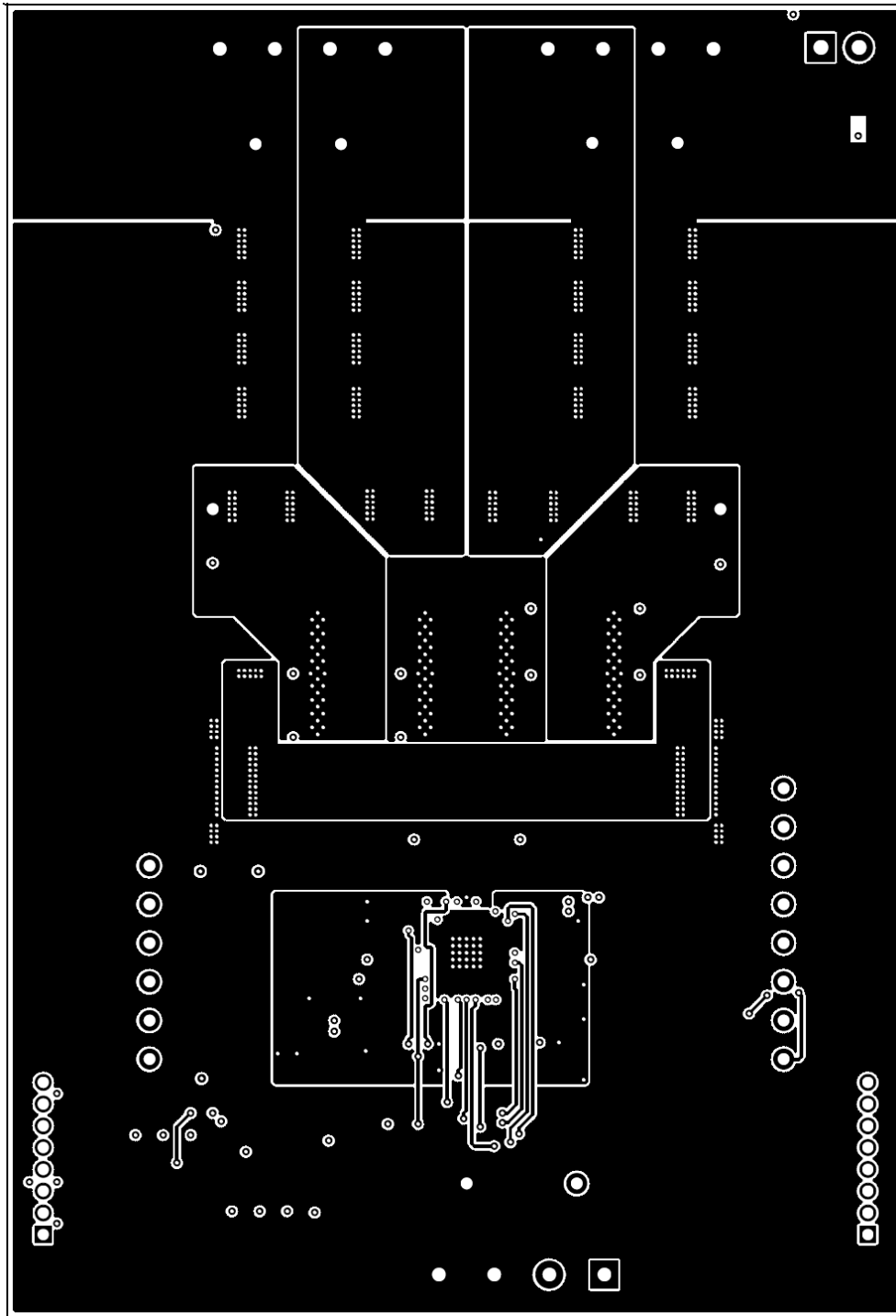


Figure 19. TPS40140EVM-002 Bottom Copper (X-Ray View from Top)

7 List of Materials

Table 3 lists the EVM components as configured according to the schematic shown in Figure 1.

Table 3. TPS40140EVM-002 Bill of Materials

COUNT	Ref	Description	Part Number	MFR
8	C1– C4, C38–C41	Capacitor, Ceramic, 22 μ F, 16V, X5R, 20%, 1210	Std	Std
2	C10, C28	Capacitor, Ceramic, 3.3nF, 50V, 0603, 10%, 0603	Std	Std
1	C11	Capacitor, Ceramic, 2.2nF, 16V, X7R, 10%, 0603	Std	Std
8	C14–C17,C31–C34	Capacitor, Aluminum-SE, 220- μ F, 4-V, 5 m Ω	EEFSE0G221R	Panasonic
2	C18, C35	Capacitor, Ceramic, 22 μ F, 6.3V, X5R, 10%, 0805	Std	Std
1	C23	Capacitor, Ceramic, 2.2nF, 16V, X7R, 10%, 0603	Std	Std
1	C25	Capacitor, Ceramic, 4.7 μ F, 6.3V, X5R, 10%, 0603	Std	Std
1	C26	Capacitor, Ceramic, 470pF, 16V, COG, 5%, 0603	Std	Std
2	C5, C37	Capacitor, Ceramic, 0.022 μ F, 16V, X7R, 10%, 0603	Std	Std
4	C6, C20, C21, C36	Capacitor, Ceramic, 1 μ F, 6.3V, X5R, 10%, 0603	Std	Std
1	C7	Capacitor, Ceramic, 330pF, 16V, COG, 5%, 0603	Std	Std
7	C8, C12, C13, C22, C24, C29, C30	Capacitor, Ceramic, 0.1 μ F, 16V, X7R, 10%, 0603	Std	Std
0	C9, C27	Capacitor, Ceramic, 3900pF, 16V, X7R, 10%, 0603	Std	Std
2	D1, D2	Diode, Schottky, 30V, 0.35Vf, SOD-323	BAT54HT1	On Semi
3	J1, J9, J10	Terminal Block, 4-pin, 15-A, 5,1mm	ED2227	OST
1	J2	Terminal Block, 2-pin, 6-A, 3,5mm	ED1514	OST
2	J7, J8	Conn, Recept, 2mm, 8-pin Right Angle, Female (36-pin Strip)	PPPN081FGGN	Sullins
1	L1	Inductor, SMT, 1.0 μ H, 32A	1HLP-5050FD	Vishay
1	L2	Inductor, SMT, 1.5 μ H, 27A	1HLP-5050FD	Vishay
2	Q1, Q8	MOSFET, N-Ch, 30V, 30A, 0.013 Ω , LFPAK	RJK0305DPB	Renesas
0	Q2, Q7	MOSFET, Open, LFPAK	Open	Open
4	Q3–Q6	MOSFET, N-Ch, 30V, 60A, 0.004 Ω , LFPAK	RJK0301DPB	Renesas
12	R1, R2, R6, R7, R22, R27–R33	Resistor, Chip, 10k Ω , 1%, 0603	Std	Std
2	R10, R11	Resistor, Chip, 51.1 Ω , 1%, 0603	Std	Std
3	R12, R17, R21	Resistor, Chip, 4.7 Ω , 5%, 0603	Std	Std
1	R13	Resistor, Chip, 510k Ω , 1%, 0603	Std	Std
1	R14	Resistor, Chip, 62k Ω , 1%, 0603	Std	Std
1	R15	Resistor, Chip, 22.6k Ω , 1%, 0603	Std	Std
1	R16	Resistor, Chip, 33k Ω , 1%, 0603	Std	Std
1	R18	Resistor, Chip, 698k Ω , 1%, 0603	Std	Std
4	R5, R9, R19, R20	Resistor, Chip, 49.9 Ω , 1%, 0603	Std	Std
1	R23	Resistor, Chip, 39k Ω , 1%, 0603	Std	Std
1	R26	Resistor, Chip, 2.7k Ω , 1%, 0603	Std	Std
0	R3, R24	Resistor, Chip, 39.2k Ω , 1%, 0603	Std	Std
2	R4, R25	Resistor, Chip, 1 Ω , 1%, 0805	Std	Std
1	R8	Resistor, Chip, 8.66k Ω , 1%, 0603	Std	Std
1	SW1	SWITCH, 9 POS, SPST, low profile, SMT	204-9ST	CTS
1	U1	IC, 2-Phase or Dual Output PWM Controller, QFN	TPS40140RHH	Texas Instruments

Table 3. TPS40140EVM-002 Bill of Materials (continued)

COUNT	Ref	Description	Part Number	MFR
17	SWN1, SWN2, TRK1, TRK2, VIN, VOUT1, VOUT2, VSHR, BODE11, BODE12, BODE21, BODE22, BP5, CMP1, CMP2, PG1, PG2	Test Point, Red, Thru Hole Color Keyed	5000	Keystone
5	GNDTP1, GNDTP2, GNDTP3, AGND1, AGND2	Test Point, Black, Thru Hole Color Keyed	5001	Keystone
2		Header, 2mm, Single, Str,8 pos, Male	PRPN081PAEN	Sullins
1	HPA193	PCB, 4.75 inch × 3.25 inch	HPA193	

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 10.8-V to 13.2-V, and the output voltage range of 3.3-V and 1.5-V fixed output at 20A load.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 70°C . The EVM is designed to operate properly with certain components above 70°C as long as the input and output ranges are maintained. These components include but are not limited to, switching transistors, inductor, and IC. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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