NP20P06YLG

MOS FIELD EFFECT TRANSISTOR

R07DS0706EJ0100
Rev.1.00
Apr 17, 2012

Description

The NP20P06YLG is P-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Low on-state resistance
  $R_{DS(on)}$ = 47 mΩ MAX. (V_{GS} = –10 V, I_D = –10 A)
  $R_{DS(on)}$ = 64 mΩ MAX. (V_{GS} = –5 V, I_D = –10 A)
  $R_{DS(on)}$ = 70 mΩ MAX. (V_{GS} = –4.5 V, I_D = –10 A)
- Logic level drive type
- Gate to Source ESD protection diode built in
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Packing		Package
NP20P06YLG-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON
NP20P06YLG-E2-AY *1			Taping (E2 type)	

Note: *1 Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–60	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	∓20	A
Drain Current (pulse) *1	$I_{D(pulse)}$	∓60	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	57	W
Total Power Dissipation (T_A = 25°C) *2	P_{T2}	1.0	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Single Avalanche Current *3	I_{AS}	17	A
Single Avalanche Energy *3	E_{AS}	29	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	2.63	°C/W
Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	150	°C/W

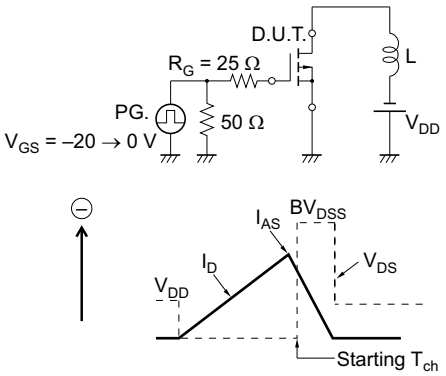
Notes: *1 T_C = 25°C, $P_W \leq 10$ μs, Duty Cycle ≤ 1%
*2 Mounted on glass epoxy substrate of 40 mm × 40 mm × 1.6 mmt with 4% copper area (35 μm)
*3 $T_{ch(start)}$ = 25°C, V_{DD} = –30 V, R_G = 25 Ω, L = 100 μH, V_{GS} = –20 V → 0 V

Electrical Characteristics (T_A = 25°C)

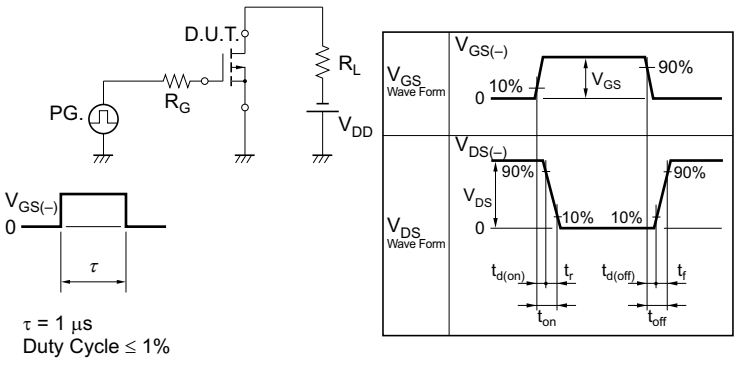
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	–1	μA	V_{DS} = –60 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	∓10	μA	V_{GS} = ∓20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	–1.0	–1.7	–2.5	V	V_{DS} = V_{GS}, I_D = –250 μA
Forward Transfer Admittance *1	$\lvert y_{fs} \rvert$	9	20	—	S	V_{DS} = –5 V, I_D = –10 A
Drain to Source On-state Resistance *1	$R_{DS(on)1}$	—	37	47	mΩ	V_{GS} = –10 V, I_D = –10 A
	$R_{DS(on)2}$	—	41	64	mΩ	V_{GS} = –5 V, I_D = –10 A
	$R_{DS(on)3}$	—	43	70	mΩ	V_{GS} = –4.5 V, I_D = –10 A
Input Capacitance	C_{iss}	—	1605	2407	pF	V_{DS} = –25 V
Output Capacitance	C_{oss}	—	150	225	pF	V_{GS} = 0 V
Reverse Transfer Capacitance	C_{rss}	—	96	173	pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$	—	8	16	ns	V_{DD} = –30 V, I_D = –10 A
Rise Time	t_r	—	8	20	ns	V_{GS} = –10 V
Turn-off Delay Time	$t_{d(off)}$	—	160	320	ns	R_G = 0 Ω
Fall Time	t_f	—	80	200	ns	
Total Gate Charge	Q_G	—	34	51	nC	V_{DD} = –48 V
Gate to Source Charge	Q_{GS}	—	4	—	nC	V_{GS} = –10 V
Gate to Drain Charge	Q_{GD}	—	9	—	nC	I_D = –20 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$	—	0.95	1.5	V	I_F = 20 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	—	38	—	ns	I_F = 20 A, V_{GS} = 0 V
Reverse Recovery Charge	Q_{rr}	—	50	—	nC	di/dt = 100 A/μs

Note: *1 Pulsed test

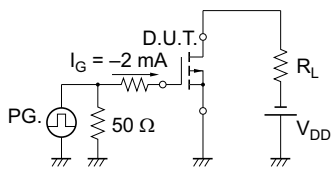
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

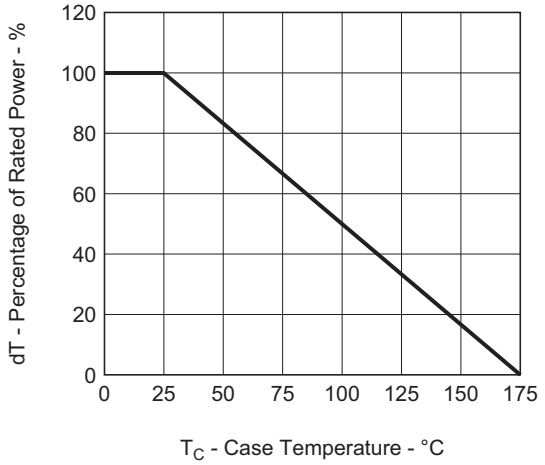


TEST CIRCUIT 3 GATE CHARGE

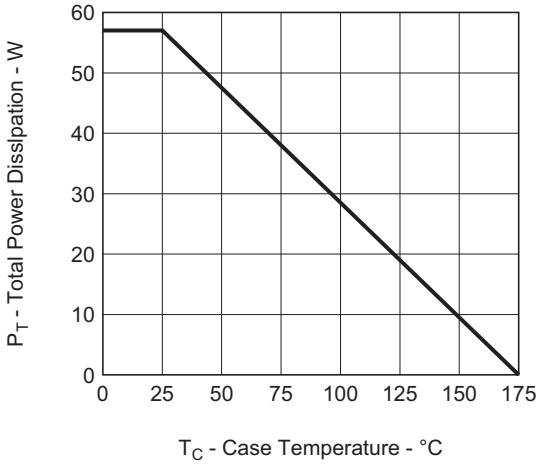


Typical Characteristics (T_A = 25°C)

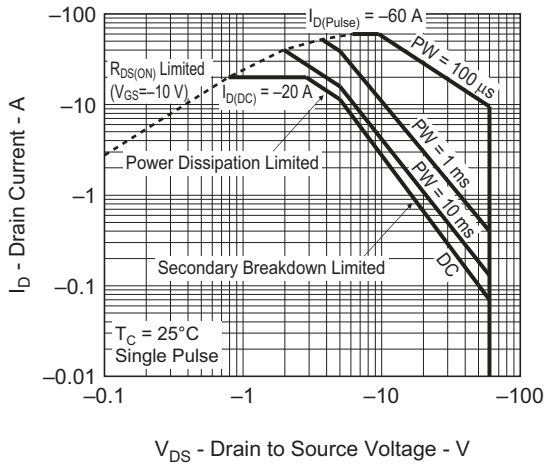
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



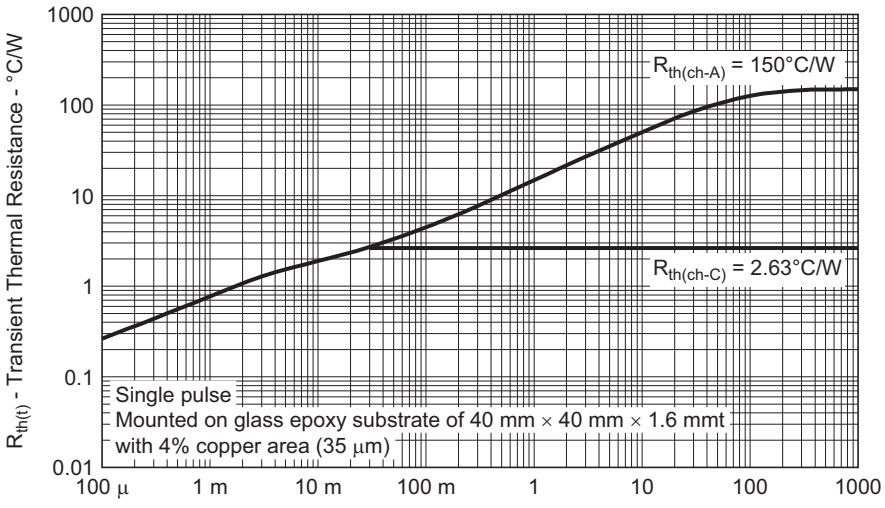
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



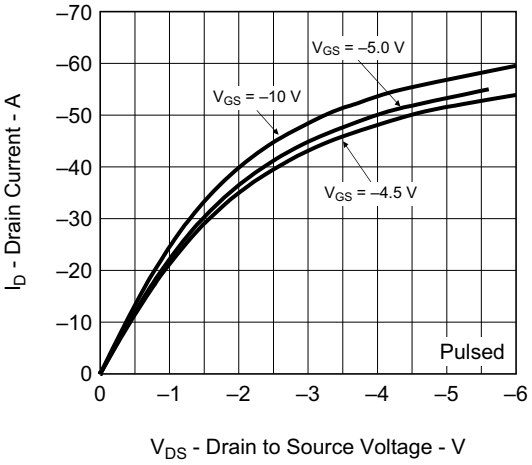
FORWARD BIAS SAFE OPERATING AREA



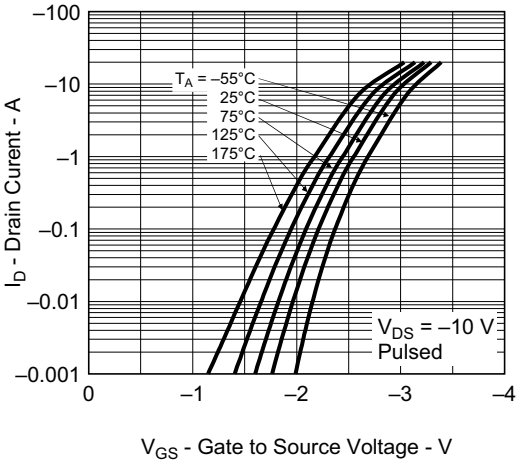
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



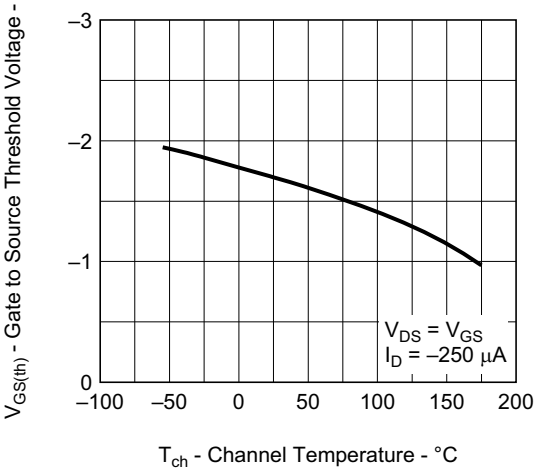
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



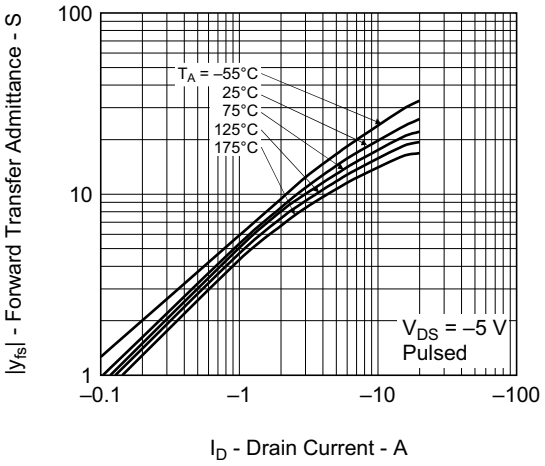
FORWARD TRANSFER CHARACTERISTICS



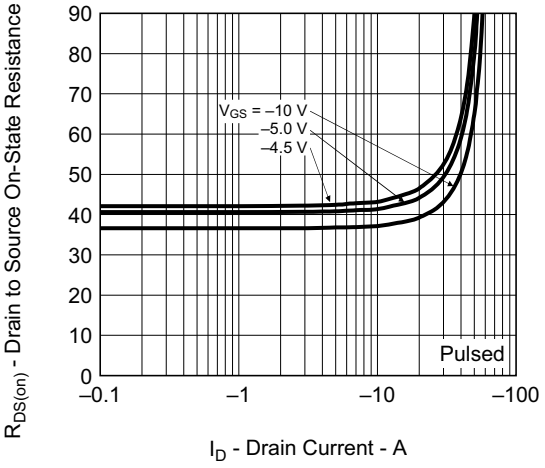
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



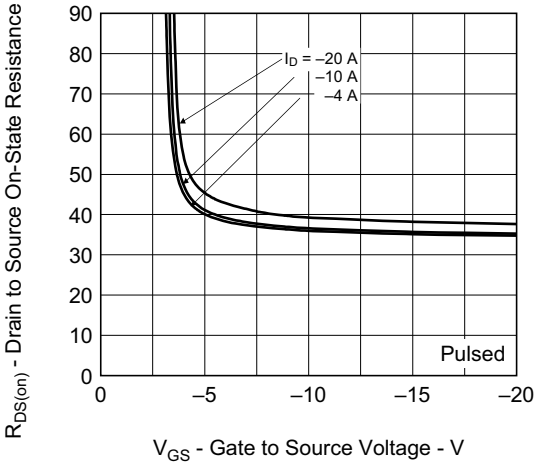
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



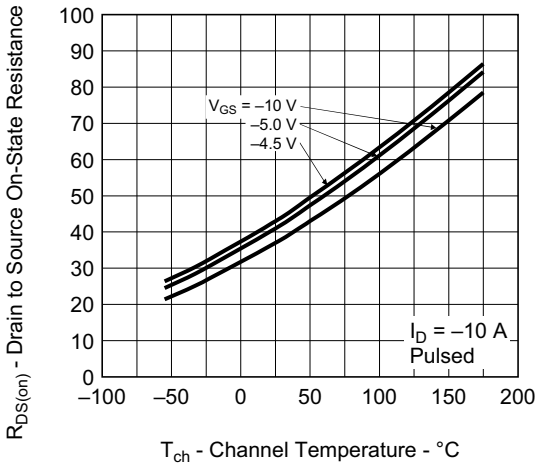
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



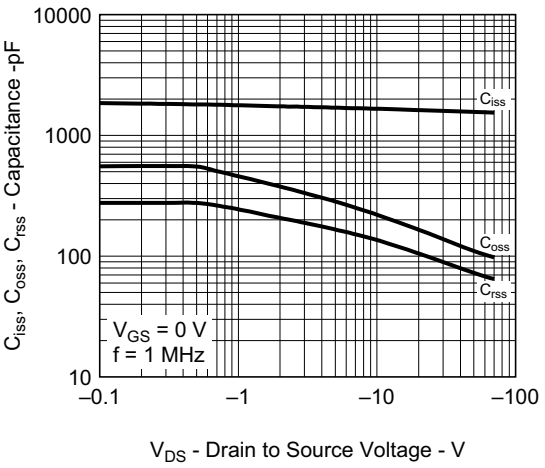
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



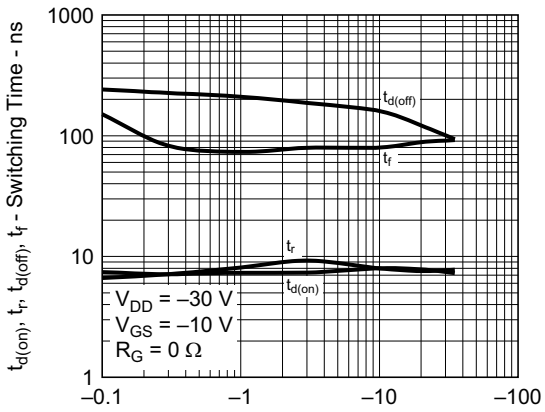
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



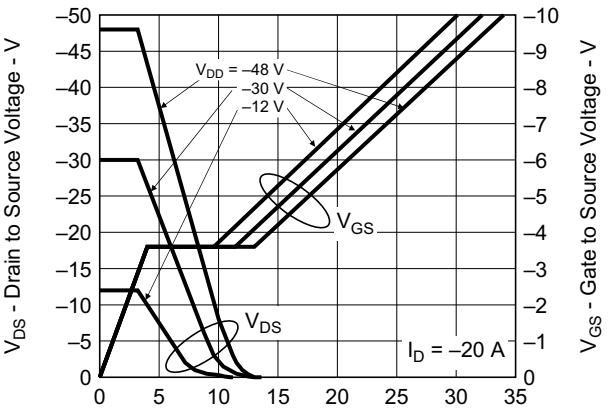
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



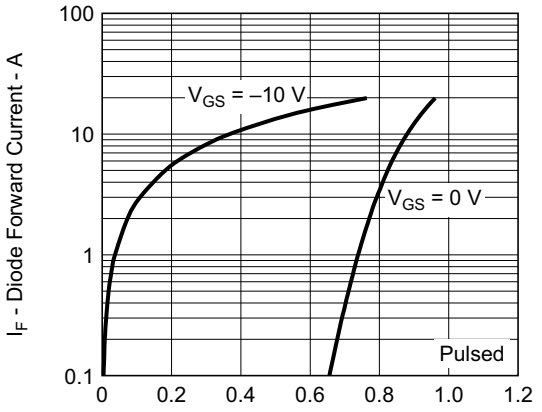
SWITCHING CHARACTERISTICS



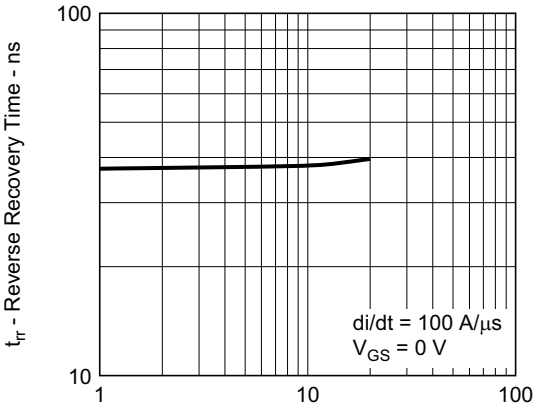
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

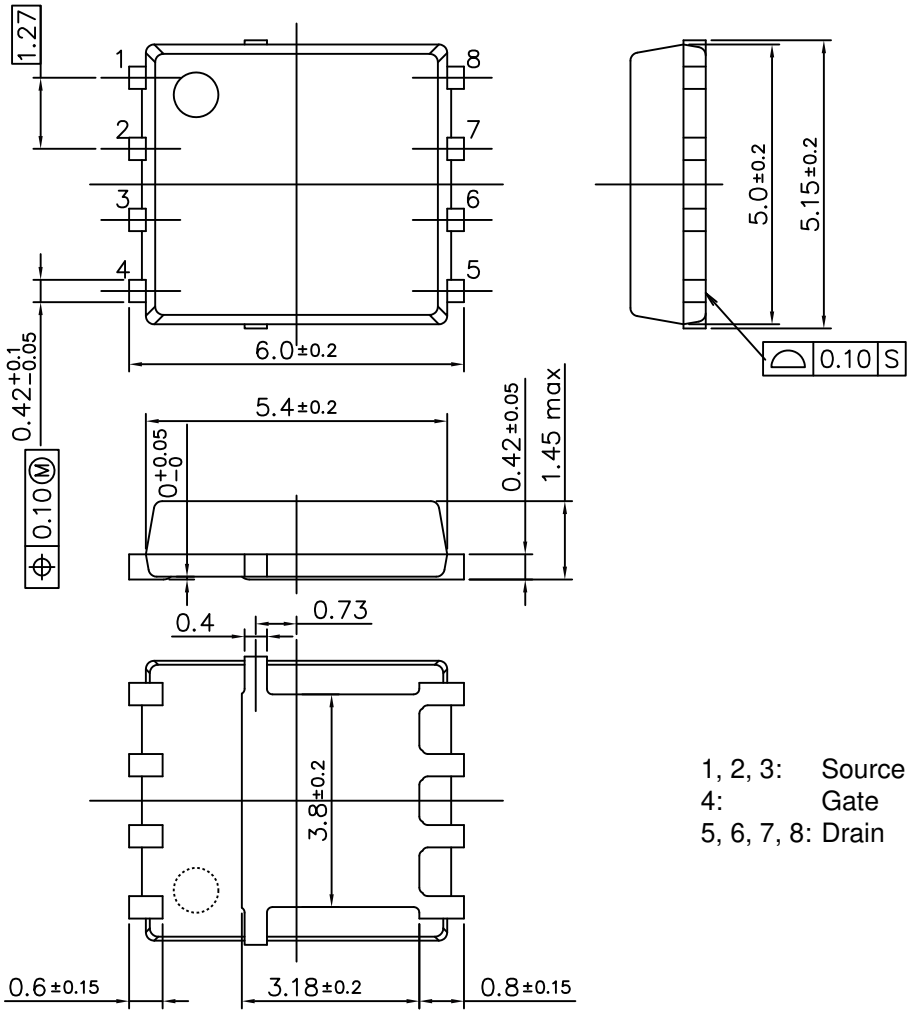


REVERSE RECOVERY TIME vs. DRAIN CURRENT

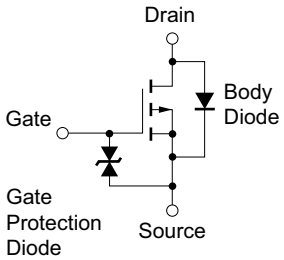


Package Drawings (Unit: mm)

8-pin HSON (Mass: 0.13 g TYP.)



Equivalent Circuit



Remark: The diode connected betweeen the gate and source of the transisor serves as a protector against EDS. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Revision History	NP20P06YLG Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Apr 17, 2012	—	First Edition Issued

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