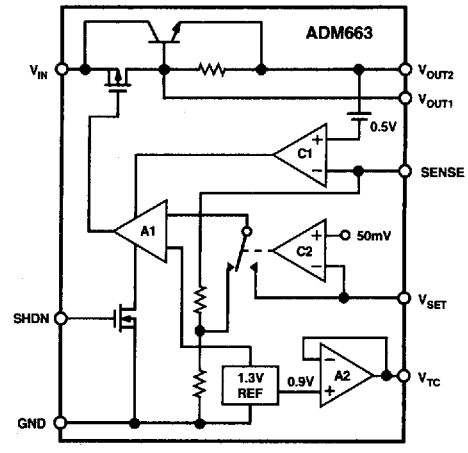
+5 V Fixed, Adjustable Micropower Linear Voltage Regulators

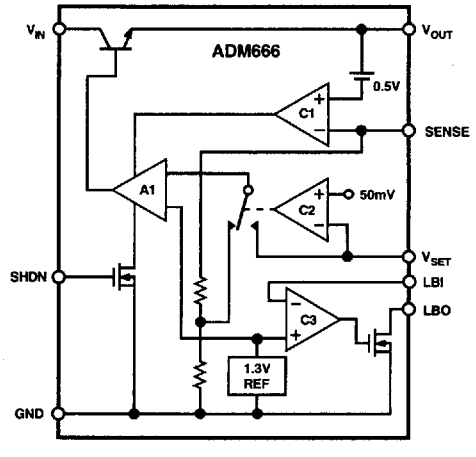
ADM663/ADM666

FEATURES
5 V Fixed or +1.3 V to +16 V Adjustable
Low Power CMOS: 12 μA max Quiescent Current
40 mA Output Current
Current Limiting
Pin Compatible with MAX663/666
+2 V to +16.5 V Operating Range
Low Battery Detector ADM666
No Overshoot on Power-Up

APPLICATIONS
Handheld Instruments
LCD Display Systems
Pagers
Remote Data Acquisition

FUNCTIONAL BLOCK DIAGRAMS





GENERAL DESCRIPTION

The ADM663/ADM666 are precision voltage regulators featuring a maximum quiescent current of 12 μA. They can be used to give a fixed +5 V output with no additional external components or can be adjusted from 1.3 V to 16 V using two external resistors. Fixed or adjustable operation is automatically selected via the V_{SET} input. The low quiescent current makes these devices especially suitable for battery powered systems. The input voltage range is 2 V to 16.5 V and an output current up to 40 mA is provided. The ADM663 can directly drive an external pass transistor for currents in excess of 40 mA. Additional features include current limiting and low power shutdown. Thermal shutdown circuitry is also included for additional safety.

The ADM666 features additional low battery monitoring circuitry to detect for low battery voltages.

The ADM663/ADM666 are pin-compatible replacements for the MAX663/666. Both are available in 8-pin DIP and in narrow surface mount (SOIC) packages.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM663AN	–40°C to +85°C	N-8
ADM663AR	–40°C to +85°C	R-8
ADM666AN	–40°C to +85°C	N-8
ADM666AR	–40°C to +85°C	R-8

*For outline information see Package Information section.

SPECIFICATIONS (V_{IN} = +9 V, V_{OUT} = + 5 V, T_A = + 25°C unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Input Voltage, V_{IN}	2.0		16.5	V	$T_A = T_{MIN}$ to T_{MAX}
Quiescent Current, I_Q					No Load, V_{IN} = +16.5 V
		6	12	µA	T_A = +25°C
			15	µA	$T_A = T_{MIN}$ to T_{MAX}
Output Voltage, V_{OUT}	4.75	5.0	5.25	V	$T_A = T_{MIN}$ to T_{MAX}, V_{SET} = GND
Line Regulation, $\Delta V_{OUT}/\Delta V_{IN}$		0.03	0.35	%/V	+2 V ≤ V_{IN} ≤ +15 V, $V_{OUT} = V_{REF}$
Load Regulation, $\Delta V_{OUT}/\Delta I_{OUT}$		3.0	7.0	Ω	ADM663, 1 mA ≤ I_{OUT2} ≤ 20 mA
		1.0	5.0	Ω	ADM663, 50 µA ≤ I_{OUT1} ≤ 5 mA
		3.0	7.0	Ω	ADM666, 1 mA ≤ I_{OUT} ≤ 20 mA
Reference Voltage, V_{SET}	1.27		1.33	V	$V_{OUT} = V_{SET}$
Reference Tempco, $\Delta V_{SET}/\Delta T$		±100		ppm/°C	$T_A = T_{MIN}$ to T_{MAX}
V_{SET} Internal Threshold, $V_{F/A}$		50		mV	$V_{SET} < V_{F/A}$ for +5 V Out;
					$V_{SET} > V_{F/A}$ for Adj. Out
V_{SET} Input Current, I_{SET}		±0.01	±10	nA	$T_A = T_{MIN}$ to T_{MAX}
Shutdown Input Voltage, V_{SHDN}	1.4			V	V_{SHDN} High = Output Off
			0.3	V	V_{SHDN} Low = Output On
Shutdown Input Current, I_{SHDN}		±0.01	±10	nA	
SENSE Input Threshold, V_{OUT}–V_{SENSE}		0.5		V	Current Limit Threshold
SENSE Input Resistance, R_{SENSE}		3		MΩ	
Input-Output Saturation Resistance, R_{SAT}					
ADM663 V_{OUT1}		200	500	Ω	V_{IN} = +2 V, I_{OUT} = 1 mA
		70	150	Ω	V_{IN} = +9 V, I_{OUT} = 2 mA
		50	150	Ω	V_{IN} = +15 V, I_{OUT} = 5 mA
Output Current from $V_{OUT(2)}$, I_{OUT}	40			mA	+3 V ≤ V_{IN} ≤ +16.5 V, V_{IN}–V_{OUT} = +1.5 V
Minimum Load Current, $I_{L(MIN)}$			1.0	µA	T_A = +25°C
			5.0	µA	$T_A = T_{MIN}$ to T_{MAX}
LBI Input Threshold, V_{LBI}	1.21	1.28	1.37	V	ADM666
LBI Input Current, I_{LBI}		±0.01	±10	nA	ADM666
LBO Output Saturation Resistance, R_{SAT}		35	100	Ω	ADM666, I_{SAT} = 2 mA
LBO Output Leakage Current		10		nA	ADM666, LBI = 1.4 V
V_{TC} Open Circuit Voltage, V_{TC}		0.9		V	ADM663
V_{TC} Sink Current, I_{TC}	2.0	8.0		mA	ADM663
V_{TC} Temperature Coefficient		+2.5		mV/°C	ADM663

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

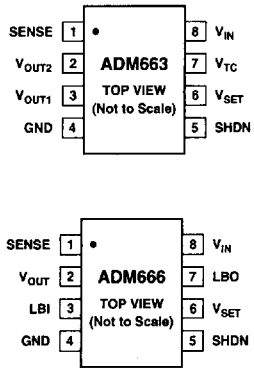
(T_A= +25°C unless otherwise noted)

Input Voltage, V_{IN} ..... +18 V
Terminal Voltage
(ADM663) Pins 1, 3, 5, 6, 7
..... (GND – 0.3 V) to (V_{IN} + 0.3 V)
(ADM666) Pins 1, 2, 3, 5, 6
..... (GND – 0.3 V) to (V_{IN} + 0.3 V)
(ADM663) Pin 2 ..... (GND – 0.3 V) to (V_{OUT1} + 0.3 V)
(ADM666) Pin 7 ..... (GND – 0.3 V) to +16.5 V
Output Source Current
(ADM663, ADM666) Pin 2 ..... 50 mA
(ADM663) Pin 3 ..... 25 mA
Output Sink Current,
(ADM663, ADM666) Pin 7 .....–20 mA

Power Dissipation, N-8 ..... 625 mW
(Derate 8.3 mW/°C above +50°C)
θ_{JA}, Thermal Impedance ..... 120°C/W
Power Dissipation R-8 ..... 450 mW
(Derate 6 mW/°C above +50°C)
θ_{JA}, Thermal Impedance ..... 170°C/W
Operating Temperature Range
Industrial (A Version) .....–40°C to +85°C
Storage Temperature Range .....–65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C
ESD Rating .....>5000 V

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DIP & SOIC PIN CONFIGURATIONS



PIN FUNCTION DESCRIPTION

Mnemonic	Function
$V_{OUT(1)\ (2)}$	Voltage Regulator Output(s)
V_{IN}	Voltage Regulator Input
SENSE	Current Limit Sense Input. (Referenced to $V_{OUT(2)}$.) If not used it should be connected to $V_{OUT(2)}$
GND	Ground Pin. Must be connected to 0 V
LBI	Low Battery Detect Input. Compared with 1.3 V
LBO	Low Battery Detect Output. Open Drain Output
SHDN	Digital Input. May be used to disable the device so that the power consumption is minimized
V_{SET}	Voltage Setting Input. Connect to GND for +5 V output or connect to resistive divider for adjust able output
V_{TC}	Temperature-Proportional Voltage for negative TC Output

GENERAL INFORMATION

The ADM663/ADM666 contains a micropower bandgap reference voltage source, an error amplifier A1, two comparators C1, C2 and a series pass output transistor. A P-channel FET and an NPN transistor are used on the ADM663 while the ADM666 uses an NPN output transistor.

CIRCUIT DESCRIPTION

The internal bandgap reference is trimmed to 1.3 V ± 30 mV. This is used as a reference input to the error amplifier A1. The feedback signal from the regulator output is supplied to the other input by an on-chip voltage divider or by two external resistors. When V_{SET} is at ground, the internal divider provides the error amplifier's feedback signal giving a +5 V output. When V_{SET} is at more than 50 mV above ground, the error amplifier's input is switched directly to the V_{SET} pin, and external resistors are used to set the output voltage. The external resistors are selected so that the desired output voltage gives 1.3 V at V_{SET}.

Comparator C1 monitors the output current via the SENSE input. This input, referenced to $V_{OUT(2)}$, monitors the voltage drop across a load sense resistor. If the voltage drop exceeds 0.5 V, then the error amplifier A_1 is disabled and the output current is limited.

The ADM663 has an additional amplifier, A2, which provides a temperature-proportional output, V_{TC}. If this is summed into the inverting input of the error amplifier, a negative temperature coefficient results at the output. This is useful when powering liquid crystal displays over wide temperature ranges.

The ADM666 has an additional comparator, C3 which compares the voltage on the Low Battery Input, LBI, pin to the internal +1.3 V reference. The output from the comparator drives an open drain FET connected to the Low Battery Output pin, LBO. The Low Battery Threshold may be set using a suitable voltage divider connected to LBI. When the voltage on LBI falls below 1.3 V, the open drain output LBO is pulled low.

Both the ADM663 and the ADM666 contain a shutdown (SHDN) input which can be used to disable the error amplifier and hence the voltage output. The quiescent current in shutdown is less than 12 µA.

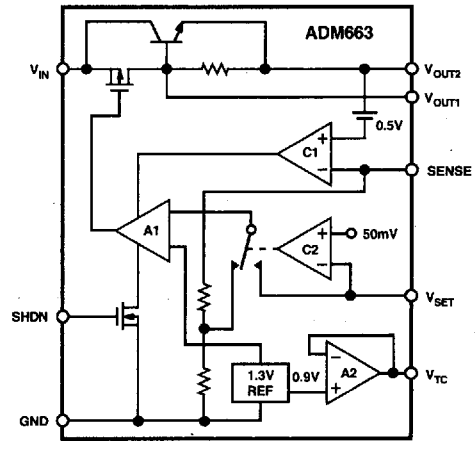


Figure 1. ADM663 Functional Block Diagram

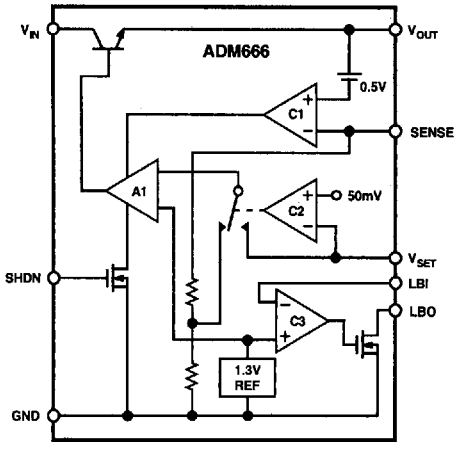


Figure 2. ADM666 Functional Block Diagram

Circuit Configurations

For a fixed +5 V output the V_{SET} input is grounded and no external resistors are necessary. This basic configuration is shown in Figure 3. Current limiting is not being utilized so the SENSE input is connected to $V_{OUT(2)}$. The input voltage can range from +6 V to +16 V and output currents up to 40 mA are available provided that the maximum package power dissipation is not exceeded.

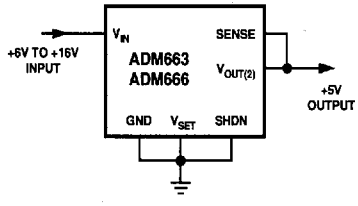


Figure 3. ADM663/ADM666 Fixed +5 V Output

Output Voltage Setting

If V_{SET} is not connected to GND, the output voltage is set according to the following equation.

$$V_{OUT} = V_{SET} \times \frac{R1 + R2}{R1} \quad where\ V_{SET} = 1.30\,V$$

The resistor values may be selected by firstly choosing a value for R1 and then selecting R2 according to the following equation.

$$R2 = R1 \times \left(\frac{V_{OUT}}{1.30} - 1 \right)$$

The input leakage current on V_{SET} is 10 nA maximum. This allows large resistor values to be chosen for R1 and R2 with little degradation in accuracy. For example, a 1 MΩ resistor may be selected for R1 and then R2 may be calculated accordingly. The tolerance on V_{SET} is guaranteed at less than ±30 mV so in most applications, fixed resistors will be suitable.

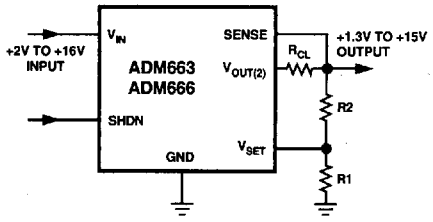


Figure 4. ADM663/ADM666 Adjustable Output

Current Limiting

Current limiting may be achieved by using an external current sense resistor in series with $V_{OUT(2)}$. When the voltage across the sense resistor exceeds the internal 0.5 V threshold, current limiting is activated. The sense resistor is therefore chosen such that the voltage across it will be 0.5 V when the desired current limit is reached.

$$R_{CL} = \frac{0.5}{I_{CL}}$$

where R_{CL} is the current sense resistor, I_{CL} is the maximum current limit.

The value chosen for R_{CL} should also ensure that the current is limited to less than the 50 mA absolute maximum rating and also that the power dissipation will also be within the package maximum ratings.

If current limiting is employed, there will be an additional voltage drop across the sense resistor which must be considered when determining the regulators dropout voltage.

If current limiting is not used, the SENSE input should be connected to $V_{OUT(2)}$.

Shutdown Input (SHDN)

The SHDN input allows the regulator to be switched off with a logic level signal. This will disable the output and reduce the current drain to a low quiescent (12 µA maximum) current. This is very useful for low power applications. The SHDN input should be driven with a CMOS logic level signal since the input threshold is 0.3 V. In TTL systems, an open collector driver with a pull-up resistor may be used.

If the shutdown function is not being used, then SHDN should be connected to GND.

Low Supply or Low Battery Detection

The ADM666 contains on-chip circuitry for low power supply or battery detection. If the voltage on the LBI pin falls below the internal 1.3 V reference, then the open drain output LBO will go low. The low threshold voltage may be set to any voltage above 1.3 V by appropriate resistor divider selection.

$$R3 = R4 \times \left(\frac{V_{BATT}}{1.30} - 1 \right)$$

where R3 and R4 are the resistive divider resistors and V_{BATT} is the desired low voltage threshold.

Since the LBI input leakage current is less than 10 nA, large values may be selected for R3 and R4 in order to minimize loading. For example, a 6 V low threshold, may be set using 10 MΩ for R3 and 2.7 MΩ for R4.

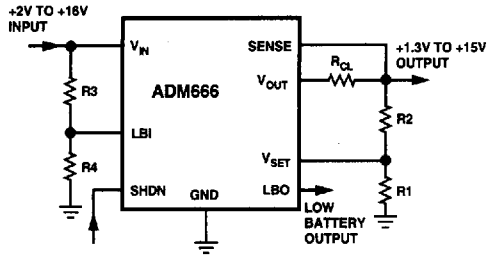


Figure 5. ADM666 Adjustable Output with Low Battery Detection

High Current Operation

The ADM663 contains an additional output, V_{OUT1}, suitable for directly driving the base of an external NPN transistor. Figure 6 shows a configuration which can be used to provide +5 V with boosted current drive. A 1 Ω current sensing resistor limits the current at 0.5 A.

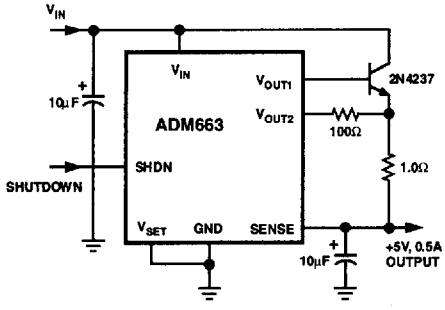


Figure 6. ADM663 Boosted Output Current (0.5 A)

Temperature Proportional Output

The ADM663 contains a V_{TC} output with a positive temperature coefficient of +2.5 mV/°C. This may be connected to the summing junction of the error amplifier (V_{SET}) through a resistor resulting in a negative temperature coefficient at the output of the regulator.

This is especially useful in multiplexed LCD displays to compensate for the inherent negative temperature coefficient of the LCD threshold. At 25°C the voltage at the VTC output is typically 0.9 V. The equations for setting both the output voltage and the tempco are given below. If this function is not being used, then V_{TC} should be left unconnected.

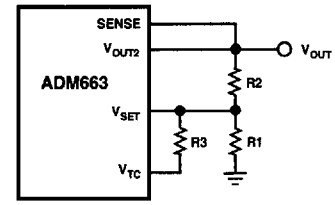


Figure 7. ADM663 Temperature Proportional Output

$$V_{OUT} = V_{SET} \times \left(1 + \frac{R2}{R1}\right) + \frac{R2}{R3} \times \left(V_{SET} - V_{TC}\right)$$

$$TCV_{OUT} = \frac{-R2}{R3} \times TVC_{TC}$$

where $V_{SET} = +1.3V$, $V_{TC} = +0.9V$, $TCV_{TC} = +2.5\,mV/°C$

APPLICATION HINTS

Input-Output (Dropout Voltage)

A regulator's minimum input-output differential or dropout voltage determines the lowest input voltage for a particular output voltage. The ADM663/ADM666 dropout voltage is 0.8 V at its rated output current. For example when used as a fixed +5 V regulator the minimum input voltage is +5.8 V. At lower output currents, (I_{OUT} < 5 mA), on the ADM663, V_{OUT1} may be used as the output driver in order to achieve lower dropout voltages. Please refer to Figure 9. In this case the dropout voltage depends on the voltage drop across the internal FET transistor. This may be calculated by multiplying the FET's saturation resistance by the output current. As the current limit circuitry is referenced to V_{OUT2}, V_{OUT2} should be connected to V_{OUT1}. For high current operation V_{OUT2} should be used alone and V_{OUT1} left unconnected.

Bypass Capacitors

The high frequency performance of the ADM663/ADM666 may be improved by decoupling the output using a filter capacitor. A capacitor value of 10 µF is suitable.

An input capacitor helps reduce noise and improves dynamic performance. A suitable input capacitor of 0.1 µF or greater may be used.

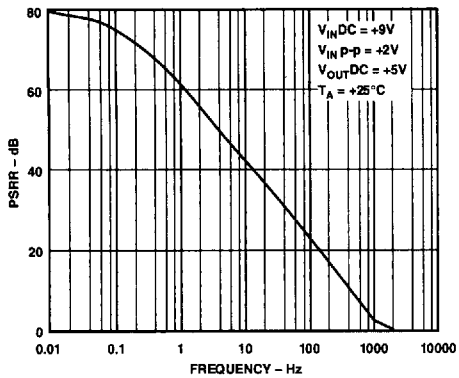


Figure 8. Power Supply Rejection Ratio vs. Frequency

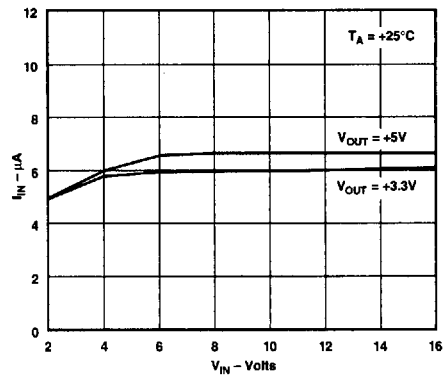


Figure 10. Quiescent Current vs. Input Voltage

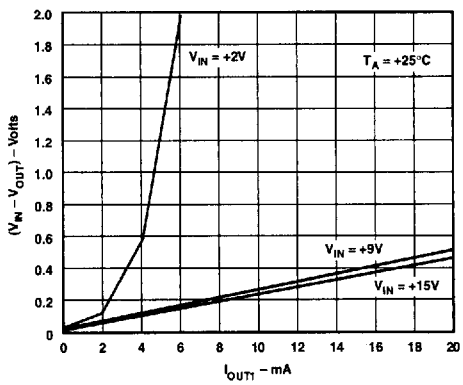


Figure 9. V_{OUT1} Input-Output Differential vs. Output Current

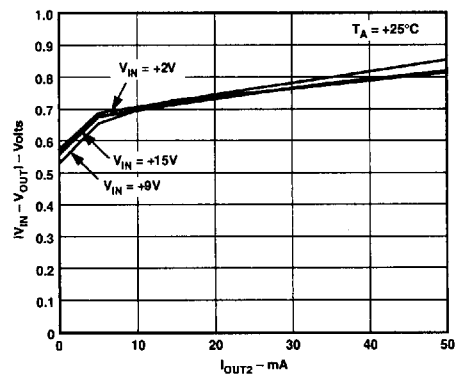


Figure 11. $V_{OUT(2)}$ Input-Output Differential vs. Output Current

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