

BAT15-02ELS

Single silicon RF Schottky diode



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Technical documents



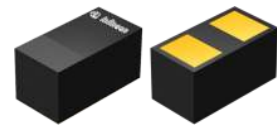
Simulation



Support

Product description

This Infineon RF Schottky diode is a silicon low barrier N-type device with an integrated guard ring on-chip for over-voltage protection. Its low barrier height, low forward voltage and low junction capacitance make BAT15-02ELS a suitable choice for mixer and detector functions in applications which frequencies are as high as 12 GHz.



Feature list

- Low inductance $L_S = 0.2$ nH (typical)
- Low capacitance $C = 0.2$ pF (typical) at voltage $V_R = 0$ V and frequency $f = 1$ MHz
- TSSLP-2-3 package (0.62 mm x 0.32 mm x 0.31 mm) with a 0201 foot print
- Pb-free, RoHS compliant and halogen free

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Potential applications

For mixers and detectors in:

- Mobile devices
- Modules and embedded systems

Device information

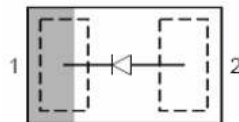


Table 1 Part information

Product name / Ordering code	Package	Pin configuration	Marking	Pieces / Reel
BAT15-02ELS / BAT1502ELSE6327XTSA1	TSSLP-2-3	Single, leadless	S underscore	15 k
BAT15-02ELS / BAT1502ELSE6433XTMA1				70 k

Attention: ESD (Electrostatic discharge) sensitive device, observe handling precautions!

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1 Absolute maximum ratings

Table 2 Absolute maximum ratings at $T_A=25^{\circ}\text{C}$, unless otherwise specified

Parameter	Symbol	Values		Unit	Note or test condition
		Min.	Max.		
Diode reverse voltage	V_R	-	4	V	
Forward current	I_F	-	110	mA	
Total power dissipation	P_{TOT}	-	100	mW	$T_S \leq 82^{\circ}\text{C}$ ¹⁾
Junction temperature	T_J	-	150	°C	
Operating temperature	T_{OP}	-55	150		
Storage temperature	T_{STG}	-55	150		

Attention: *Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding only one of these values may cause irreversible damage to the component.*

¹ T_S is the soldering point temperature.

Electrical performance in test fixture

2 Electrical performance in test fixture

2.1 Electrical characteristics

Table 3 Electrical characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Breakdown voltage	V_{BR}	4	–	–	V	$I_R = 100\text{ }\mu\text{A}$
Reverse current	I_R	–	–	5	μA	$V_R = 1\text{ V}$
Forward voltage	V_F	0.16	0.25	0.32	V	$I_F = 1\text{ mA}$
		0.25	0.35	0.41		$I_F = 10\text{ mA}$
Differential forward resistance	R_F	–	8	10	Ω	$I_F = 10\text{ mA} / 50\text{ mA}$ ¹⁾
Capacitance	C	–	0.2	0.23	pF	$V_R = 0\text{ V}, f = 1\text{ MHz}$
Inductance	L_S	–	0.2	–	nH	

2.2 Characteristic curves

At $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

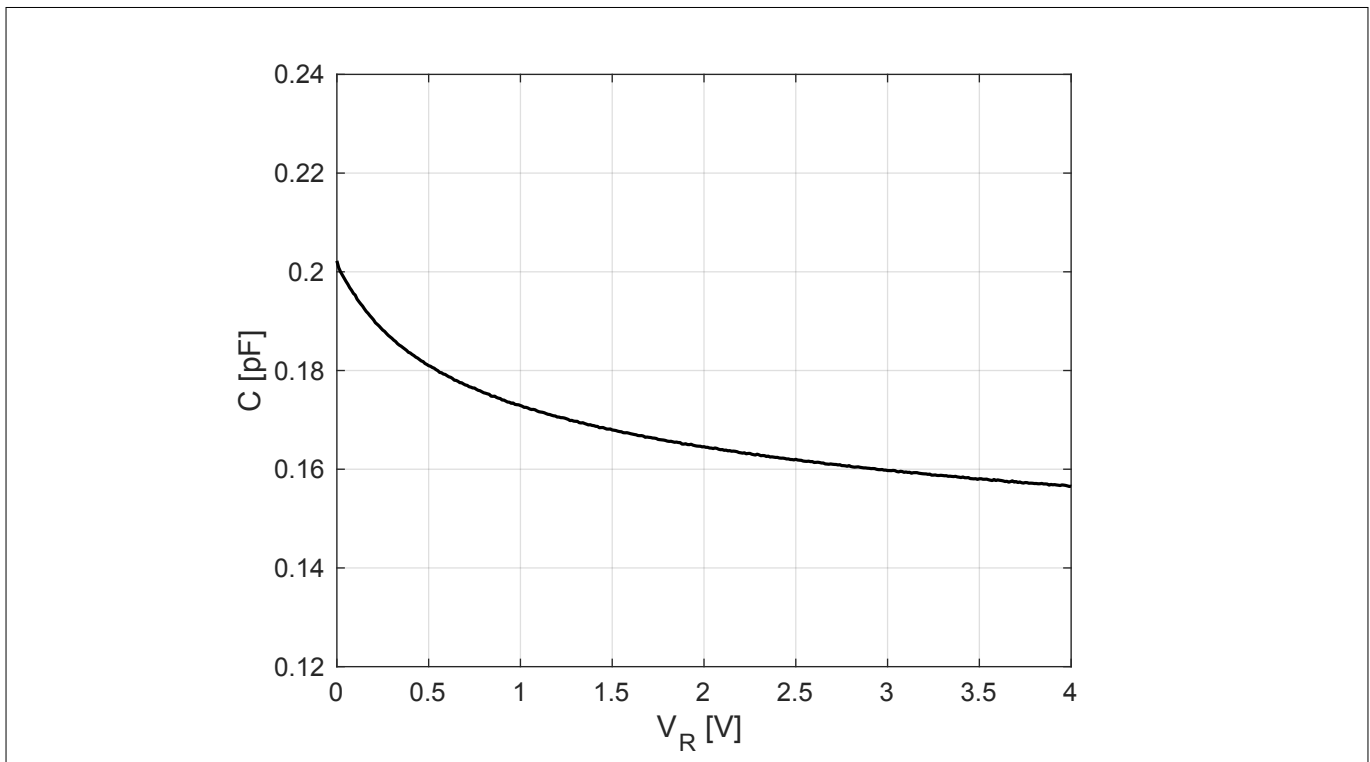


Figure 1 Capacitance C vs. reverse voltage V_R at frequency $f = 1\text{ MHz}$

¹
$$R_F = \frac{V_F(50\text{ mA}) - V_F(10\text{ mA})}{50\text{ mA} - 10\text{ mA}}$$

Electrical performance in test fixture

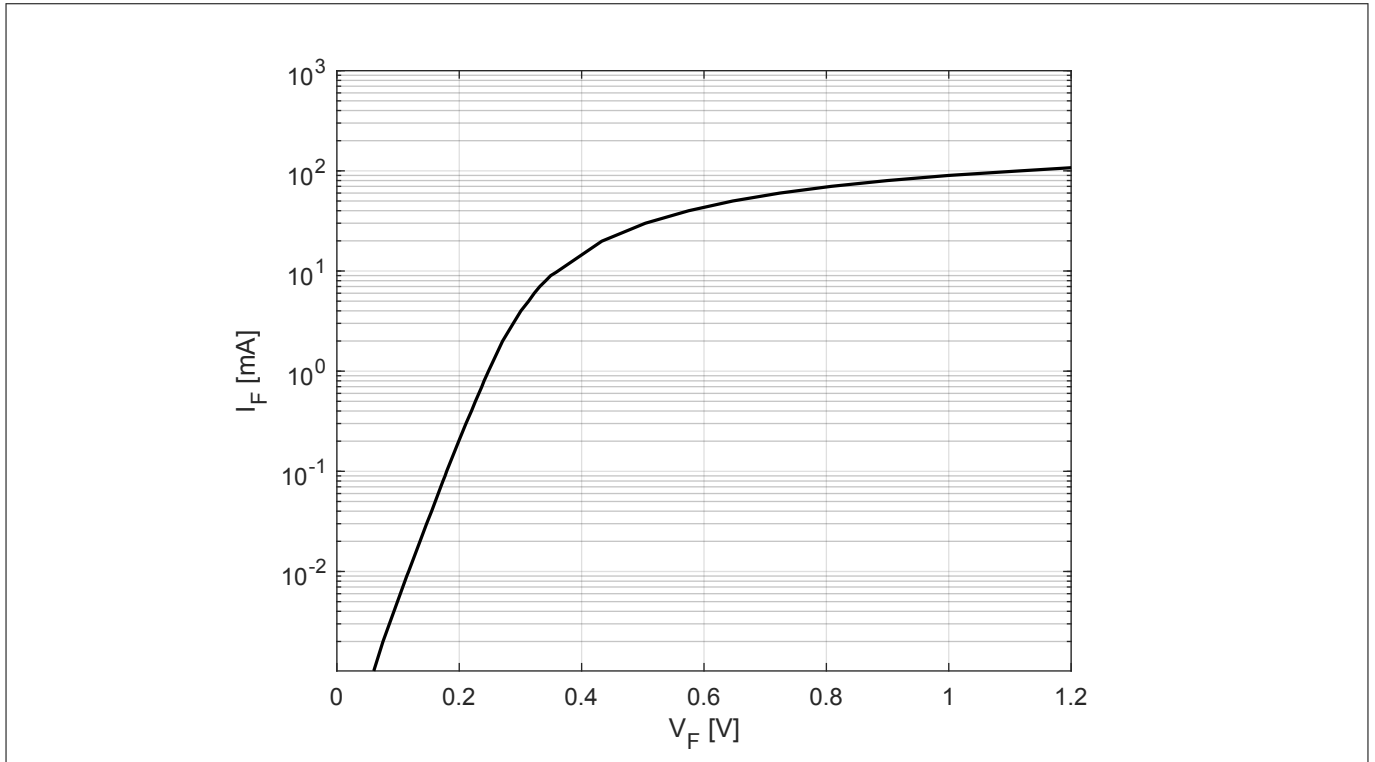


Figure 2 Forward current I_F vs. forward voltage V_F

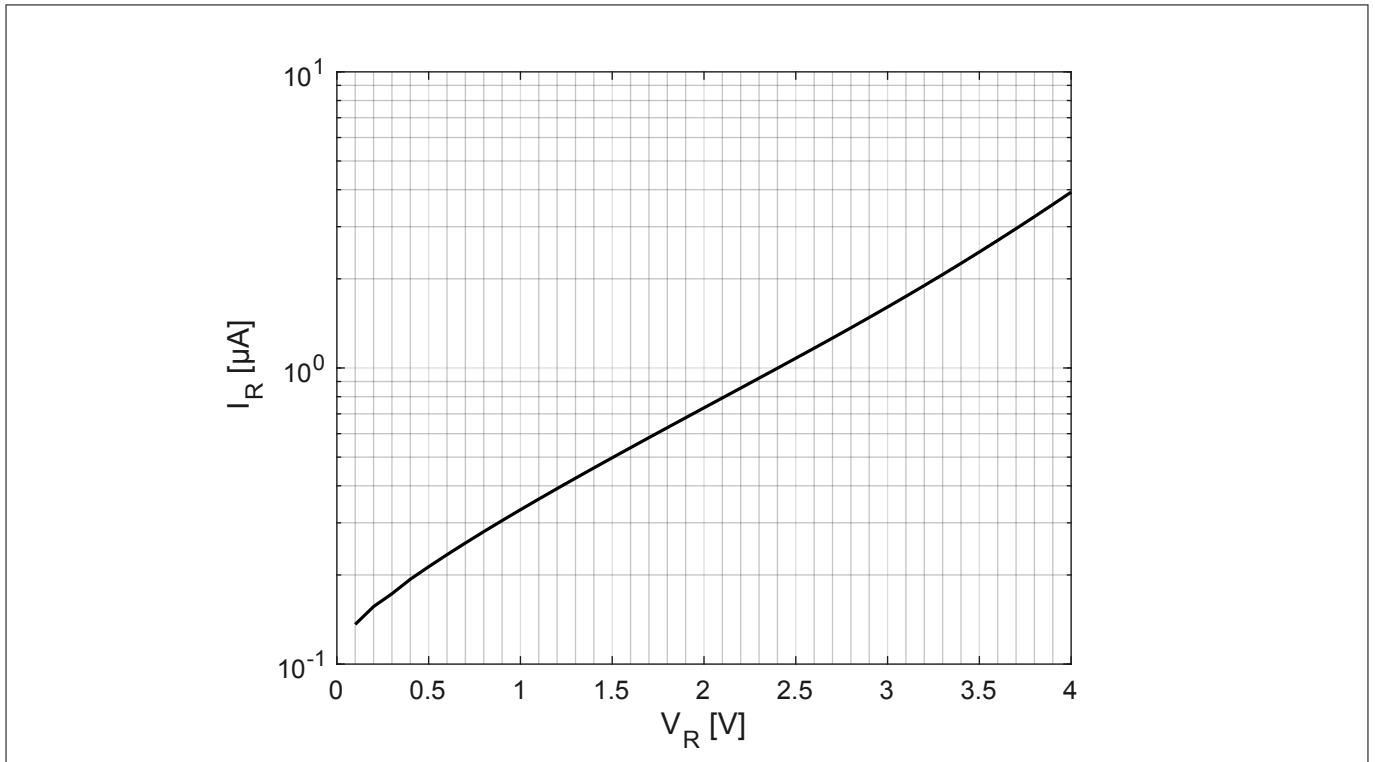


Figure 3 Reverse current I_R vs. reverse voltage V_R

Note: The curves shown in this chapter have been generated using typical devices but shall not be understood as a guarantee that all devices have identical characteristic curves.

Thermal characteristics

3 Thermal characteristics

Table 4 Thermal resistance

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Thermal resistance (junction - soldering point)	R_{thJS}	-	675	-	K/W	$T_S = 82\text{ °C}$ ¹⁾

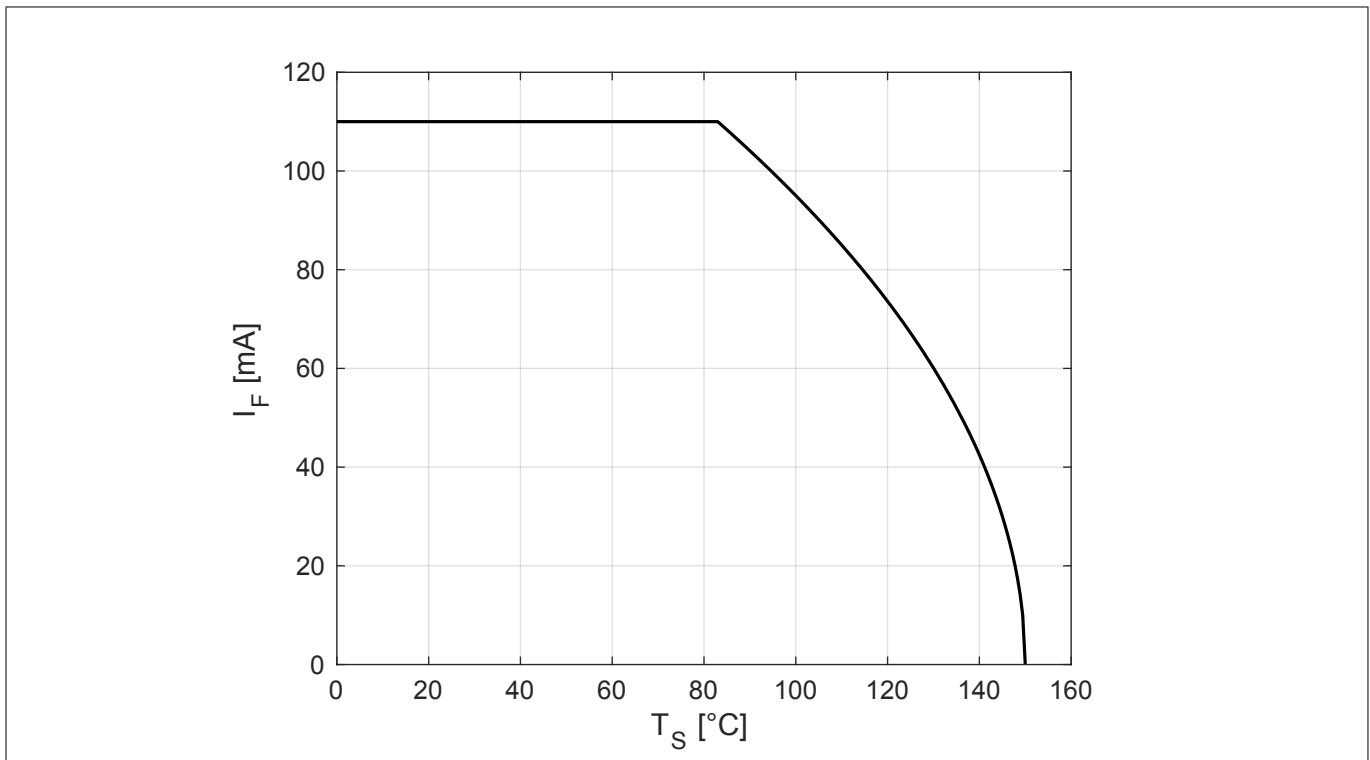


Figure 4 Permissible forward current I_F in DC operation

¹ For R_{thJS} in other conditions refer to the curves in this chapter.

Thermal characteristics

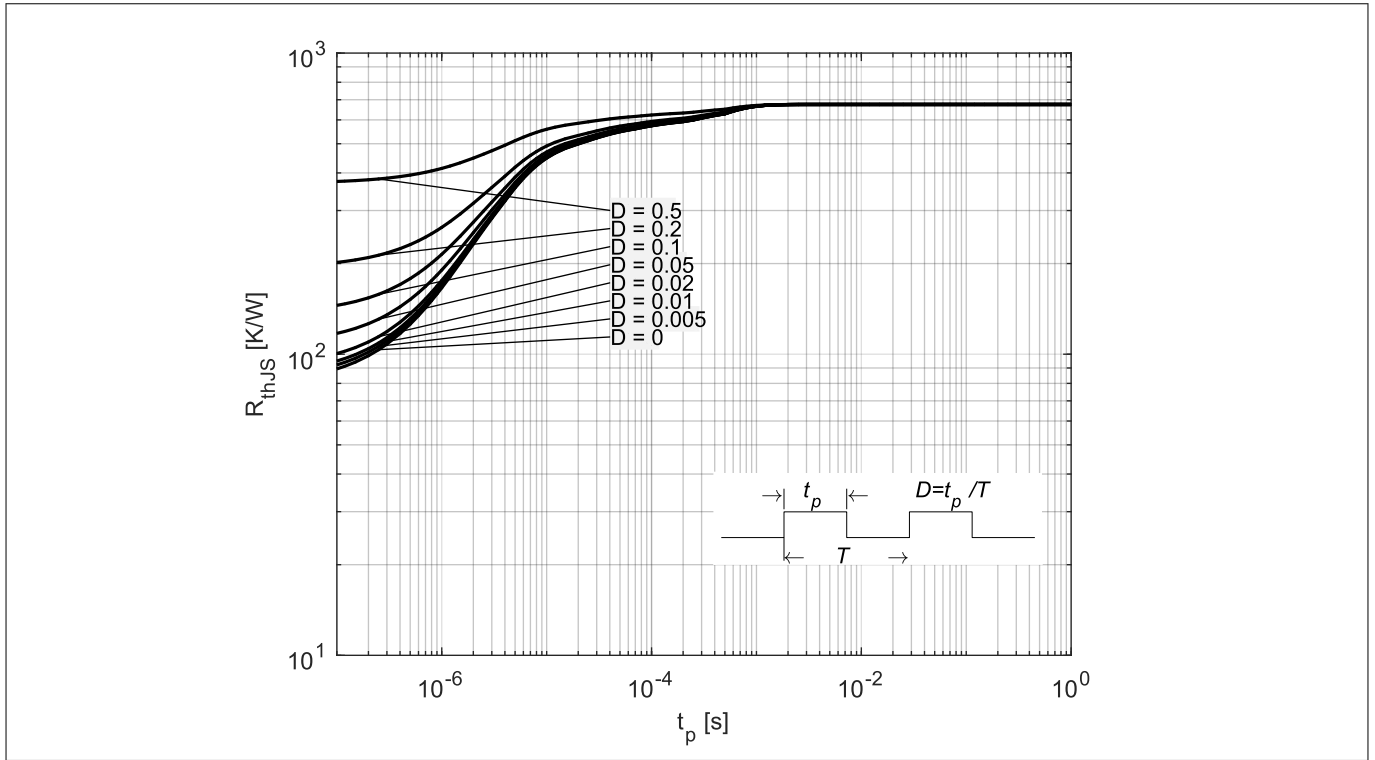


Figure 5 Thermal resistance R_{thJS} in pulse operation

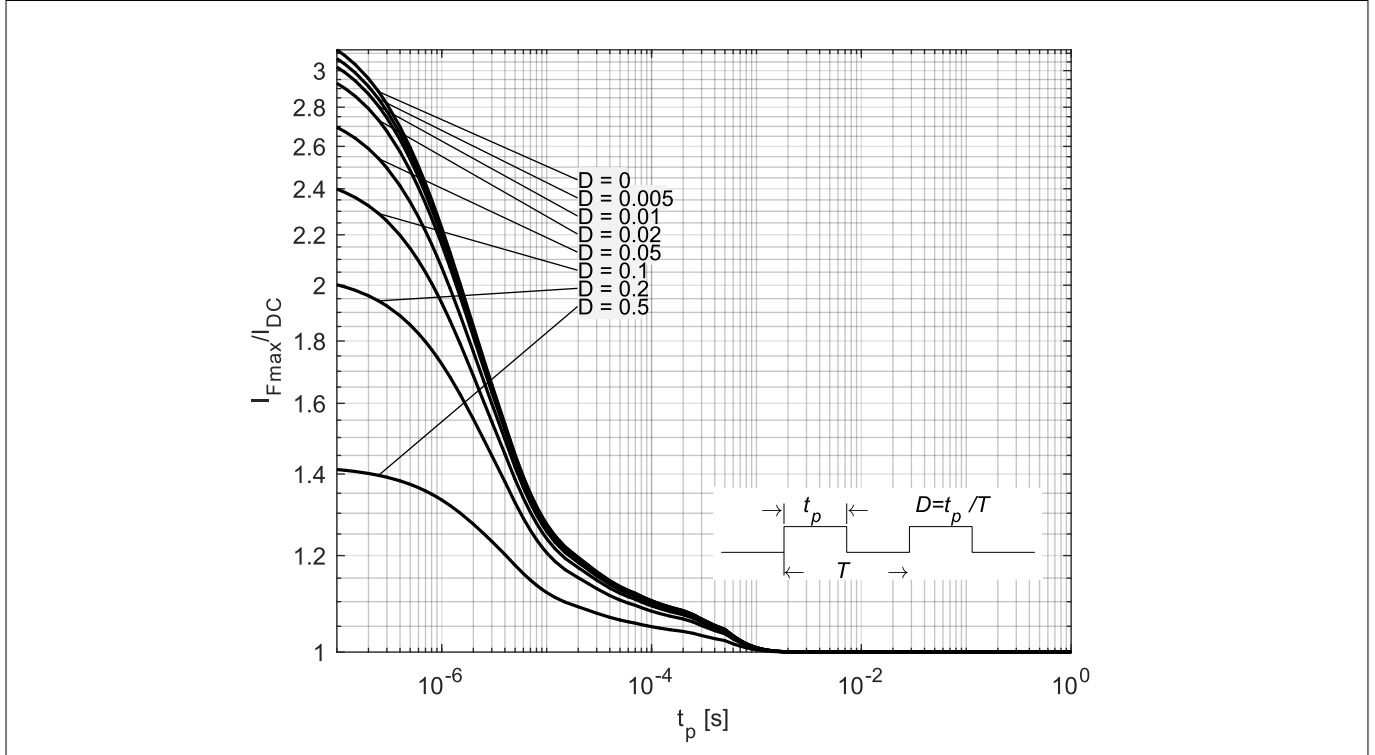


Figure 6 Permissible forward current ratio I_{Fmax}/I_{DC} in pulse operation

Package information TSSLP-2-3

4 Package information TSSLP-2-3

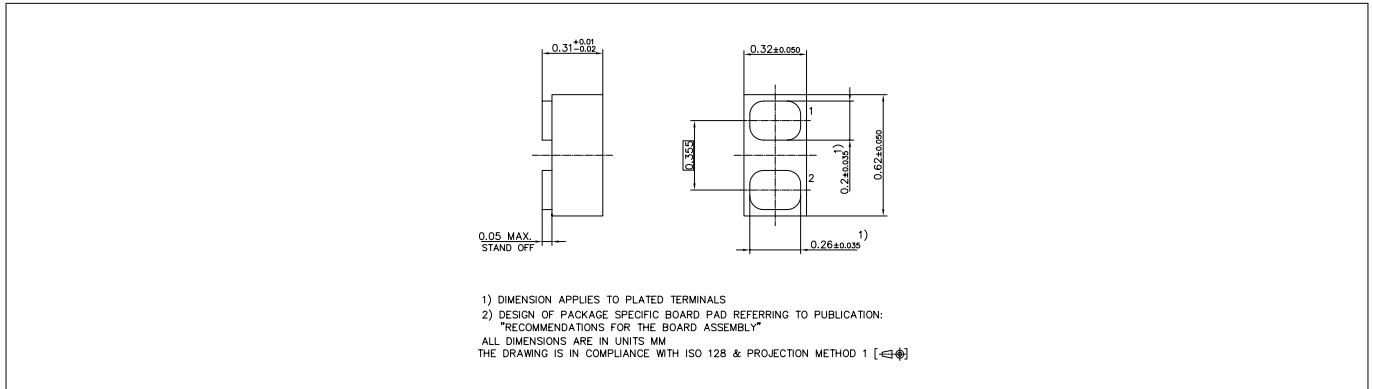


Figure 7 Package outline

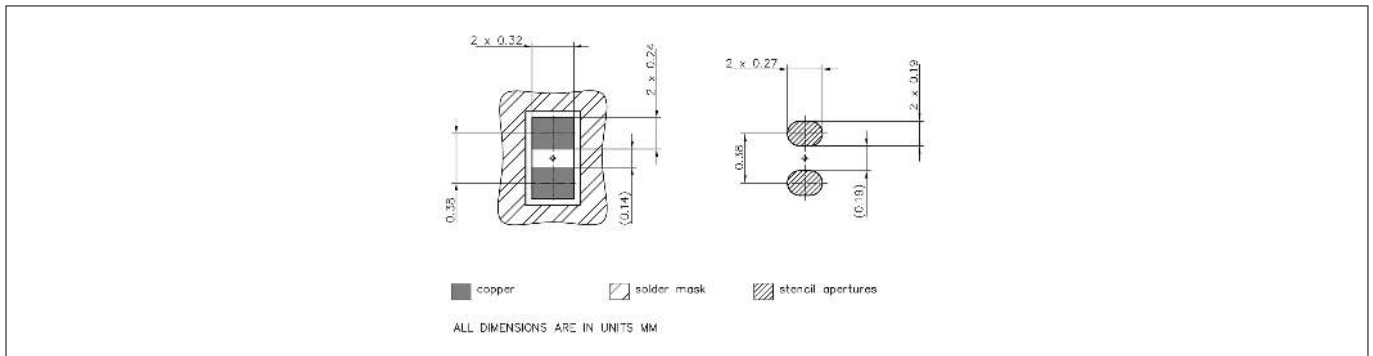


Figure 8 Foot print

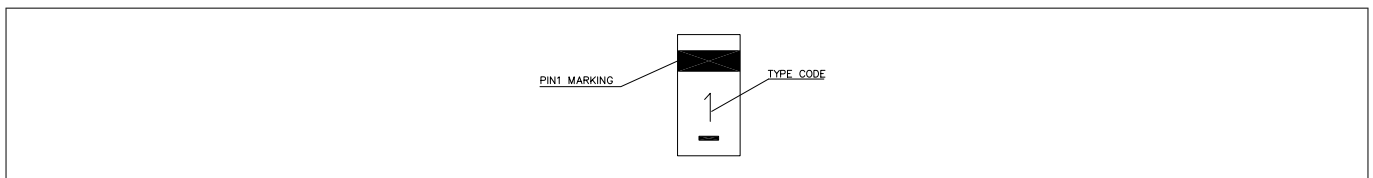


Figure 9 Marking layout example

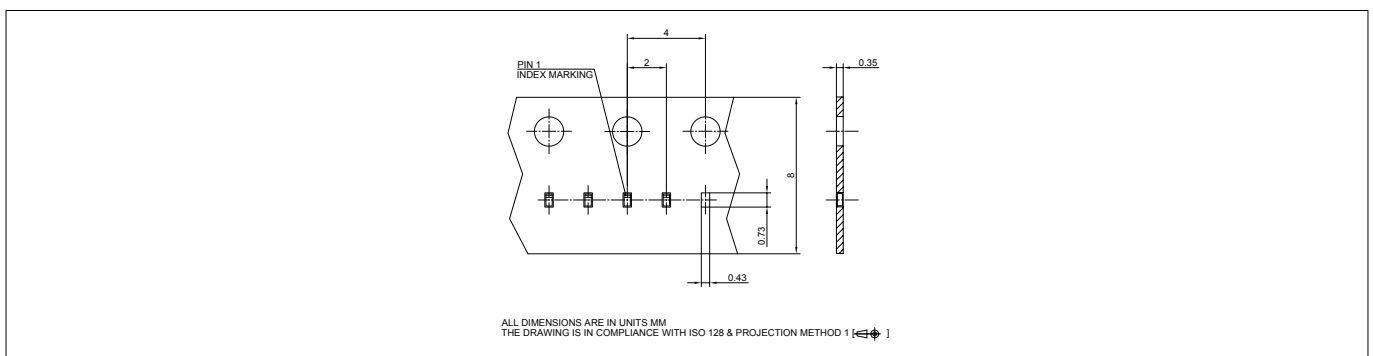


Figure 10 Tape dimensions

Note: See our [Recommendations for Printed Circuit Board Assembly of TSLP/TSSLP/TSNP Packages](#). The marking layout is an example. For the real marking code refer to the device information on the first page. The number of characters shown in the layout example is not necessarily the real one. The marking layout can consist of less characters.

References

5 References

[1]	Infineon AG - <i>Recommendations for Printed Circuit Board Assembly of Infineon TSLP/TSSLP/TSNP Packages</i>
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Revision history

Document version	Date of release	Description of changes
1.0	2018-09-07	<ul style="list-style-type: none">• Change from series datasheet to individual one• Initial release of datasheet• Typical values and curves updated to the values of the production (No product or process change behind)• Maximum/typical values added• Typical curves removed

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