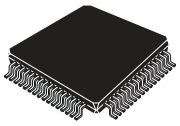
STLC5046

Programmable four channel CODEC and filter

Features

- Programmable monolithic 4 channel
- CODEC/Filter
- Single +3.3 V supply
- Pin-strap / MCU control mode
- A/µ Law programmable
- Linear coding (16 bits) option
- PCM highway format automatically detected: 1.536 or 1.544 MHz; 2.048, 4.096, 8192 MHz
- TX gain programming: 16 dB range; <0.1 dB step
- RX gain programming: 26 dB range; <0.1 dB step
- Programmable time slot assignment
- Digital and analog loopbacks
- SLIC control port
- Static mode (16 I/Os)
- Dynamic mode (12 I/Os + 4 CS)
- LQFP64 package
- PCM in HI-Z mode



LQFP64

Description

The STLC5046 is a monolithic programmable 4 channel codec and filter. It operates with a single +3.3 V supply.

The analog interface is based on a receive output buffer driving the SLIC RX input and on an amplifier input stage.

Due to the single supply voltage a proper mid supply reference level is generated internally by the device and all analog signals are referred to this level (AGND).

The PCM interface uses one common 8 kHz frame sync. pulse for transmit and receive direction. The bit clock can be selected between four standards: 1.536/1.544 MHz, 2.048 MHz, 4.096 MHz, 8192 MHz. Device programmability is achieved by means of 41 registers allowing to set the different parameters like TX/RX gains, encoding Law (A/µ), time slot assignment, independent channels power up/down, loopbacks, PCM bits offset.

Thanks to pin-strap option, the most significant of the above parameters can be set by hardware connection of dedicated pins. This allow to use this device also on line card without MCU on board. When pin-strap option is selected different pins of the device will change their function (see pin description).

In MCU control mode the STLC5046 can be programmed via serial interface running up to 4 MHz.

One interrupt output pin is also provided.

Table 1. Device summary

Order code	Temperature range	Package	Packing
E-STLC5046(1)	-40°C to +85°C	LQFP64	Tube

1. ECOPACK® (see *Section 7*)

Contents

List of tables

List of figures

1 Block diagram and pin connection

Figure 1. Block diagram

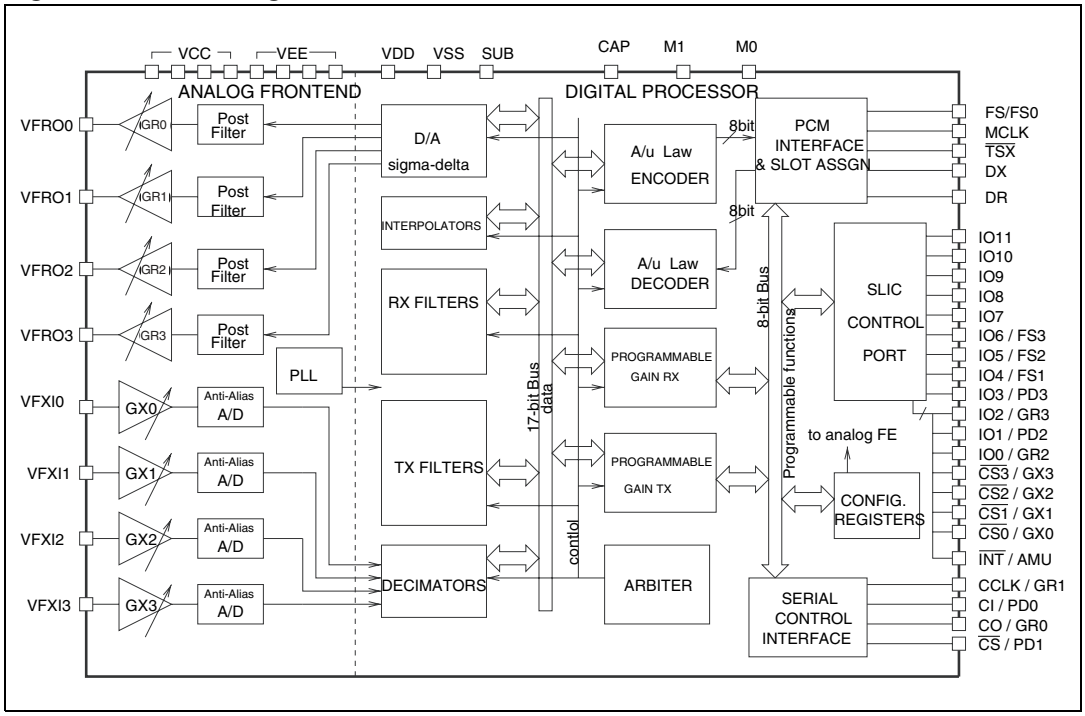
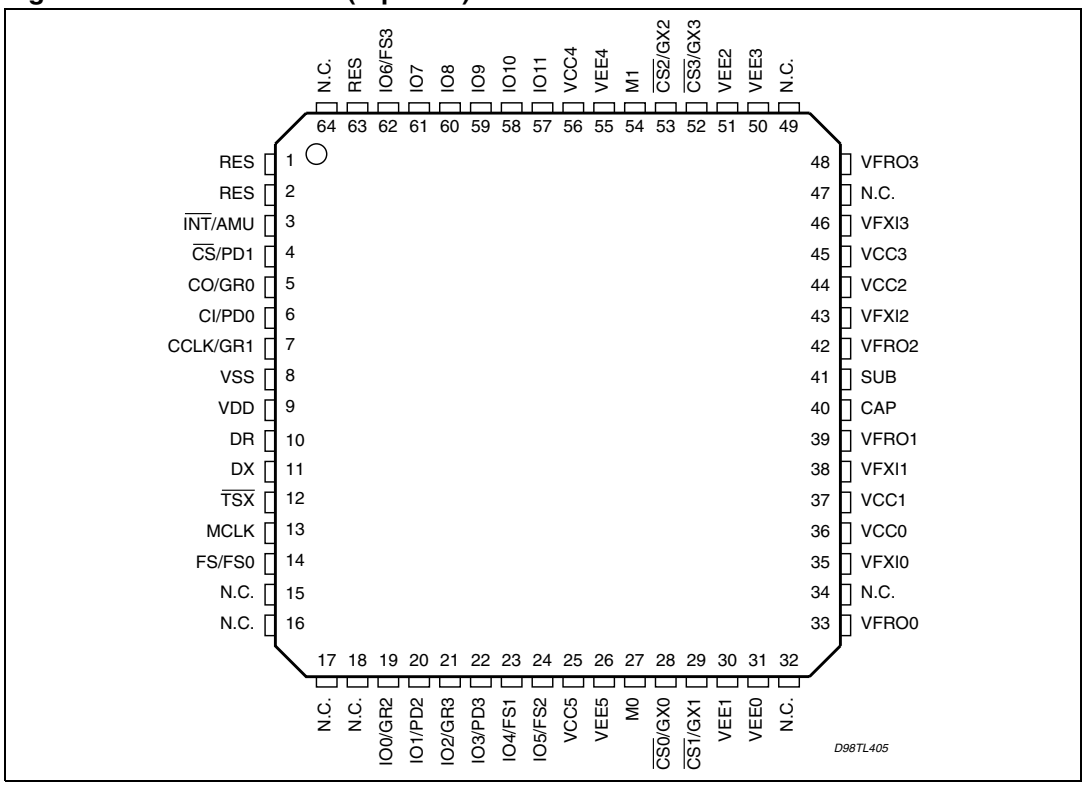


Figure 2. Pin connection (top view)



1.1 Pin description

Table 2. I/O definition

Type	Definition
AI	Analog input
AO	Analog output
ODO	Open drain output
DI	Digital input
DO	Digital output
DIO	Digital input/output
DTO	Digital tristate output
DPS	Digital power supply
APS	Analog power supply

Table 3. Pin description

N.	Name	Type	Function
Analog			
33	VFRO0	AO	Receive analog amplifier output channel 0. PCM data received on the programmed time slot on DR input is decoded and appears at this output.
39	VFRO1	AO	Receive analog amplifier output channel 1. PCM data received on the programmed time slot on DR input is decoded and appears at this output.
42	VFRO2	AO	Receive analog amplifier output channel 2. PCM data received on the programmed time slot on DR input is decoded and appears at this output.
48	VFRO3	AO	Receive analog amplifier output channel 3. PCM data received on the programmed time slot on DR input is decoded and appears at this output.
35	VFXI0	AI	TX Input amplifier channel 0. Typ 1M.input impedance
38	VFXI1	AI	TX Input amplifier channel 1. Typ 1M.input impedance
43	VFXI2	AI	TX Input amplifier channel 2. Typ 1M.input impedance
46	VFXI3	AI	TX Input amplifier channel 3. Typ 1M.input impedance
40	CAP	AI	AGND voltage filter pin. A 100nF capacitor must be connected between ground and this pin.
Power supply			
25, 36, 37, 44, 45, 56,	VCC/0/1/2 /3/ 4/5	APS	Total 6 pins: 3.3 V analog power supplies, should be shorted together, require 100nF decoupling capacitor to VEE.
26,30, 31, 50, 51,55	VEE/0/1/2 /3/ 4/5	APS	Total 6 pins: analog ground, should be shorted together.
9	VDD	DPS	Digital power supply 3.3 V, require 100 nF decoupling capacitor to VSS.
8	VSS	DPS	Digital ground

Table 3. Pin description (continued)

<table>
<tr><th>N.</th><th>Name</th><th>Type</th><th>Function</th></tr>
<tr><td>41</td><td>SUB</td><td>DPS</td><td>Substrate connection. Must be shorted together with VEE and VSS pins as close as possible the chip.</td></tr>
<tr><td colspan="4">Not connected</td></tr>
<tr><td>15, 16, 17, 18, 32, 34, 47, 49, 64</td><td>N.C.</td><td></td><td>Not connected.</td></tr>
<tr><td>1,2,63</td><td>RES</td><td></td><td>Reserved: must be left not connected.</td></tr>
<tr><td colspan="4">Digital</td></tr>
<tr><td>27</td><td>M0</td><td>DI</td><td>Mode select, see M1</td></tr>
<tr><td>54</td><td>M1</td><td>DI</td><td>
<table>
<tr><th>M1</th><th>M0</th><th>Mode select</th></tr>
<tr><td>0</td><td>1</td><td>Pin-strap mode: basic functions selected by proper pin strapping</td></tr>
<tr><td>1</td><td>0</td><td>MCU mode: device controlled via serial interface</td></tr>
<tr><td>0</td><td>0</td><td>Reset status</td></tr>
<tr><td>1</td><td>1</td><td>Not allowed</td></tr>
</table>
</td></tr>
<tr><td>13</td><td>MCLK</td><td>DI</td><td>Master clock input. Four possible frequencies can be used: 1.536/1.544 MHz; 2.048 MHz; 4.096 MHz; 8.192 MHz. The device automatically detect the frequency applied. This signal is also used as bit clock and it is used to shift data into and out of the DR and DX pins.</td></tr>
<tr><td>12</td><td>$\overline{\text{TSX}}$</td><td>ODO</td><td>Transmit time slot (open drain output, 3.2mA). Normally it is floating in high impedance state except when a time slot is active on the DX output. In this case $\overline{\text{TSX}}$ output pulls low to enable the backplane line driver.</td></tr>
<tr><td>11</td><td>DX</td><td>DTO</td><td>Transmit PCM interface. It remains in high impedance state except during the assigned time slots during which the PCM data byte is shifted out on the rising edge of MCLK.</td></tr>
<tr><td>10</td><td>DR</td><td>DI</td><td>Receive PCM interface. It remains inactive except during the assigned receive time slots during which the PCM data byte is shifted in on the falling edge of MCLK.</td></tr>
<tr><td>61</td><td>IO7</td><td>DIO</td><td>SLIC control I/O pin #7. Can be programmed as input or output via DIR register. Depending on content of CONF register can be a static input/output or a dynamic input/output synchronized with the $\overline{\text{CSn}}$ output signals controlling the SLICs.</td></tr>
<tr><td>60</td><td>IO8</td><td>DIO</td><td>SLIC control I/O pin #8. (see IO7 description).</td></tr>
<tr><td>59</td><td>IO9</td><td>DIO</td><td>SLIC control I/O pin #9. (see IO7 description).</td></tr>
<tr><td>58</td><td>IO10</td><td>DIO</td><td>SLIC control I/O pin #10. (see IO7 description).</td></tr>
<tr><td>57</td><td>IO11</td><td>DIO</td><td>SLIC control I/O pin #11. (see IO7 description).</td></tr>
<tr><td colspan="4">Digital (dual mode)</td></tr>
</table>

Table 3. Pin description (continued)

N.	Name	Type	Function
14	FS/FS0	DI	MCU control mode: FS. Frame Sync. Pulse. A pulse or a square wave waveform with an 8kHz repetition rate is applied to this pin to define the start of the receive and transmit frame. Effective start of the frame can be then shifted of up to 7 clock pulses independently in receive and transmit directions by proper programming of the PCMSH register. Pin-strap control mode: FS0. Frame Sync. pulse of channel #0. One MCLK cycle long, starts PCM data transfer in the Time Slot following its falling edge (Short Frame Delayed Timing).
19	IO0/GR2	DIO/DI	MCU control mode: IO0. Slic control I/O pin #0. Can be programmed as input or output via DIR register. Depending on content of CONF register can be a static input/output or a dynamic input/output synchronized with the $\overline{CSn}$ output signals controlling the SLICs. Pin-strap control mode: GR2. Receive gain programming channel 2: 1: Receive gain = -0.8 dB 0: Rec. gain = -4.3 dB
20	IO1/PD2	DIO/DI	MCU control mode: IO1. Slic control I/O pin #1. (see IO0 description). Pin-strap control mode: PD2. Power Down command channel 2: 1: Channel 2 Codec is in power down. (equivalent to CONF reg bit2 = 1) 0: Channel 2 Codec is in power up. (equivalent to CONF reg. bit2 = 0)
21	IO2/GR3	DIO/DI	MCU control mode: IO2. Slic control I/O pin #2. (see IO0 description) Pin-strap control mode: GR3. Receive gain programming channel 3. (see GR2 description)
22	IO3/PD3	DIO/DI	MCU control mode: IO3. Slic control I/O pin #3. (see IO0 description). Pin-strap control mode: PD3. Power down command channel 3. (see PD2 description)
23	IO4/FS1	DIO/DI	MCU control mode: IO4 Slic control I/O pin #4. (see IO0 description). Pin-strap control mode: FS1. Frame sync. pulse of channel #1. One MCLK cycle long, starts PCM data transfer in the time slot following its falling edge (short frame delayed timing).
24	IO5/FS2	DIO/DI	MCU control mode: IO4. Slic control I/O pin #5. (see IO0 description). Pin-strap control mode: FS2. Frame sync. pulse of channel #1. One MCLK cycle long, starts PCM data transfer in the time slot following its falling edge (short frame delayed timing).

Table 3. Pin description (continued)

N.	Name	Type	Function
62	IO6/FS3	DIO/DI	MCU control mode: IO4. Slic control I/O pin #6. (see IO0 description). Pin-strap control mode: FS3. Frame sync. pulse of channel #1. One MCLK cycle long, starts PCM data transfer in the time slot following its falling edge (short frame delayed timing).
28	$\overline{CS0}$/GX0	DO/DI	MCU control mode: $\overline{CS0}$. Slic CS control #0. Depending on CONF reg. content can be a CS output for SLIC #0 or a static I/O. When configured as CS output it is automatically generated by the Codec with a repetition time of 31.25 µs. In this mode also the IO11.0 are synchronized and carry proper data in and out synchronous with CS. Pin-strap control mode: GX0. Transmit gain programming channel 0: 1: Transmit gain = 0 dB 0: Transmit gain = - 3.5 dB
29	$\overline{CS1}$/GX1	DO/DI	MCU control mode: $\overline{CS1}$: Slic CS control #1, (see $\overline{CS0}$ description). Pin-strap control mode: GX1. Transmit gain programming channel 1 (see GX0 description)
53	$\overline{CS2}$/GX2	DO/DI	MCU control mode: $\overline{CS2}$. Slic CS control #2, (see $\overline{CS0}$ description). Pin-strap control mode: GX2. Transmit gain programming channel 2 (see GX0 description)
52	$\overline{CS3}$/GX3	DO/DI	MCU control mode: $\overline{CS3}$. Slic CS control #3, (see $\overline{CS0}$ description). Pin-strap control mode: GX3. Transmit gain programming channel 3 (see GX0 description)
4	$\overline{CS}$/PD1	DI/DI	MCU control mode: $\overline{CS}$. Chip Select of Serial Control Bus. When this pin is low control information can be written to or read from the device via the CI and CO pins. Pin-strap control mode: PD1. Power Down command channel 1. (see PD2 description).
7	CCLK/GR1	DI/DI	MCU control mode: CCLK. Clock of Serial Control Bus. This clock shifts serial control information into or out of CI or CO when $\overline{CS}$ input is low depending on the current instruction. CCLK may be asynchronous with the other system clocks. Pin-strap control mode: GR1. Receive gain programming ch. 1, (see GR2 description).
6	CI/PD0	DI/DI	MCU control mode: CI. Control Data Input of Serial Control Bus. Control data is shifted in the device when $\overline{CS}$ is low and clocked by CCLK. Pin-strap control mode: PD0. Power Down command channel 0. (see PD2 description).

Table 3. Pin description (continued)

N.	Name	Type	Function
5	CO/GR0	DTO/DI	MCU control mode: CO. Control Data Output of Serial Control Bus. Control data is shifted out the device when $\overline{CS}$ is low and clocked by CCLK. During the first 8 CCLK pulses the CO pin is H. I., valid data are shifted out during the following 8 CCLK pulses. Pin-strap control mode: GR0. Receive gain programming ch. 0, (see GR2 description).
3	$\overline{INT}$/AMU	ODO/DI	MCU control mode: $\overline{INT}$. Interrupt output (open drain), goes low when a data change has been detected in the I/O pins. One mask registers allow to mask any I/O pin. Interrupt is reset when the I/O register is read. Pin-strap control mode: AMU. A/µ Law selection: AMU=0: µ Law AMU=1: A Law, even bit inverted

2 Functional description

2.1 Power on initialization

When power is first applied it is recommended to reset the device by forcing the condition M1.0=00, in order to clear all the internal registers.

In MCU mode M0 is set steadily Low and the device is reset by applying a negative pulse to M1 (its operative level in MCU mode is High); same result can be obtained by writing an High level into the control bit RES of the CONF register.

In pin-strap mode M1 is set steadily Low and the device is reset by applying a negative pulse to M0 (its operative level in pin-strap mode is High); at the end of the Reset phase (M0=High) the device is programmed according to the logical configuration of the control pins.

During the reset condition all the I/On and CS_n pins are set as inputs, DX is set in high impedance and all VFROn outputs are forced to AGND.

2.2 Power down state

Each of the four channel may be put into power down mode by setting the appropriate bit in the CONF register or strapping to VDD the proper pin. In this mode the eventual programmed DX channel is set in high impedance while the VFRO outputs are forced to AGND. In pin-strap mode the value forced on the input pin is internally updated every FS signal.

2.3 Transmit path

The analog VFXI signal through an amplifier stage is applied to a PCM converter and the corresponding digital signal is sent to DX output.

In MCU mode, the amplifier gain can be programmed with two different values by means of TXG Reg.: 0 dB or +3.52 dB.

A programmable gain block after the A/D conversion allows to set transmit gain in 12dB range, with steps <0.1dB by writing proper code into GTXn register.

Setting GTXn=00h, the transmitted signal is muted, i.e. an idle PCM signal is generated on DX.

A/μ coding Law is selected by bit5 (AMU) of CONF reg.

Setting LIN=1 (bit6 of CONF reg.) the linear coding Law is selected (16bits); in this case the signal sent on DX will take two adjacent PCM time slots.

In Pin-strap mode, the amplifier gain is set to 0dB; only two values of Transmit gain can be selected according to the level of GXn control input (in Pin-strap):

GXn=1 selects the gain corresponding to GTXn=FFh (0 dB)

GXn=0 selects the gain corresponding to GTXn=8Fh (-3.5 dB)

Different gain value is obtained through proper voltage divider.

A/μ coding Law is selected according to AMU pin level:

AMU=0 µ Law selected.

AMU=1 A Law selected.

VFXI input must be AC coupled to the signal source; the voltage swing allowed is 1.0Vpp when the preamplifier gain is set 0dB or 0.66Vpp if the gain is set to 3.52dB (MCU mode only); higher levels must be reduced through proper dividers.

Typical impedance of VFXI input is 1Mohm.

Figure 3. Transmit path

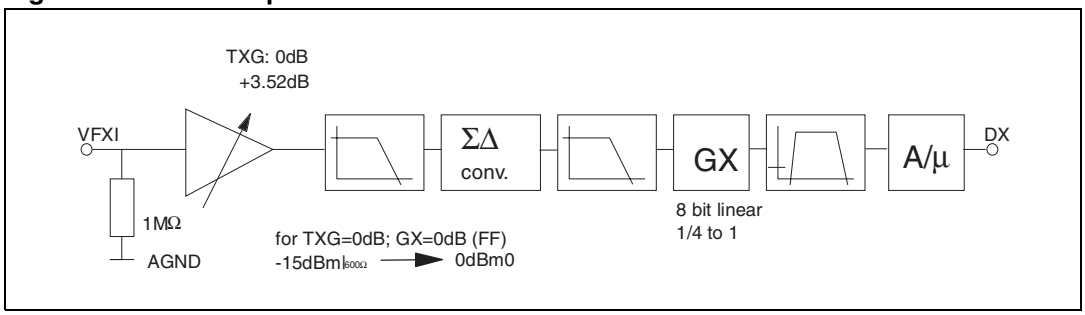


Figure 4. Receive path

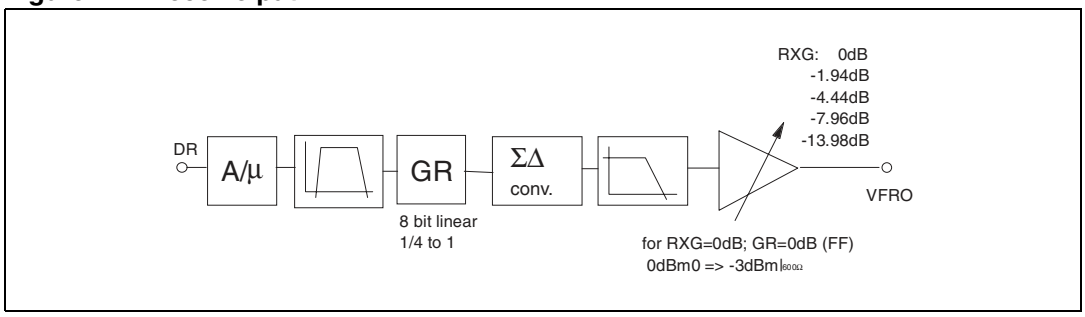
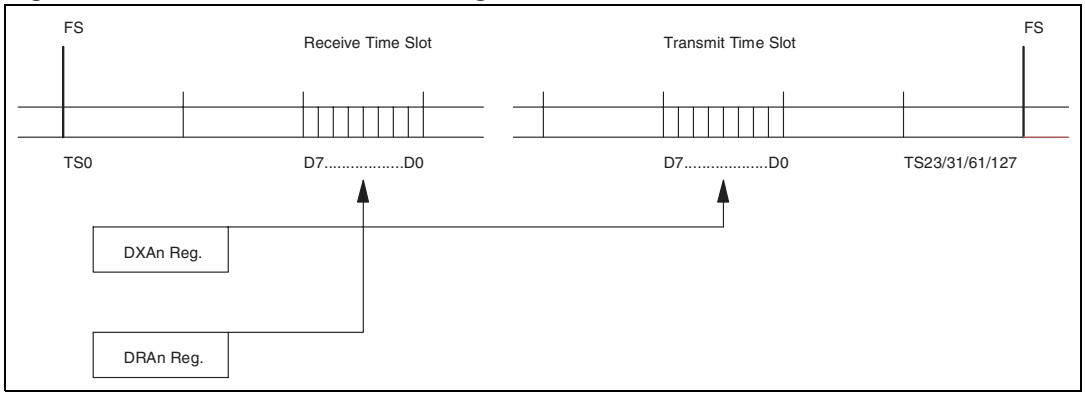


Figure 5. MCU mode: time slot assignment



2.4 Receive path

The received PCM signal DR through the decoder section, the gain select block and the D/A converter is converted in an analog signal which is transferred to VFRO output through an amplifier stage.

In MCU mode a programmable gain block before the A/D conversion allows to set receive gain in 12dB range, with steps <0.1 dB by writing proper code into GRXn register.

The amplifier gain can be programmed with five different values by means of RXG register: 0 dB -1.94 dB -4.44 dB -7.96 dB -13.98 dB.

Setting GRXn=00h, the receive signal is muted and VFRO output is set to AGND.

A/µ coding Law is selected by bit5 (AMU) of CONF reg.

Setting LIN = 1 (bit6 of CONF reg.) the linear coding Law is selected (16bits); in this case the signal received on DR will take two adjacent PCM time slots.

In pin-strap mode only two values of Receive Gain can be selected according to the level of GRn control input (in pin-strap) GRn = 1 selects the gain corresponding to GRXn= E2h, RXG = 0dB (-0.8 dB) GRn = 0 selects the gain corresponding to GRXn = AFh, RXG = -1.94 dB (-4.3 dB).

Different gain value is obtained through proper voltage divider.

A/µ coding Law is selected according to AMU pin level:

AMU=0 µ Law selected.

AMU=1 A Law selected.

VFRO output, referred to AGND must be AC coupled to the load, referred to VSS, to prevent a DC current flow.

VFRO has a drive capability of 1.0mA (peak value), with a max AC swing of 2 Vpp.

In order to get the best noise performances it is recommended to keep the GRX value as close as possible to the maximum (FFh) setting properly the additional attenuation by means of RXG.

2.5 PCM interface

The STLC5046 dedicate five pins (six in pin-strap mode) to the interface with the PCM highways.

MCLK represents the bit clock and is also used by the device as a source for the clock of the internal Sigma Delta converter timings. Four possible frequencies can be used: 1.536/1.544 MHz (24 channels PCM frame); 2048 MHz (32 channels PCM frame); 4.096 MHz (64 channels PCM frame); 8.192 MHz (128 channels PCM frame).

The operating frequency is automatically detected by the device when both MCLK and FS are applied. MCLK is synchronizing both the transmit data (DX) and the receive data (DR).

2.5.1 MCU mode

The Frame Sync. signal FS is the common time base for all the four channels; Short (one MCLK period) or Long (more than one MCLK period) FS are allowed.

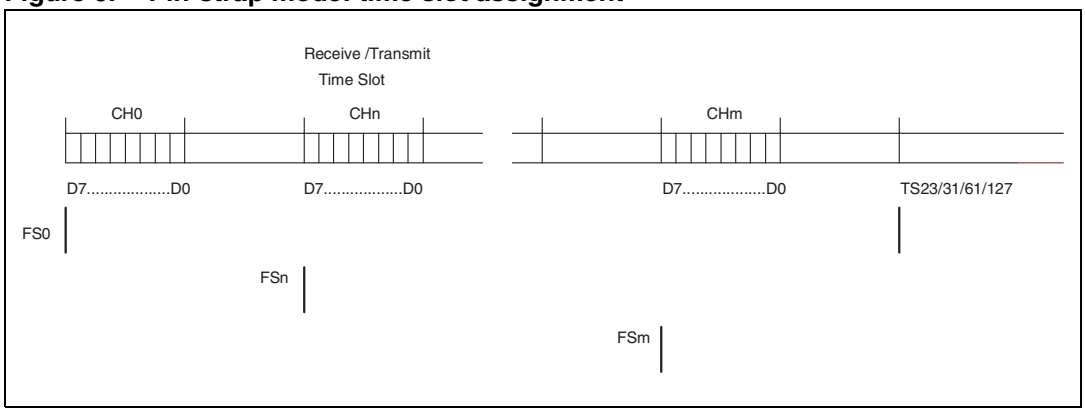
Transmit and Receive programmable Time-Slots are framed to an internal sync. signal that can be coincident with FS or delayed of 1 to 7 MCLK cycles depending on the programming of PCMSH register.

DX represent the transmit PCM interface. It remains in high impedance state except during the assigned time slots during which the PCM data byte is shifted out on the rising edge of MCLK.

The four channels can be shifted out in any possible timeslot as defined by the DXA0 to DXA3 registers. If one codec is set in Power Down by software programming the corresponding timeslot is set in High Impedance. When linear coding mode is selected by CONF register programming the output channel will need two consecutive timeslots (see register description).

DR represent the receive PCM interface. It remains inactive except during the assigned time slots during which the PCM data byte is shifted in on the falling edge of MCLK. The four channels are shifted in any possible timeslot as defined by the DRA0 to DRA3 registers.

Figure 6. Pin-strap mode: time slot assignment



2.5.2 Pin-strap mode

When pin-strap mode is selected, dedicated Frame Sync. FS3..0 are provided on dual function pins:

MCU	Pin-strap	Pin
FS	FS0	14
IO4	FS1	23
IO5	FS2	24
IO6	FS3	62

The PCMSH register cannot be accessed, therefore the beginning of the transmit and receive frame is identified by the rising edge of the FSn signal.

Each channel has its dedicated Frame Sync. signal FSn. Short or Long frame timing is automatically selected; depending on the FS signal applied to FS0 input. The assigned Time Slot (Transmit and Receive) takes place in the 8 MCLK cycles following the falling edge of FSn in case of Short Frame or the rising edge in case of Long Frame. If one codec is set in Power Down by proper pin-strap configuration the corresponding timeslot is not loaded and the VFRO output is kept at steady AGND level.

Finally by means of the LOOPB register is possible to implement a digital or analog loop_back on any of the selected channels.

$\overline{TSX}$ represent the Transmit Time Slot (open drain output, 3.2mA). Normally it is floating in high impedance state except when a time slot is active on the DX output. In this case TSX output pulls low to enable the backplane line driver. Should be strapped to VSS when not used.

Table 4. Control byte structure

First byte (address)							
7	6	5	4	3	2	1	0
R/$\overline{W}$	D/$\overline{S}$	A5	A4	A3	A2	A1	A0
D7	D6	D5	D4	D3	D2	D1	D0

R/$\overline{W}$ = 0: Write register

R/$\overline{W}$ = 1: Read register

D/$\overline{S}$ = 0: Single byte

D/$\overline{S}$ = 1: Two bytes

A5..A0: Register Address

2.6 Control interface

STLC5046 has two control modes, a microprocessor control mode and a pin-strap control mode. The two modes are selected by M0 and M1 pins. When M0 = low, M1 = high (MCU control mode) the MCU port is activated; and the 41 registers of the device can be programmed. When M0 = high, M1 = low (Pin-strap mode) the microprocessor control port is disabled and some of the digital pins change their function allowing to perform a very basic programming of the device.

In pin-strap mode the status of the control pins is entered at power-on reset and refreshed at any Frame Sync. cycle.

In MCU mode the control information is written to or read from STLC5046 via the serial four wires control bus:

CCLK: Control Clock

$\overline{CS}$: Chip Select input

CI: Serial Data input

CO: Serial Data output

All control instructions require 2 bytes, with the exception of the single byte for command synchronization. The first byte specify the register address, and the type of access (Read or Write). The second byte contain the data to be loaded into the register (on CI wire) or carried out the register content (on CO wire) depending on the R/W bit of the first byte. CO wire is normally in High Impedance and goes to low impedance only during the second byte in case of Read operation. This allows to use a common wire for both CI/CO.

Serial data CI is shifted to the serial input register on the rising edge of CCLK and CO is shifted out on the falling.

$\overline{CS}$, normally High, is set Low during the transmission / reception of a byte, lasting 8CCLK pulses.

Though, in general, two bytes of the same instruction take two $\overline{CS}$ separated cycles, STLC5046 can handle the data transfer in a single 16 CCLK CS cycle, in both the directions.

One additional wire provided to the control interface is an open drain interrupt output (INT) that goes low when a change of status is detected on the I/O pins.

2.7 SLIC control interface

The device provides 12 I/O pins plus 4 $\overline{CS}$ signals. The interface can work in dynamic or static mode: it can be selected by means of DIR register.

- Dynamic Mode: the I/O pins are configured as input or output by means of DIR register. The CS signals are used to select the different SLIC interface. In this case the I/O pin can be multiplexed. The data loaded from SLIC#n via I/O pins configured as input can be read in the DATAn register. The data written in a DATAn register will be loaded on the I/O pins configured as output when the Csn signal will be active.
- Static Mode: The CS signal can be used as I/O pins. They can be configured as input or output I/O by means of DATA1 register. The data corresponding to the CS signal can be read or written by means of DATA2 register. All data related to th other I/O pins can be read or written by means of DATA0 register.

3 Registers addresses

Table 5. Registers addresses (only MCU mode)

Address	Name	Description
00h	CONF	Configuration register
01h	DIR-L	I/O Direction (bit 7-0)
02h	DIR-H	I/O Direction (bit 11-8)
03h	DATA0-L	I/O Data ch#0/ Static Data; (bit 7-0)
04h	DATA0-H	I/O Data ch#0/ Static Data; (bit 11-8)
05h	DATA1-L	I/O Data ch#1 (bit 7-0) / CS Direction
06h	DATA1-H	I/O Data ch#1 (bit 11-8)
07h	DATA2-L	I/O Data ch#2 (bit 7-0) / CS Data
08h	DATA2-H	I/O Data ch#2 (bit 11-8)
09h	DATA3-L	I/O Data ch#3 (bit 7-0)
0Ah	DATA3-H	I/O Data ch#3 (bit 11-8)
0Bh	GTX0	Transmit Gain ch#0
0Ch	GTX1	Transmit Gain ch#1
0Dh	GTX2	Transmit Gain ch#2
0Eh	GTX3	Transmit Gain ch#3
0Fh	GRX0	Receive Gain ch#0
10h	GRX1	Receive Gain ch#1
11h	GRX2	Receive Gain ch#2
12h	GRX3	Receive Gain ch#3
13h	DXA0	Transmit Timeslot ch#0
14h	DXA1	Transmit Timeslot ch#1
15h	DXA2	Transmit Timeslot ch#2
16h	DXA3	Transmit Timeslot ch#3
17h	DRA0	Receive Timeslot ch#0
18h	DRA1	Receive Timeslot ch#1
19h	DRA2	Receive Timeslot ch#2
1Ah	DRA3	Receive Timeslot ch#3
1Bh	PCMSH	PCM Shift register
1Ch	DMASK-L	Interrupt Mask I/O Port (03h)
1Dh	DMASK-H	Interrupt Mask I/O Port (04h)
1Eh	CMASK	Interrupt Mask I/O Port (07h)
1Fh	PCHK-A	Persistency Check Time for Input A
20h	PCHK-B	Persistency Check Time for Input B
21h	INT	Interrupt register
22h	ALARM	Alarm register
23h	AMASK	Interrupt Mask for Alarm
24h	LOOPB	Loopback register
25h	TXG	Transmit Preamp. Gain
26h	RXG-1,0	Receive Preamp. Gain (ch1 ch0)
27h	RXG-3,2	Receive Preamp. Gain (ch3 ch2)
31h	SRID	Silicon Revision Identification Code

3.1 Registers description

3.1.1 Configuration register (CONF)

Addr=00h; Reset Value=3Fh

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RES	LIN	AMU	STA	PD3	PD2	PD1	PD0

RES=0 Normal operation

RES=1 Device reset: I/0n and $\overline{CSn}$ are all inputs, DX is H.I. (equivalent to Hw. reset).

LIN=0 A or µ Law PCM encoding

LIN=1 Linear encoding (16 bits), two's complement.

AMU=0 µ Law selection

AMU=1 A Law selection (even bits inverted)

STA=0 $\overline{CS0}$ to $\overline{CS3}$ scan the four SLICs connected to the I/O control port, each $\overline{CS}$ has a 31.25µs repetition time.

STA=1; I/O are static, $\overline{CS0}$ to $\overline{CS3}$ are configured as generic static I/O

PD3..0=0 CODEC 3..0 is active

PD3..0=1 CODEC 3..0 is in power Down. When one codec is in Power Down the corresponding VFRO output is forced to AGND. and the corresponding transmit time slot on DX is set in H.I.

Pin-strap value:

RES	0	AMU	0	PD3	PD2	PD1	PD0

3.1.2 I/O Direction register (DIR)

Addr=01h; Reset Value=00h

Addr=02h; Reset Value=X0h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IO_7	IO_6	IO_5	IO_4	IO_3	IO_2	IO_1	IO_0
				IO_{11}	IO_{10}	IO_9	IO_8

$IO_{11..0}$ = 0; I/O pin 11..0 is an input, data on the I/O input is written in DATAn register bit 11..0.

$IO_{11..0}$ = 1; I/O pin 11..0 is an output, data contained in DATAn register bit11..0 is transferred to the I/O output.

Pin-strap value:

0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

3.1.3 I/O Data register channel #0 (DATA0)

Addr=03h; Reset Value=00h

Addr=04h; Reset Value=X0h

If bit 4 of CONF register (STA)=0

Dynamic I/O mode:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$D0_7$	$D0_6$	$D0_5$	$D0_4$	$D0_3$	$D0_2$	$D0_1$	$D0_0$
				$D0_{11}$	$D0_{10}$	$D0_9$	$D0_8$

When $\overline{CS0}$ is active D011..0 are transferred to the corresponding I/O pins configured as outputs (see DIR register). For the I/O pins configured as inputs the corresponding $D0_{11..0}$ will be written by the values applied to those pins while CS0 is low.

If bit 4 of CONF register (STA)=1

Static I/O mode:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DS_7	DS_6	DS_5	DS_4	DS_3	DS_2	DS_1	DS_0
				DS_{11}	DS_{10}	DS_9	DS_8

$D_{11..0}$ are transferred to the corresponding I/O pins configured as outputs (see DIR register). For the I/O pins configured as inputs the corresponding $D_{11..0}$ will be written by the values applied to those pins.

Pin-strap value:

0	0	0	0	0	0	0	0
				0	0	0	0

3.1.4 I/O Data register channel #1 (DATA1)

Addr=05h; Reset Value=00h

Addr=06h; Reset Value=X0h

If bit 4 of CONF register (STA)=0

Dynamic I/O mode:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$D1_7$	$D1_6$	$D1_5$	$D1_4$	$D1_3$	$D1_2$	$D1_1$	$D1_0$
				$D1_{11}$	$D1_{10}$	$D1_9$	$D1_8$

When $\overline{CS1}$ is active $D_{11..0}$ are transferred to the corresponding I/O pins configured as outputs (see DIR register). For the I/O pins configured as inputs the corresponding $D_{11..0}$ will be written by the values applied to those pins while $\overline{CS1}$ is low.

If bit 4 of CONF register (STA)=1

Static I/O mode:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
				CIO_3	CIO_2	CIO_1	CIO_0

CIO0..3=0 The $\overline{CS0..3}$ is a static input, DATA is written in DATA2 register bits 0..3.

CIO0..3=1 The $\overline{CS0..3}$ is a static output, DATA is taken from DATA2 register bits 0..3.

Pin-strap value:

0	0	0	0	0	0	0	0
				0	0	0	0

3.1.5 I/O Data register channel #2 (DATA2)

Addr=07h; Reset Value=00h

Addr=08h; Reset Value=X0h

If bit 4 of CONF register (STA)=0

Dynamic I/O mode:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$D2_7$	$D2_6$	$D2_5$	$D2_4$	$D2_3$	$D2_2$	$D2_1$	$D2_0$
				$D2_{11}$	$D2_{10}$	$D2_9$	$D2_8$

When $\overline{CS2}$ is active $D2_{11..0}$ are transferred to the corresponding I/O pins configured as outputs (see DIR register). For the I/O pins configured as inputs the corresponding D11..0 will be written by the values applied to those pins while $\overline{CS2}$ is low.

If bit 4 of CONF register (STA)=1

Static I/O mode:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
				CD_3	CD_2	CD_1	CD_0

$CD_{3..0}$ are transferred to the corresponding $\overline{CS}$ pin if configured as static output (see register DATA1). For the $\overline{CS}$ pins configured as static inputs the corresponding $CD_{3..0}$ will be written by the values applied to those pins.

Pin-strap value:

0	0	0	0	0	0	0	0
				0	0	0	0

3.1.6 I/O Data register channel #3 (DATA3)

Addr=09h; Reset Value=00h

Addr=0Ah; Reset Value=X0h

Used only if bit 4 of CONF register (STA)=0; Dynamic

I/O mode:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$D3_7$	$D3_6$	$D3_5$	$D3_4$	$D3_3$	$D3_2$	$D3_1$	$D3_0$
				$D3_{11}$	$D3_{10}$	$D3_9$	$D3_8$

When $\overline{CS3}$ is active D11..0 are transferred to the corresponding I/O pins configured as outputs (see DIR register). For the I/O pins configured as inputs the corresponding D11..0 will be written by the values applied to those pins while $\overline{CS3}$ is low.

If bit4 of CONF register (STA)=1

Static I/O mode:

can be used as general purpose R/W registers, without any direct action on the control of the device.

Pin-strap value:

0	0	0	0	0	0	0	0
				0	0	0	0

3.1.7 Transmit Gain channel #0 (GTX0)

Addr=0Bh; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

00h:Stop any transmit signal, null level is transmitted in the corresponding timeslot on DX output.

>00h:Digital gain is inserted in the TX path equal to:

20log[0.25+0.75*(progr. value/256)]

Pin-strap values:

GX0=1: 0 dB gain (value = FFh):

1	1	1	1	1	1	1	1

GX0=0: -3.5 dB gain (value = 8Fh):

1	0	0	0	1	1	1	1

3.1.8 Transmit Gain channel #1 (GTX1)

Addr=0Ch; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

00h:Stop any transmit signal, null level is transmitted in the corresponding timeslot on DX output.

>00h:Digital gain is inserted in the TX path equal to:

20log[0.25+0.75*(progr. value/256)]

Pin-strap values:

GX0=1: 0 dB gain (value = FFh):

1	1	1	1	1	1	1	1

GX0=0: -3.5 dB gain (value = 8Fh):

1	0	0	0	1	1	1	1

3.1.9 Transmit Gain channel #2 (GTX2)

Addr=0Dh; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

00h: Stop any transmit signal, null level is transmitted in the corresponding timeslot on DX output.

>00h:Digital gain is inserted in the TX path equal to:

20log[0.25+0.75*(progr. value/256)]

Pin-strap values:

GX0=1: 0 dB gain (value = FFh):

1	1	1	1	1	1	1	1

GX0=0: -3.5 dB gain (value = 8Fh):

1	0	0	0	1	1	1	1

3.1.10 Transmit Gain channel #3 (GTX3)

Addr=0Eh; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

00h:Stop any transmit signal, null level is transmitted in the corresponding timeslot on DX output.

>00h:Digital gain is inserted in the TX path equal to:

20log[0.25+0.75*(progr. value/256)]

Pin-strap values:

GX0=1: 0 dB gain (value = FFh):

1	1	1	1	1	1	1	1

GX0=0: -3.5 dB gain (value = 8Fh):

1	0	0	0	1	1	1	1

3.1.11 Receive Gain channel #0 (GRX0)

Addr=0Fh; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

00h:Stop any received signal, AGND level is forced on the VFRO0 analog output.

>00h:Digital gain is inserted in the RX path equal to:

20log[0.25+0.75*(progr. value/256)]

Pin-strap values:

GR0=1: -0.8 dB gain (value = E2h):

1	1	1	0	0	0	1	0

GR0=0: -2.36 dB gain (value = AFh):

1	0	1	0	1	1	1	1

Overall gain including also RXG:

GR0 = 1:-0.8 dB; GR0 = 0: -4.3 dB

3.1.12 Receive Gain channel #1 (GRX1)

Addr=10h; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

00h:Stop any received signal, AGND level is forced on the VFRO1 analog output.

>00h:Digital gain is inserted in the RX path equal to:

20log[0.25+0.75*(progr. value/256)]

Pin-strap values:

GR1=1: -0.8 dB gain (value = E2h):

1	1	1	0	0	0	1	0

GR1=0: -2.36 dB gain (value = AFh):

1	0	1	0	1	1	1	1

Overall gain including also RXG:

GR1= 1:-0.8 dB; GR1 = 0: -4.3 dB

3.1.13 Receive Gain channel #2 (GRX2)

Addr=11h; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

00h:Stop any received signal, AGND level is forced on the VFRO2 analog output.

>00h:Digital gain is inserted in the RX path equal to:

$$20\log[0.25+0.75*(\text{progr. value}/256)]$$

Pin-strap values:

GR2=1: -0.8 dB gain (value = E2h):

1	1	1	0	0	0	1	0

GR2=0: -2.36 dB gain (value = AFh):

1	0	1	0	1	1	1	1

Overall gain including also RXG:

GR2 = 1:-0.8 dB; GR2 = 0: -4.3 dB

3.1.14 Receive Gain channel #3 (GRX3)

Addr=12h; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

00h:Stop any received signal, AGND level is forced on the VFRO3 analog output.

>00h:Digital gain is inserted in the TX path equal to:

20log[0.25+0.75*(progr. value/256)]

Pin-strap values:

GR3=1: -0.8 dB gain (value = E2h):

1	1	1	0	0	0	1	0

GR3=0: -4.3 dB gain (value = AFh):

1	0	1	0	1	1	1	1

Overall gain including also RXG:

GR3 = 1:-0.8 dB; GR3 = 0: -4.3 dB

3.1.15 Transmit Time Slot channel #0 (DXA0)

Addr=13h; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EN0	T06	T05	T04	T03	T02	T01	T00

EN0=0: Selected transmit time slot on DX output is in H.I.

EN0=1: Selected transmit time slot on DX output is active carrying out the PCM encoded signal of VFXI0.

T06..0: Define time slot number (0 to 127) on which PCM encoded signal of VFXI0 is carried out.

If linear mode is selected (LIN=1 of CONF register) the 16 bits will be carried out as follows: the 8 most significative bits in the programmed time slot, the 8 least significative bits in the following timeslot.

Example: if T06..T00=00:

TS0								TS1							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Pin-strap value (value 80h):

1	0	0	0	0	0	0	0

Referred to FS0.

3.1.16 Transmit Time Slot channel#1 (DXA1)

Addr=14h; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EN1	T16	T15	T14	T13	T12	T11	T10

EN1=0: Selected transmit time slot on DX output is in H.I.

EN1=1: Selected transmit time slot on DX output is active carrying out the PCM encoded signal of VFXI1.

T16..0:Define time slot number (0 to 127) on which PCM encoded signal of VFXI1 is carried out.

If linear mode is selected (LIN=1 of CONF register) the 16 bits will be carried out as follows: the 8 most significative bits in the programmed time slot, the 8 least significative bits in the following timeslot.

Example: if T16..T10=00:

TS0								TS1							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Pin-strap value (value 80h):

1	0	0	0	0	0	0	0

Referred to FS1.

3.1.17 Transmit Time Slot channel #2 (DXA2)

Addr=15h; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EN2	T26	T25	T24	T23	T22	T21	T20

EN2=0: Selected transmit time slot on DX output is in H.I.

EN2=1: Selected transmit time slot on DX output is active carrying out the PCM encoded signal of VFXI2.

T26..0:Define time slot number (0 to 127) on which PCM encoded signal of VFXI2 is carried out.

If linear mode is selected (LIN=1 of CONF register) the 16 bits will be carried out as follows: the 8 most significative bits in the programmed time slot, the 8 least significative bits in the following timeslot.

Example: if T26..T20=00:

TS0								TS1							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Pin-strap value (value 80h):

1	0	0	0	0	0	0	0

Referred to FS2.

3.1.18 Transmit Time Slot channel #3 (DXA3)

Addr=16h; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EN3	T36	T35	T34	T33	T32	T31	T30

EN3=0: Selected transmit time slot on DX output is in H.I.

EN3=1: Selected transmit time slot on DX output is active carrying out the PCM encoded signal of VFXI3.

T36..0:Define time slot number (0 to 127) on which PCM encoded signal of VFXI3 is carried out.

If linear mode is selected (LIN=1 of CONF register) the 16 bits will be carried out as follows: the 8 most significative bits in the programmed time slot, the 8 least significative bits in the following timeslot.

Example: if T36..T30=00:

TS0								TS1							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Pin-strap value (value 80h):

1	0	0	0	0	0	0	0

Referred to FS3.

3.1.19 Receive Time Slot channel #0 (DRA0)

Addr=17h; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EN0	R06	R05	R04	R03	R02	R01	R00

EN0=0: Disable reception of selected time slot.

EN0=1: Selected receive time slot on DR input is PCM decoded and transferred to VFRO0 output.

R06..0:Define receive time slot number (0 to 127) on carrying the PCM signal to be decoded and transferred to VFRO0 output.If linear mode is selected (LIN=1 of CONF register) the 16 bits will be used as linear code as follows: the 8most significative bits in the programmed time slot, the 8 least significative bits in the following timeslot.

Example: if R06..R00=00:

TS0								TS1							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Pin-strap value (value 80h):

1	0	0	0	0	0	0	0

Referred to FS0.

3.1.20 Receive Time Slot channel #1 (DRA1)

Addr=18h; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EN0	R16	R15	R14	R13	R12	R11	R10

EN1=0: Disable reception of selected time slot.

EN1=1: Selected receive time slot on DR input is PCM decoded and transferred to VFRO1 output.

R16..0:Define receive time slot number (0 to 127) on carrying the PCM signal to be decoded and transferred to VFRO1 output.If linear mode is selected (LIN=1 of CONF register) the 16 bits will be used as linear code as follows: the 8most significative bits in the programmed time slot, the 8 least significative bits in the following timeslot.

Example: if R16..R10=00:

TS0								TS1							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Pin-strap value (value 80h):

1	0	0	0	0	0	0	0

Referred to FS1.

3.1.21 Receive Time Slot channel #2 (DRA2)

Addr=19h; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EN0	R26	R25	R24	R23	R22	R21	R20

EN2=0: Disable reception of selected time slot.

EN2=1: Selected receive time slot on DR input is PCM decoded and transferred to VFRO1 output.

R26..0:Define receive time slot number (0 to 127) on carrying the PCM signal to be decoded and transferred to VFRO2 output.If linear mode is selected (LIN=1 of CONF register) the 16 bits will be used as linear code as follows: the 8most significative bits in the programmed time slot, the 8 least significative bits in the following timeslot.

Example: if R26..R20=00:

TS0								TS1							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Pin-strap value (value 80h):

1	0	0	0	0	0	0	0

Referred to FS2.

3.1.22 Receive Time Slot channel #3 (DRA3)

Addr=1Ah; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EN0	R36	R35	R34	R33	R32	R31	R30

EN3=0: Disable reception of selected time slot.

EN3=1: Selected receive time slot on DR input is PCM decoded and transferred to VFRO1 output.

R36..0:Define receive time slot number (0 to 127) on carrying the PCM signal to be decoded and transferred to VFRO2 output.If linear mode is selected (LIN=1 of CONF register) the 16 bits will be used as linear code as follows: the 8most significative bits in the programmed time slot, the 8 least significative bits in the following timeslot.

Example: if R36..R30=00:

TS0								TS1							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Pin-strap value (value 80h):

1	0	0	0	0	0	0	0

Referred to FS3.

3.1.23 PCM Shift register (PCMSH)

Addr=1Bh; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	XS2	XS1	XS0		RS2	RS1	RS0

XS2..0:Effective start of the TX frame is the programmed values of clock pulses (0 to 7) after the FS rising edge.

RS2..0:Effective start of the RX frame is the programmed values of clock pulses (0 to 7) after the FS rising edge.

Pin-strap value (value=00h):

0	0	0	0	0	0	0	0

3.1.24 Interrupt Mask register for I/O port (DMASK)

Addr=1Ch; Reset Value=FFh

Addr=1Dh; Reset Value=XFh

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0
				MD11	MD10	MD9	MD8

MD11..0=1: The corresponding I/O doesn't generate interrupt.

MD11..0=0: The corresponding I/O (programmed as Input) generate interrupt if a change of status is detected.

Input lines with persistency check generate interrupt if the changed status remains stable longer than the time programmed in the persistency check registers PCHKA/B. Lines without persistence check generate an immediate interrupt request.

Mask register has no effect on those pins configured as outputs, those pins will not generate interrupt.

Pin-strap value.

1	1	1	1	1	1	1	1
				1	1	1	1

3.1.25 Interrupt Mask register for CD port (CMASK)

Addr=1Eh; Reset Value=XFh

Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
				MC3	MC2	MC1	MC0

In MCU mode, dynamic I/O configuration, MCn bits are the disable/enable interrupt related to the channel n:

MC3..0= 0 Any I/O line of the related channel is enabled to generate interrupt depending on DMASK setting.

MC3..0=1 Any I/O line of the related channel is disabled to generate interrupt independently of DMASK setting.

In MCU mode, static I/O configuration, MCn bits are the interrupt mask bits related to CSn that are configured as I/O lines.

MC3..0=1: The corresponding I/O doesn't generate interrupt.

MC3..0=0: The corresponding I/O generate interrupt if a change of status is detected.

Input lines with persistency check generate interrupt if the changed status remains stable longer than the time programmed in the persistency check registers PCHKA/B

Lines without persistency check generate an immediate interrupt request.

Mask register has no effect on those pins configured as outputs, those pins will not generate interrupt.

Pin-strap value (value=00h):

1	1	1	1	1	1	1	1

3.1.26 Persistency Check register (PCHK-A/B)

Two input signals per channel, labeled A and B, are submitted to persistency check.

In dynamic mode (STA=0), A and B inputs of the four channels, are sampled on the multiplexed lines IO0 (pin13) and IO1 (pin14).

In static mode (STA=1) the persistency check is performed on four pairs of lines, assigned to each channel according to the table:

CHAN#	Input A	Input B
0	IO0 (pin 19)	IO1 (pin 20)
1	IO4 (pin 17)	IO5 (pin 18)
2	IO6 (pin 48)	IO7 (pin 47)
3	IO10 (pin 44)	IO11 (pin 43)

Addr=1Fh; Reset Value=00h

Addr=20h; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0
TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0

TA7..0 and TB7..0, content of PCHKA and PCHKB registers, define the minimum duration of input A and B to generate interrupt; spurious transitions shorter than the programmed value are ignored.

The time width can be calculated according to the formula:

Time-Width A = (TA7..0) x 64 µs

Time-Width B = (TB7..0) x 64 µs

If PCHKA/B is programmed to 00h the persistency check is not performed and any detected transition will generate interrupt.

All the inputs, with or without persistency check, are sampled with a repetition rate of 32µs

Pin-strap value:

0	0	0	0	0	0	0	0

0	0	0	0	0	0	0	0

3.1.27 Interrupt register (INT)

Addr=21h; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
			ICKF	ID3	ID2	ID1	ID0

ICKF = 1: If interrupt is generated by a change of bit 0 in register ALARM.

In dynamic I/O configuration the ID3..0 bits latch the interrupt request from the related channel.

Any single bit IDn is cleared after reading related I/O register or by setting MCn bit High (i.e. when channel n is disabled to generate interrupt).

In static I/O configuration ID0 and ID2 bits latch the interrupt request from I/O11..0 and CS3..0 respectively:

ID0: is set High when the interrupt is requested from any the I/O11..0 lines.

ID2: is set High when the interrupt is requested from any of the CS3..0 (configured as I/O).

ID0 and ID2 are cleared after reading related I/O register.

ID1 and ID3 are don't care.

Pin-strap value (value=00b):

			0	0	0	0	0

3.1.28 Alarm register (ALARM)

Addr=22h; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
						POR	CKF

CKF=1: If number of PCM clock pulses in one frame period does not match expected value.

POR=1: If a Power On Reset is detected during operation.

The register ALARM is cleared after reading operation only if signals are inactive.

Pin-strap value (value=00h):

						0	0

3.1.29 Interrupt Mask register for Alarm (AMASK)

Addr=23h; Reset Value=11b

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
							MCF

MCF=1: The corresponding alarm bit (CKF) doesn't generate interrupt.

MCF=0: The corresponding alarm bit (CKF) generates interrupt.

Pin-strap value (value=00h):

							1

3.1.30 Loopback register (LOOPB)

Addr=24h; Reset Value=00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DL3	DL2	DL1	DL0	AL3	AL2	AL1	AL0

DL3..0=0: Normal Operation

DL3..0=1: Codec #3..0 is set in Digital Loopback mode, this means that the receive PCM signal applied to the programmed Receive Time Slot is transferred to the programmed Transmit Time Slot.

AL3..0=0: Normal Operation

AL3..0=1: Codec #3..0 is set in Analog Loopback mode, this means that the VFRO signal is transferred to the VFXI input internally into the Codec.

When loopbacks are enabled the signal appears also at the corresponding VFRO output. It is possible to have no signal on the VFRO output programming the GR register to 00h in case of digital loopback.

Pin-strap value (value=00h):

0	0	0	0	0	0	0	0

3.1.31 Transmit Preamplifier Gain register (TXG)

Addr=25h; Reset Value=X0h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
				XG3	XG2	XG1	XG0

XG3..0=0: Transmit preamplifier gain ch. 3..0 = 0dB

XG3..0=1: Transmit preamplifier gain ch. 3..0 = 3.52dB

Overall transmit gain depends on combination of TXG and GTXn registers. For XGn=0 and GTXn=FF 0dBm0 at DX output correspond to -15dBml600. (137mVrms) at VFXI input.

Pin-strap value (value=00h):

				0	0	0	0

3.1.32 Receive Amplifier Gain registers (RXG-10/32)

Addr: 26h; Reset Value=00h

Addr: 27h; Reset Value=00h

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		R12	R11	R10	R02	R01	R00
		R32	R31	R30	R22	R21	R20

Rn2	Rn1	Rn0	Receive amplifier gain ch#n (dB)
0	0	0	Mute
0	0	1	-13.98
0	1	0	-7.96
0	1	1	-4.44
1	0	0	-1.94
1	0	1	0
1	1	0	0
1	1	1	0

Overall receive gain depends on the receive amplifier gain (Rn2..0 setting in RXG reg.) and digital gain (GRXn reg. setting).

As a reference: when Rn2..0 is set for 0dB gain and GRXn=FFh (max. gain) 0dBm0 at DR input correspond to a level at VFRO output equal to 547mVrms (e.g. -3dBm 600ohm)

Pin-strap value:

	Rn2	Rn1	Rn0
GRn = 1	1	1	1
GRn = 0	1	0	0

Overall gain including also GRXn;

GRn = 1: -0.8dB; GRn = 0: -4.3dB.

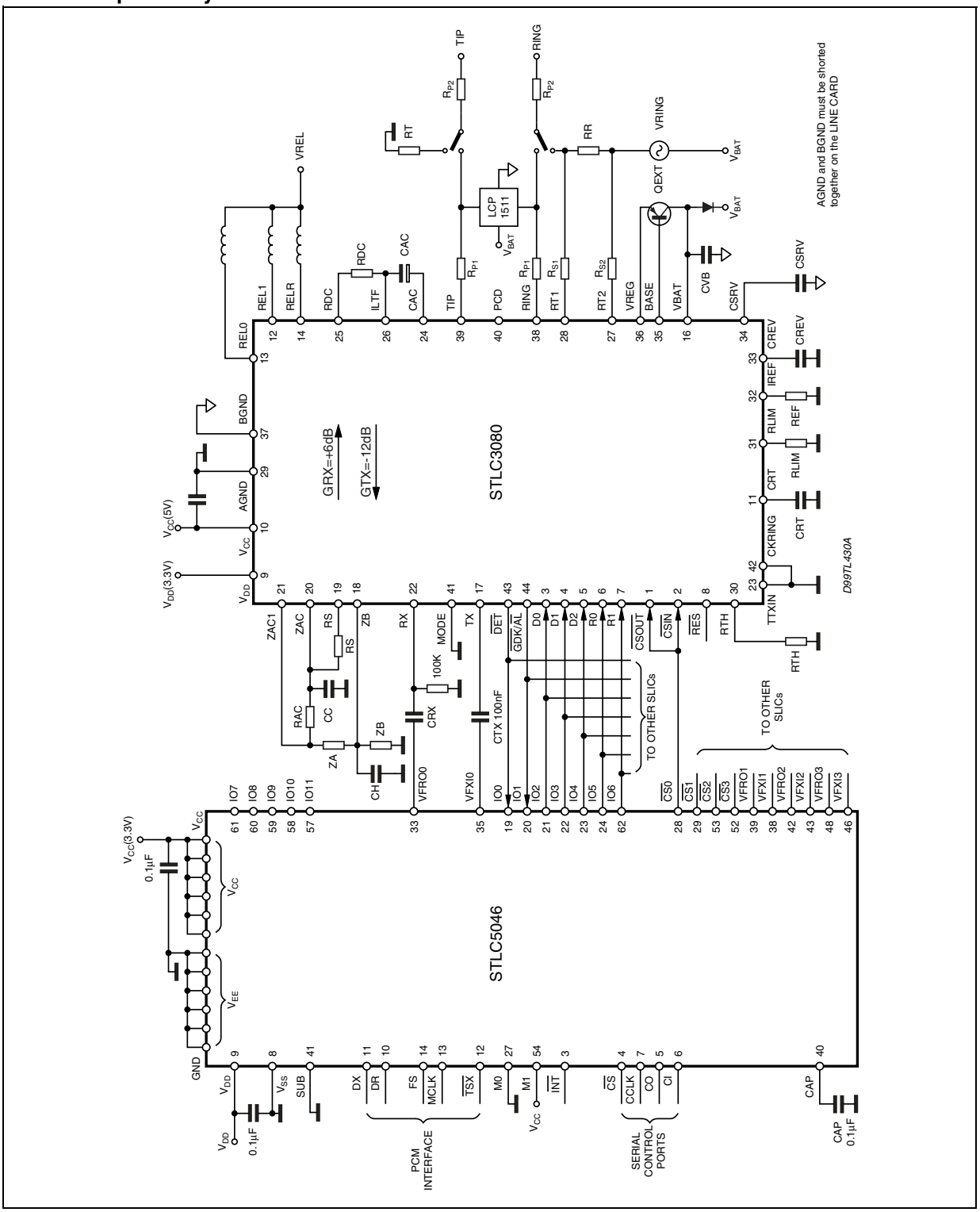
3.1.33 Silicon Revision Identification Code (SR=D)

Addr: 31h; Read Only.

X	X	X	X	0	0	0	0

4 Application circuit

Figure 7. Typical application circuit with STLC3080 without metering pulse injection and I/O pins in dynamic mode



5 Electrical characteristics

(Typical value 25°C and nominal supply voltage. Minimum and maximum value are guaranteed over the temperature 0 to 70°C range by production testing and supply voltage range shown in the Operating Ranges. Performances over -40 to +85°C are guaranteed by product characterization unless otherwise specified.)

Table 6. Electrical characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Digital interface						
Vil	Input voltage low DI pins		0		$0.2V_{DD}$	V
Vih	Input voltage high DI pins(1)		$0.8V_{DD}$		5.5	V
Iil	Input current low DI pins		-10		10	µA
Iih	Input current high DI pins		-10		10	µA
Ci	Input capacitance (all dig. inp.)			5		pF
Vol	Output voltage low DX, TSX pins	Iol = 3.2 mA (other pins Iol = 1mA)	0		0.4	V
Voh	Output voltage high DX pin	Ioh = -3.2 mA (other pins Iol = 1mA)	$0.85V_{DD}$		V_{DD}	V
Analog interface						
RIX	Transmit input amplifier input impedance (VFXI)			1		MΩ
ROR	Receive output impedance (-1.0V < VFRO < 1.0V, IVFRO = 1mA)			1		Ω
Power dissipation						
Idd (pd)	Power down current			9	11	mA
Idd	Active current			48	60	mA
Master clock timing						
f_{MCLK}	Frequency of MCLK	frequency is automatically detected		1.536 1.544 2.048 4.096 8.192		MHz MHz MHz MHz MHz
t_{WMH}	Period of MCLK high	Measured from V_{IH} to V_{IH}	40			ns
t_{WML}	Period of MCLK low	Measured from V_{IL} to V_{IL}	40			ns
t_{RM}	Rise time of MCLK	Measured from V_{IL} to V_{IH}			15	ns
t_{FM}	Fall time of MCLK	Measured from V_{IH} to V_{IL}			15	ns

Table 6. Electrical characteristics (continued)

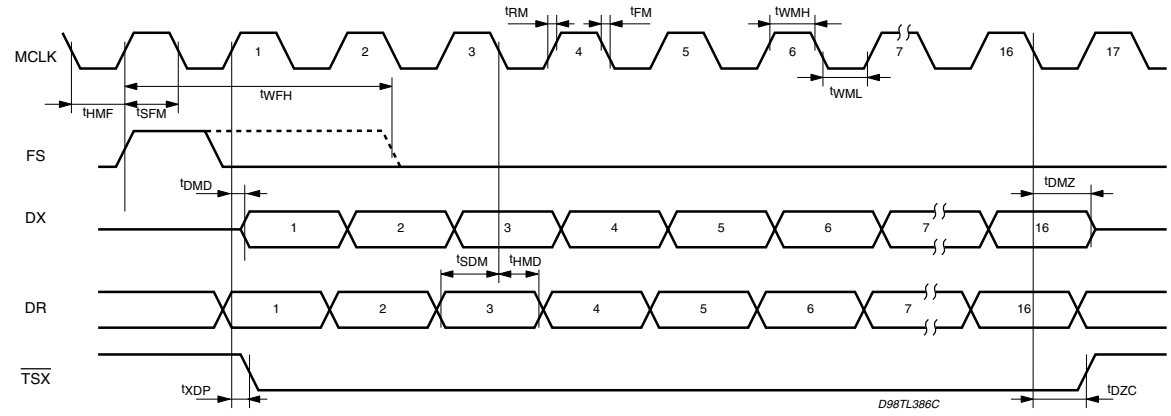
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
PCM interface timing						
t_{HMF}	Hold time MCLK low to FS low		10			ns
t_{SFM}	Setup time, FS high to MCLK low		10			ns
t_{DMD}	Delay time, MCLK high to data valid				10	ns
t_{DMZ}(2)	Delay time, MCLK low to DX disabled	Pull up resistor = 1 kΩ C_{load} = 30 pF	5		40	ns
t_{SDM}	Setup time, D_R valid to MCLK low		15			ns
t_{HMD}	Hold time, MCLK low to D_R invalid		5			ns
t_{DZC}(2)	Delay time, MCLK low to TSX high	Pull up resistor = 1 kΩ C_{load} = 30 pF			40	ns
t_{XDP}	Delay time, MCLK high to TSX low				10	ns
Serial control port timing						
f_{CCLK}	Frequency of CCLK				4.096	MHz
t_{WCH}	Period of CCLK high	Measured from V_{IH} to V_{IH}	100			ns
t_{WCL}	Period of CCLK low	Measured from V_{IL} to V_{IL}	100			ns
t_{RC}	Rise time of CCLK	Measured from V_{IL} to V_{IH}			20	ns
t_{FC}	Fall time of CCLK	Measured from V_{IH} to V_{IL}			20	ns
t_{HCS}	Hold time, CCLK high to CS– low		5			ns
t_{SSC}	Setup time, CS– low to CCLK high		10			ns
t_{SDC}	Setup time, CI valid to CCLK high		20	10		ns
t_{HCD}	Hold time, CCLK high to CI invalid		10			ns
t_{DCD}	Delay time, CCLK low to CO data valid				30	ns
t_{DSD}	Delay time, CS–low to CO data valid				20	ns
t_{DDZ}(2)	Delay time CS–high or 8th CCLK low to CO high impedance whichever comes first	Pull up resistor = 1 kΩ C_{load} = 30 pF			50	ns
t_{HSC}	Hold time, 8th CCLK high to CS– high		10			ns
t_{SCS}	Setup time, CS– high to CCLK high		10			ns

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SLIC control interface timing						
TCS	Chip select repetition rate			31.25		µs
t_{csw}	Chip select pulse width			3.90		µs
t_{DIV}	Time CS low to data input valid				1.65	µs
t_{DII}	Time data input invalid to CS high				1.65	µs
t_{DOA}	Time data output available to CS low		1.8			µs
t_{DON}	Time CS high to data output not available		1.8			µs

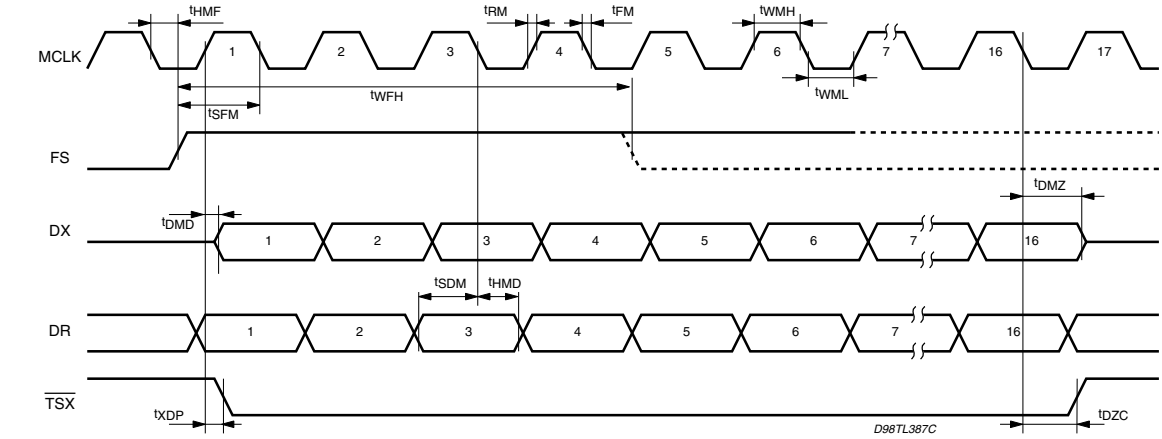
1. All the digital input are five-volt tolerant
   - maximum DC voltage 5.5 V
   - maximum peak voltage 6.5 V
2. It is defined as the time at which the output achieves the off state.

Figure 8. Pin-strap mode short frame sync. timing



Note: T_{WFH} has to be shorter than or equal to 3 MCLK period to select Short Frame.

Figure 9. Pin-strap mode long frame sync. timing



Note: T_{WFH} has to be shorter than or equal to 3 MCLK period to select Short Frame.

Figure 10. MCU mode frame sync. timing

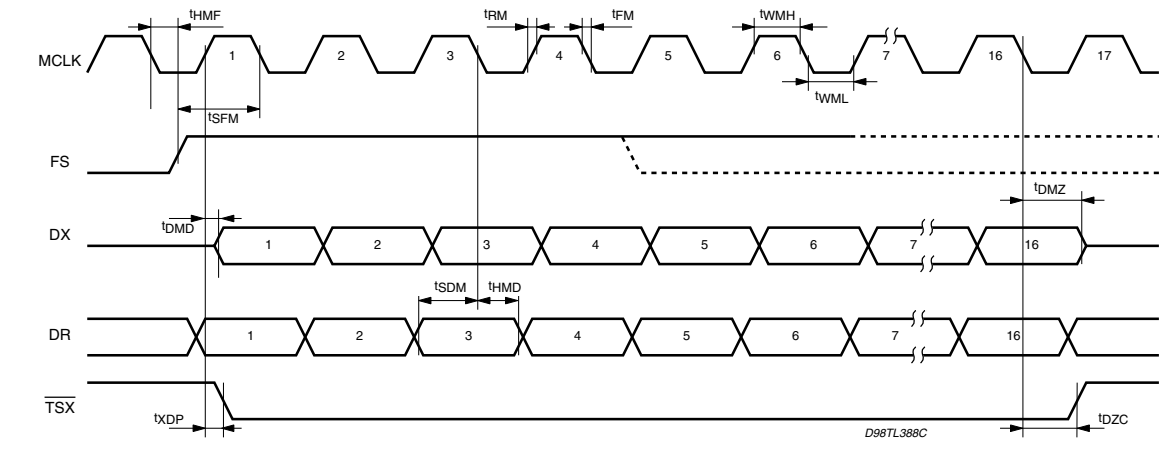


Figure 11. Serial control port timing

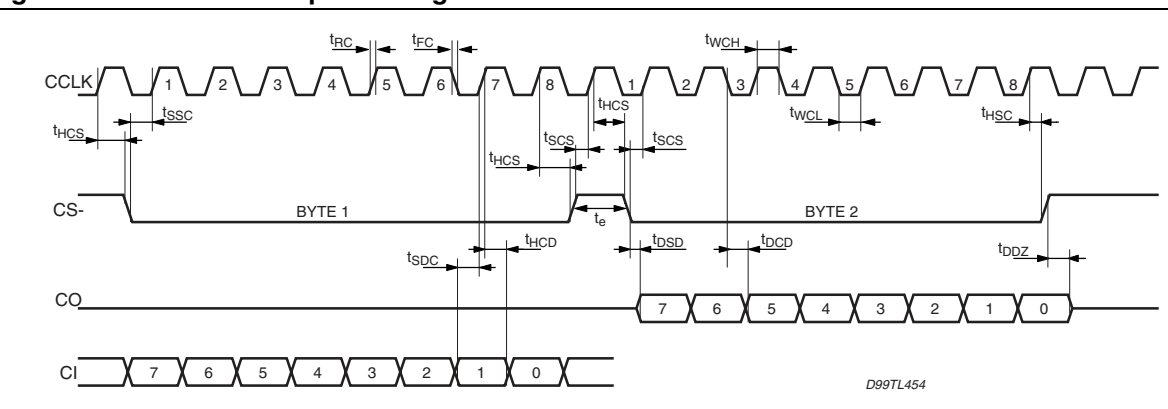
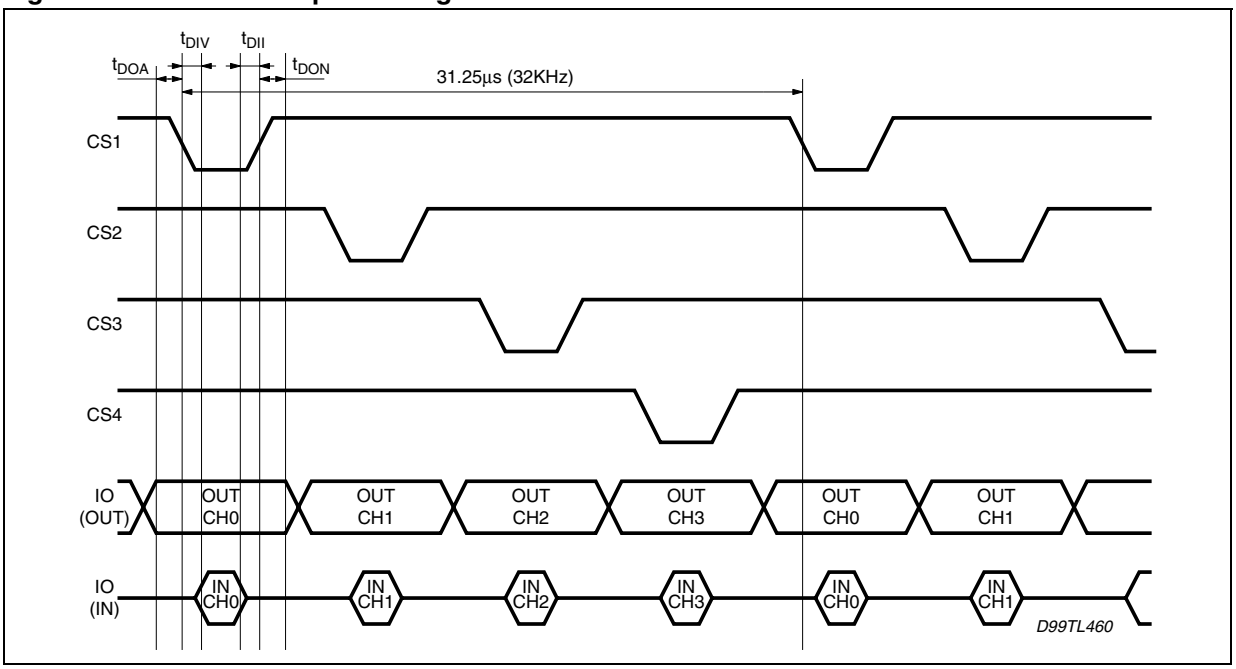


Figure 12. SLIC control port timing



6 Transmission characteristics

Table 7. Transmission characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Transmission transfer characteristics						
	Absolute levels The nominal 0dBm0 levels are: TXG = 0 dB, GTXn = 0 dB (FF)			137		mVrms
GXA	Transmit gain Absolute accuracy	Referred to 0 dB level	-0.15		0.15	dB
GXAG	Transmit gain variation with programmed gain (within 3 dB from max. dig. level)		-0.15		+0.15	dB
GFX	Gain variation with frequency (relative to gain at 1004 Hz); 0 dBm0 input signal 50 Hz 60 Hz 200 Hz 300-3000 Hz 3400 Hz 4000 Hz 4600 Hz and above		 -1.8 -0.15 -0.7		 -20 -20 0 0.15 0 -14.0 -32.0	dB
GAXT	Gain variation with temperature		-0.10		0.10	dB
GAXE	Gain variation with Supplies ±5% 0 dBm0 Input Signal		-0.05		0.05	dB
GTX	Gain Tracking with Tone (1004 Hz µ Law, 820 Hz A Law)	GSX = 3 to -40 dBm0 GSX = -40 to -50 dBm0 GSX = -50 to -55 dBm0	-0.2 -0.4 -1.2		0.2 0.4 1.2	dB
QDX	Quantization distortion with tone (1004 Hz µ Law, 820 Hz A Law)	VFXI = +3 dBm0 VFXI = 0 to -30 dBm0 VFXI = -40 dBm0 VFXI = -45 dBm0 VFXI = -50 to -55 dBm0	33 36 30 25 15			dB
NCT	Transmit Noise C Message Weighted (µ Law)			17	22	dBrnCo
NPT	Transmit Noise Psophometric Weighted (A Law)			-73	-68	dBm0p

Table 7. Transmission characteristics (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DDX(1)	Differential envelope delay (1 to 2.56 kHz input sinewave @ 0dBm0)	500Hz 604Hz 1000Hz 1792Hz 2604Hz 2792Hz			170 110 25 0 70 95	µs
DAX(1)	Absolute delay @ 1 kHz 500 to 2800Hz				420	µs
DPXM	Single frequency distortion (µ Law 0 dBm0 sinewave @ 1004 Hz)				-46	dB
DPXA	Single frequency distortion (A Law 0 dBm0 sinewave @ 820 Hz)				-46	dB
Receive transfer characteristics						
	Absolute levels The nominal 0 dBm) levels are VFRO: RGX = 0 dB, GRXn = 0 db (FF)			547		mVrms
GRA	Transmit gain absolute accuracy (within 3 dB from max. dig. level)	Referred to 0 dB level	-0.15		0.15	dB
GRAG	Receive gain variation with programmed gain		-0.18		+0.18	dB
GFR	Gain variation with frequency (relative to gain at 1004 Hz); 0dBm0 input signal.	Below 200 Hz 200 Hz 300-3000 Hz 3400 Hz 4000 Hz	 -0.25 -0.15 -0.7		0.15 0.15 0.15 0 -14	dB
GART	Gain variation with temperature		-0.1		+0.1	dB
GARE	Gain variation with supplies	0 dBm0 input signal V_{CC}= V_{DD}= 3.3 V ±5%	-0.05		0.05	dB
GTR	Gain Tracking with tone (1004 Hz µ Law, 820 Hz A Law)	DR = 3 to -40 dBm0 DR = -40 to -50 dBm0 DR = -50 to -55 dBm0	-0.2 -0.4 -1.2		0.2 0.4 1.2	dB
QDR	Quantization distortion with tone (1004 Hz µ Law, 820 Hz A Law)	DR = 3 dBm0 DR = 0 to -30 dBm0 DR = -40 dBm0 DR = -45 dBm0 DR = -50 to -55 dBm0	33 36 30 25 15			dB

Table 7. Transmission characteristics (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
GSPR	Out of band spurious noise 0 dBm0 180 to 3400 Hz sinewave at DR				32	dB
NCR	Receive noise C message weighted (µ Law)			5	11	dBrnCo
NPR	Receive noise psophometric weighted (A Law)			-85	-79	dBm0p
DDR(1)	Differential envelope delay (1 to 2.56 kHz input sinewave @ 0 dBm0)	500 Hz 604 Hz 1000 Hz 1792 Hz 2604 Hz 2792 Hz			25 0 0 0 90 115	µs
DAR(1)	Absolute delay @ 1kHz 500 to 2800Hz				440	µs
DPR1	Single frequency distortion (0 dBm0 sinewave @ 1004 Hz)				-46	dB
PSRR	Power supply rejection ratio 1 kHz, 50 mVrms		30			dB
CTX-R	Transmit to receive crosstalk (input signal 200 Hz to 3450 Hz at 0 dBm0)				-76	dB
CTR-X	Receive to transmit crosstalk (input signal 200 Hz to 3450 Hz at 0 dBm0)				-76	dB
CT-ICH	Inter channel crosstalk, TX and TX direction.	Input 200 to 3450Hz at 0dBm0 at VFXI of one channel; all other VFXI inputs and all DR inputs receive idle signal. Output is measured at DX of the 3 idle channels. Input 200 to 3450Hz at 0dBm0 at DR of one channel; all other DR inputs and all VFXI inputs receive idle signal. Output is measured at VFRO of the 3 idle channels.			-78	dB

1. Typical value not tested in production.

7 Package information

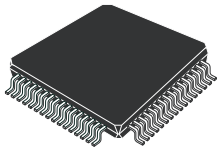
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK® is an ST trademark.

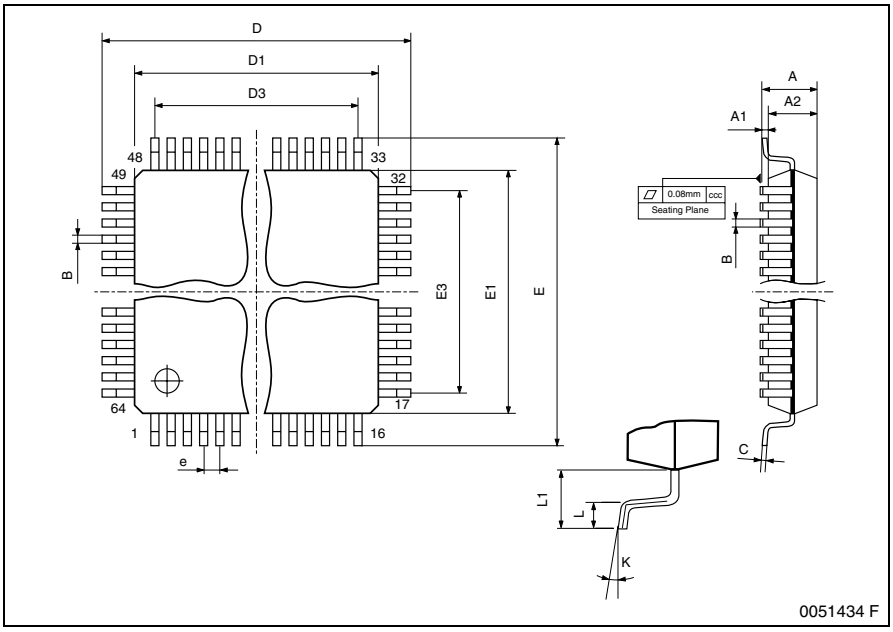
Figure 13. LQFP64 (10 x 10 x 1.4 mm) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.0066	0.0086	0.0106
C	0.09			0.0035		
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		7.50			0.295	
e		0.50			0.0197	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		7.50			0.295	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0393	
K	0° (min.), 3.5° (typ.), 7° (max.)					
ccc			0.080			0.0031

OUTLINE AND MECHANICAL DATA



LQFP64 (10 x 10 x 1.4mm)



8 Revision history

Table 8. Document revision history

Date	Revision	Changes
14-Jan-2004	3	Initial release in EDOCS dms.
22-May-2006	4	Added new part number “E-STLC5046”. Changed look and fill.
20-Aug-2009	5	Updated *Section 7: Package information on page 49*

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com