SiI9136-3/SiI1136 HDMI Deep Color Transmitter

Data Sheet

SiI-DS-1084-D

June 2017

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ACPI	Advanced Configuration and Power Interface
CBUS	Control Bus
CEC	Consumer Electronics Control
CPI	CEC Programming Interface
CSC	Color Space Converters
DDC	Display Data Channel
DSC	Display Stream Compression
DVI	Digital Visual Interface
EDDC	Enhanced Display Data Channel
EDID	Extended Display Identification Data
EMI	Electromagnetic interference
ESD	Electrostatic Discharge
GPIO	General Purpose Input/Output
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HDTV	High-Definition Television
HPD	Hot Plug Detect
I^2C	Inter-Integrated Circuit
KSV	Key Selection Vector
MCLK	Master Clock
SPDIF	Sony/Philips Digital Interface Format
TMDS	Transition Minimized Differential Signaling
TPI	Transmitter Programming Interface
VSIF	Vendor Specific InfoFrame

1. General Description

The Lattice Semiconductor SiI9136-3/SiI1136 transmitter is an HDMI® Deep Color transmitter with 3D and 4K x 2K support for consumer electronics products such as set-top boxes, Blu-ray players and recorders, A/V Receivers, DVD players and recorders, personal video recorders, home theater-in-a-box systems, and home theater PCs. Figure 1.1 shows an example of system architecture using the SiI9136-3/SiI1136 device.

The SiI9136-3/SiI1136 transmitter, with the latest generation 300 MHz TMDS™ core, enables home theater devices to deliver up to 16-bit Deep Color at 1080p/30 resolutions and up to 12-bit Deep Color at 1080p/60 resolutions. On the audio side, high bitrate audio formats such as Dolby® TrueHD and DTS-HD are supported for an enhanced digital audio experience.

1.1. Video Input

- Supports most common standard and nonstandard video input formats
- Supports most common 3D formats
- Supports video resolutions up to 8-bit 4K (30 Hz), 12-bit 1080p (60 Hz), 12-bit 720p/1080i (120 Hz), and 16-bit 1080p (30 Hz)

1.2. Audio Input

- S/PDIF input supports PCM and compressed audio formats (Dolby Digital, DTS, AC-3)
- DSD input supports Super Audio CD applications (SACD)
- I²S input supports PCM, DVD-Audio input (up to 8-channel 192 kHz)
- High Bitrate audio support such as DTS HD and Dolby True HD

1.3. HDMI Output

- DVI, HDCP (on SiI9136-3 only), and HDMI transmitter with xvYCC extended color gamut, Deep Color up to 16-bit color, 3D, and high bitrate audio support
- 300 MHz HDMI transmitter
- Supports all mandatory and some optional 3D modes
- Preprogrammed HDCP key set (on SiI9136-3 only) simplifies the manufacturing process, lowers cost, and provides the highest level of HDCP key security

1.4. Control Capability

- Consumer Electronics Control (CEC) interface that incorporates an HDMI-compliant CEC I/O and the Lattice CEC Programming Interface (CPI) reduces the need for system-level control by the system microcontroller and simplifies firmware overhead
- Four General Purpose I/O (GPIO) pins
- Three dynamic power management modes as required in the Advanced Configuration and Power Interface (ACPI) Specification, according to system needs

1.5. Packaging

- 100-pin, 14 mm x 14 mm, 0.5 mm pitch TQFP package with ePad

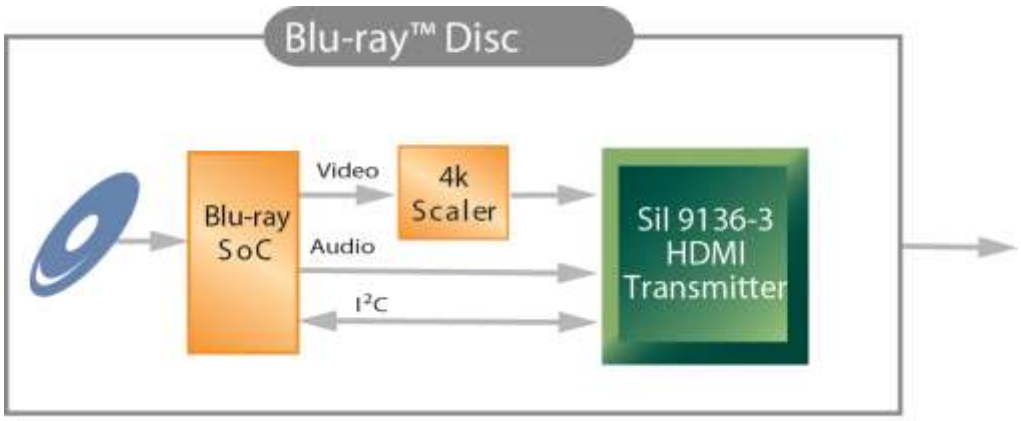


Figure 1.1. Typical Application for Streaming Sticks

2. Product Family

Table 2.1 summarizes the differences between the SiI9136-3/SiI1136 transmitter and the SiI9134 transmitter.

Table 2.1. Product Selection Guide

Transmitter	SiI9134	SiI9136	SiI9136-3/SiI1136
Video Input			
Digital Video Input Ports	1	1	1
I/O Voltage	3.3 V	3.3 V	3.3 V
Core Voltage	1.8 V	1.2 V	1.2 V
Input Pixel Clock Multiply/Divide	0.5x, 2x, 4x	0.5x, 2x, 4x	0.5x, 2x, 4x
Maximum Pixel Input Clock Rate	165 MHz	165 MHz	300 MHz
Maximum TMDS Output Clock	225 MHz	225 MHz	300 MHz
BTA-T1004 Format Support	Yes	Yes	Yes
Video Format Conversion			
36-bit and 30-bit Deep Color	Yes	Yes	Yes
48-bit Deep Color	No	Yes	Yes
xvYCC	No	Yes	Yes
YCbCr → RGB CSC	Yes	Yes	Yes
RGB → YCbCr CSC	Yes	Yes	Yes
4:2:2 → 4:4:4 Upsampling	Yes	Yes	Yes
4:4:4 → 4:2:2 Decimation	Yes	Yes	Yes
16–235 → 0–255 Expansion	Yes	Yes	Yes
0–255 → 16–235 Compression	Yes	Yes	Yes
16–235/240 Clipping	Yes	Yes	Yes
Audio Input			
S/PDIF Input Ports	1	1	1
I²S Input Bits	4 (8-channel)	4 (8-channel)	4 (8-channel)
High Bitrate Audio Support Compressed DTS-HD and Dolby True-HD	Yes	Yes	Yes
One-bit Audio (DSD/SACD)	Yes	Yes[1]	Yes[1]
2-Channel Maximum Sample Rate	192 kHz on I²S 192 kHz on S/PDIF	192 kHz on I²S 192 kHz on S/PDIF	192 kHz on I²S 192 kHz on S/PDIF
8-Channel Maximum Sample Rate	192 kHz	192 kHz	192 kHz
Down Sampling	96 kHz to 48 kHz 192 kHz to 48 kHz	96 kHz to 48 kHz 192 kHz to 48 kHz	96 kHz to 48 kHz 192 kHz to 48 kHz
Internal MCLK Generator	No	Yes[2]	Yes[2]
I²C Address Bus			
Device Address Select	CI2CA Pin	CI2CA Pin	CI2CA Pin
Master DDC Bus	Yes	Yes	Yes
Other			
CEC Interface	No	Yes	Yes
xvYCC Gamut Data	Yes	Yes	Yes
3D Support	Yes	Yes	Yes
Programming Interface	No	Yes	Yes
HDCP Reset	Software Register	Software Register	Software Register
Package	100-pin TQFP	100-pin TQFP	100-pin TQFP

Notes:

1. Shared with I²S Input Interface.
2. Internal MCLK generation is ON by default.
3. HDCP Reset does not apply to the SiI1136 transmitter.

3. Functional Description

Figure 3.1 shows the functional diagram of the SiI9136-3/SiI1136 transmitter. Pin descriptions begin on page 23. A description of each of the blocks shown in the diagram follows the figure. The power domains are described in the Power Domains section on page 29.

Note: HDCP blocks do not apply to the SiI1136 transmitter.

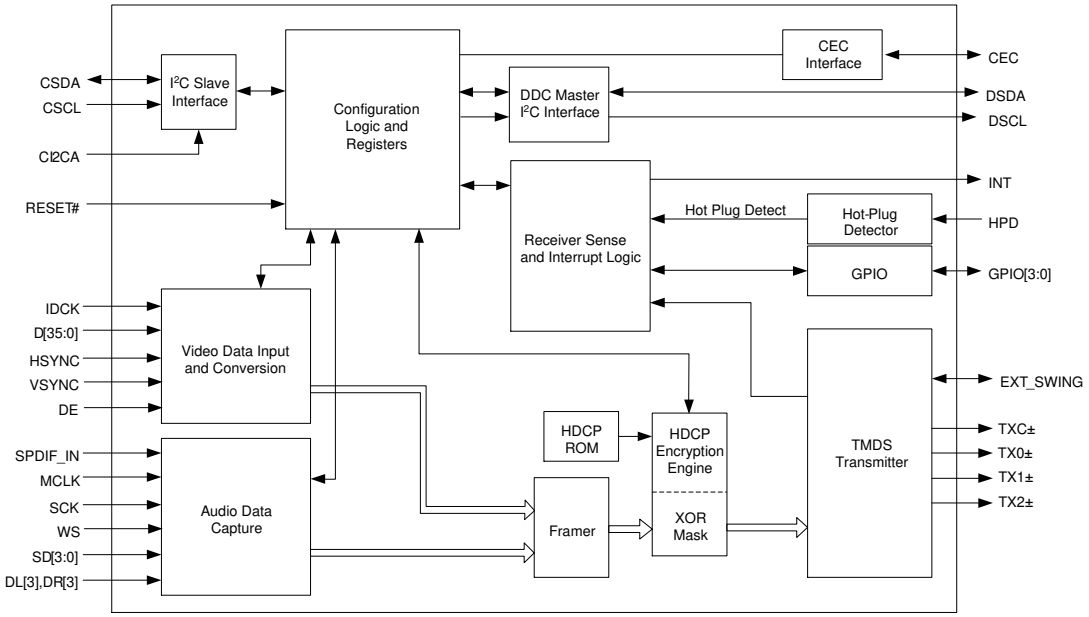


Figure 3.1. SiI9136-3/SiI1136 Functional Block Diagram

3.1. Video Data Input and Conversion

Figure 3.2 shows the video data processing stages through the transmitter. Each of the processing blocks can be bypassed by setting the appropriate register bits. The HSYNC and VSYNC input signals are required, except in embedded sync modes. The DE input signal is optional, because it can be created with the DE generator using the HSYNC and VSYNC signals.

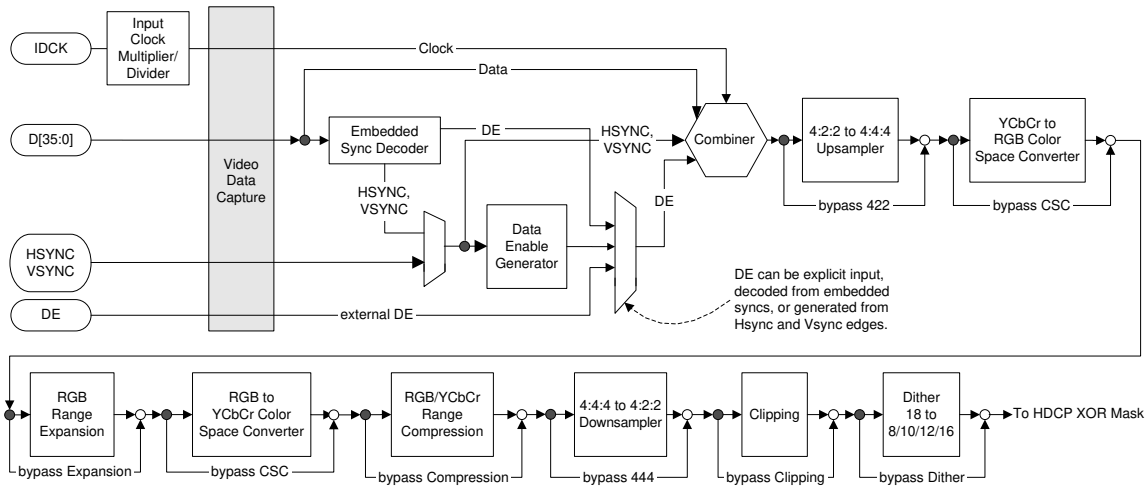


Figure 3.2. Transmitter Video Data Processing Path

3.1.1. Input Clock Multiplier/Divider

The input pixel clock can be multiplied by 0.5, 2, or 4. Video input formats that use a 2x clock, such as YC Mux mode, can be transmitted across the HDMI link with a 1x clock. Similarly, 1x-to-2x, 1x-to-4x, and 2x-to-4x conversions are possible.

3.1.2. Video Data Capture

The bus configurations support most standardized video input formats as well as other widely used non-standard formats. Each configuration has four key attributes: data width, input mode, clock mode, and synchronization.

The video input port is a 36-bit wide bus that can be configured to any of the following data widths:

- 8-, 10-, or 12-bit input in double speed clock mode
- 12-, 15-, 18-, or 24-bit input in dual edge clock mode
- 16-, 20-, 24-, 30-, or 36-input in single speed clock mode

The input mode includes color format such as RGB, YCbCr, or xvYCC, and color sampling such as 4:4:4 or 4:2:2.

Clock mode refers to the input clock rate relative to the pixel clock rate. The SiI9136-3/SiI1136 device supports 1x mode and 2x mode, or dual edge mode. 1x mode and 2x mode means that the input clock operates at one or two times the pixel clock rate. Dual edge mode means that the input clock rate equals the pixel clock rate, but a sample is captured on both the rising edge and the falling edge of the input clock. Thus, with the Video Input configured for 24 bits with a dual edge clock, 48 bits of video data are received per clock cycle. The 24 MSBs of the video data are latched on the first clock edge, and the 24 LSBs are latched on the next clock edge. The first clock edge is programmable and can be either the rising or falling edge.

Synchronization attributes refer to how the horizontal and vertical sync signals are configured. Separate synchronization involves placing the horizontal sync, vertical sync, and data enable signals on separate input pins. Embedded synchronization combines these signals with one or more of the data inputs.

3.1.3. Embedded Sync Decoder

The transmitter can create DE, HSYNC, and VSYNC signals using the Start of Active Video (SAV) and End of Active Video (EAV) codes within the ITU-R BT.656-format video stream.

3.1.4. Data Enable Generator

The transmitter includes logic to construct a Data Enable (DE) signal from the incoming HSYNC, VSYNC, and IDCK. This signal is used to correct timing from sync extraction to conform to CEA-861D timing specifications. By programming registers, the DE signal can define the size of the active display region. This feature is particularly useful when the transmitter connects to MPEG decoders that do not provide a specific DE output signal.

3.1.5. Combiner

The clock, data, and sync information is combined into a complete set of signals required for TMDS encoding. From here, the signals are manipulated by the register-selected video processing blocks.

3.1.6. 4:2:2 to 4:4:4 Upsampler

Chrominance upsampling doubles the number of chrominance samples per line, converting 4:2:2 sampled video to 4:4:4.

3.1.7. RGB Range Expansion

The SiI9136-3/SiI1136 transmitter can scale the input color range from limited-range into full-range using the range expansion block. When enabled by itself, the range expansion block expands 16–235 (64–943 to 256–3775, 4096-60415 for 30/36/48-bit color depth) limited-range data into 0–255 (0–1023, 0–4095 to 0-65535 for 30/36/48-bit color depth) full-range data for each video channel. When range expansion and the YCbCr to RGB color space converter are both enabled, the input conversion range for the Cb and Cr channels is 16–240 (64–963, 256–3855 to 4096-61695 for 30/36/48-bit color depth).

3.1.8. Color Space Converter

Two Color Space Converters (CSCs) (YCbCr to RGB and RGB to YCbCr) are available to interface to the many video formats supplied by A/V processors and to provide full DVI backward compatibility. The CSC can be adjusted to perform standard-definition conversions (ITU.601) or high-definition conversions (ITU.709) by setting the appropriate registers.

3.1.9. RGB/YCbCr Range Compression

When enabled by itself, the range compression block compresses 0–255/0–1023/0–4095/0–65535 full-range data into 16–235/64–943/256–3775/4096–60415 limited-range data for each video channel. When enabled with the RGB to YCbCr converter, this block compresses to 16–240/64–963/256–3855/4096–61695 for the Cb and Cr channels. The color range scaling is linear.

3.1.10. 4:4:4 to 4:2:2 Downsampler

Downsampling reduces the number of chrominance samples per line by half, converting 4:4:4 sampled video to 4:2:2.

3.1.11. Clipping

The clipping block, when enabled, clips the values of the output video to 16–235 for RGB video or the Y channel, and to 16–240 for the Cb and Cr channels.

3.1.12. 18-to-8/10/12/16-Dither

The 18-to-8/10/12/16-dither block dithers internally processed, 18-bit data to 8, 10, 12, or 16 bits for output on the HDMI link. It can be bypassed to output 10/12-bit modes when supplied by the A/V processor or converted in the decimator and CSC.

3.2. Audio Data Capture

The audio capture block supports I^2S, Direct Stream Digital, and S/PDIF audio input formats. The appropriate registers must be configured to describe the audio format provided to the SiI9136-3/SiI1136 transmitter. This information is passed over the HDMI link in the CEA-861D Audio Info (AI) packets.

3.3. Framer

The framer block handles the packetizing and framing of the data stream sent across the HDMI link. Audio and video data packets are inserted into the respective HDMI Video Data and Data Island periods. This block handles the correct insertion of all HDMI packet types.

3.4. HDCP Encryption Engine/XOR Mask

The HDCP encryption engine contains the logic necessary to encrypt the incoming audio and video data and includes support for HDCP authentication and repeater checks. The system microcontroller or microprocessor controls the encryption process by using a set sequence of register reads and writes. An algorithm uses HDCP keys and a Key Selection Vector (KSV) stored in the HDCP key ROM to calculate a number that is then applied to an XOR mask. This process encrypts the audio and video data on a pixel-by-pixel basis during each clock cycle. The HDCP encryption engine/XOR mask does **not** apply to the SiI1136 transmitter.

3.5. HDCP Key ROM

The SiI9136-3/SiI1136 transmitter comes preprogrammed with a set of production HDCP keys stored in an internal ROM. System manufacturers do not need to purchase key sets from the Digital-Content Protection LLC. Lattice Semiconductor handles all purchasing, programming, and security for the HDCP keys. The preprogrammed HDCP keys provide the highest level of security because there is no way to read the keys once the device is programmed. Customers must sign the HDCP license agreement (www.digital-cp.com) or be under a specific NDA with Lattice Semiconductor before receiving SiI9136-3/SiI1136 samples.

The SiI1136 transmitter is functionally equivalent to the SiI9136-3 except the HDCP keys are not preprogrammed and therefore does not support HDCP encryption.

3.6. TMDS Transmitter

The TMDS digital core performs 8-to-10-bit TMDS encoding on the data received from the HDCP XOR mask, and is then sent over three TMDS data and a TMDS clock differential lines. A resistor connected to the EXT_SWING pin controls the swing amplitude of the TMDS signal.

3.7. GPIO

The SiI9136-3/SiI1136 transmitter has four General Purpose I/O pins. Each pin supports the following functions:

- Input mode: The value can be read through local I^2C bus access; an interrupt can be generated on either the falling or the rising edge of the input signal.
- Output mode: The value can be set through the local I^2C bus access.

3.8. Hot Plug Detector

When HIGH, the Hot Plug Detection signal indicates to the transmitter that the EDID of the connected receiver is readable. A HIGH voltage is at least 2.0 V, and a LOW voltage is less than 0.8 V.

3.9. CEC Interface

The Consumer Electronics Control (CEC) Interface block provides CEC-compliant signals between CEC devices and a CEC master. A CEC controller compatible with the Lattice Semiconductor CEC API is included on-chip. The controller has a high-level register interface accessible through the I^2C interface, and can be used to send and receive CEC commands. This controller makes CEC control easy and straightforward by removing the burden of programming the host processor to perform these low-level transactions on the CEC bus. See the *CEC Programming Interface (CPI) Programmer Reference* for details on the API (see the Lattice Semiconductor Documents section on page 52). *The Programmer's Reference requires an NDA with Lattice Semiconductor.*

3.10. DDC Master I^2C Interface

The host uses the DDC master logic to read the EDID by programming the target address, offset, and number of bytes. Upon completion, or when the DDC master FIFO becomes full, an interrupt signal is sent to the host so that the host can read data out of the FIFO.

The TPI hardware uses the DDC master logic to carry out HDCP authentication tasks. The arbitration logic arbitrates the access from host and the internal TPI hardware. See the Internal DDC Master section on page 30 for more information.

3.11. Receiver Sense and Interrupt Logic

The Interrupt logic of this block buffers interrupt events from different sources. Receiver Sense and Hot Plug Interrupts are also available in power down mode. The logic for handling these interrupts when all clocks are disabled is also part of this block. The INT pin provides an interrupt signal to the system microcontroller when any of the following occur:

- Monitor Detect (either from the HPD input level or from the Receiver Sense feature) changes
- VSYNC (useful for synchronizing a microcontroller to the vertical timing interval)
- Error in the audio format
- DDC FIFO status change
- HDCP authentication error.

3.12. Configuration Logic and Registers

This block contains the configuration registers that control the operation of the transmitter. The registers are accessed via the I^2C interface. This block also contains logic for simplifying the configuration of the transmitter by automatically programming different parameters.

3.13. I^2C Slave Interface

The controller I^2C interface on the transmitter (signals CSCL and CSDA) is a slave interface with an operating frequency from 3 kHz to 400 kHz and with an input tolerance of up to 4.0 V when all device operating voltages are present. The host uses this interface to configure the transmitter by reading from and writing to appropriate registers.

4. Electrical Specifications

4.1. Absolute Maximum Conditions

Table 4.1. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC33	I/O Pin Supply Voltage	–0.3	—	4.0	V	2
CVCC12	Digital Core Supply Voltage	–0.5	—	1.5	V	2
AVCC	Analog Supply Voltage 1.2 V	–0.5	—	1.5	V	2
V_I	Input Voltage	–0.3	—	IOVCC + 0.3	V	—
V_O	Output Voltage	–0.3	—	IOVCC + 0.3	V	—
T_J	Junction Temperature	—	—	125	°C	—
T_{STG}	Storage Temperature	–65	—	150	°C	—

Notes:
1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described in the Normal Operating Conditions section.

4.2. Normal Operating Conditions

Table 4.2. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC33	I/O Pin Supply Voltage	3.135	3.3	3.465	V	—
CVCC12	Digital Core Supply Voltage	1.14	1.2	1.26	V	—
AVCC	Analog Supply Voltage, 1.2 V	1.14	1.2	1.26	V	—
V_{CCN}	Supply Voltage Noise Tolerance	—	—	100	mV_{P-P}	*
T_A	Ambient Temperature (with power applied)	0	25	70	°C	—
Θ_{ja}	Thermal Resistance (Theta JA)	—	—	29.3	°C/W	—
Θ_{jc}	Junction to case resistance (Theta JC)	—	—	12.8	°C/W	—

***Note:** The supply voltage noise is measured at test point VCCTP. See Figure 4.1. The ferrite bead provides filtering of power supply noise. The figure is representative and applies to the IOVCC33, CVCC12, and AVCC pins.

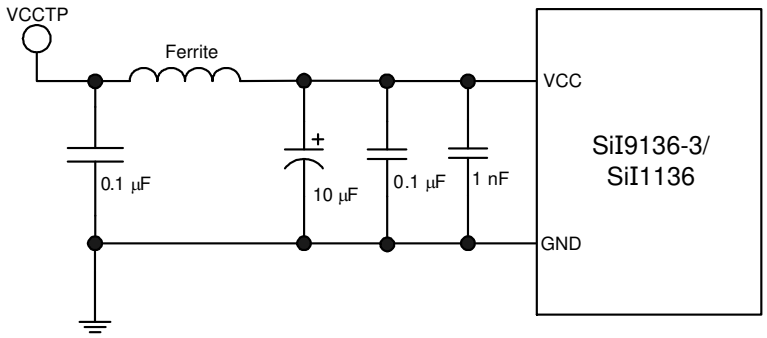


Figure 4.1. VCCTP Test Point for VCC Noise Tolerance

4.2.1. I/O Specifications

Under normal operating conditions unless otherwise specified.

Table 4.3. DC Digital I/O Specifications

Symbol	Parameter	Signal Type	Conditions	Min	Typ	Max	Units
V_{IH}	HIGH-level Input Voltage*	LVTTL	—	2.0	—	5.5	V
V_{IL}	LOW-level Input Voltage*			–0.3	—	0.8	V
VTH+	LOW to HIGH Threshold	Schmitt	RESET#, CSCL, CSDA	1.9	—	—	V
VTH-	HIGH to LOW Threshold			—	—	0.7	V
V_{TH+}	LOW to HIGH Threshold	Schmitt	DSCL, DSDA	3.0	—	—	V
V_{TH-}	HIGH to LOW Threshold			—	—	1.5	V
V_{TH+}	LOW to HIGH Threshold	Schmitt	CEC_A	2.0	—	—	V
V_{TH-}	HIGH to LOW Threshold			—	—	0.8	V
V_{OH}	HIGH-level Output Voltage	LVTTL	—	2.4	—	—	V
V_{OL}	LOW-level Output Voltage			—	—	0.4	V
I_{OZ}	High Impedance Output Leakage Current	—	@ V_O = 3.3 V or 0 V	–10	—	10	µA
I_{OH}	HIGH level Output Current	—	@ V_{OH} {Min}	—	—	8	mA
I_{OL}	LOW level Output Current	—	@ V_{OL} {Max}	—	—	8	mA

***Note:** All unused input signals should be tied LOW.

Table 4.4. TMDS I/O Specifications

Symbol	Parameter	Signal Type	Conditions	Min	Typ	Max	Units
V_{OD}	Differential outputs: single-ended swing amplitude*	TMDS	R_{LOAD} = 50 Ω R_{EXT_SWING} as defined in the Pin Descriptions section	400	500	600	mV
V_{ODD}	Differential outputs: differential swing amplitude	TMDS	—	800	1000	1200	mV
V_{DOH}	Differential HIGH level output voltage	TMDS	≤ 165 MHz TMDS clock	AVCC – 10 mV	—	AVCC + 10 mV	V
			> 165 MHz TMDS clock	AVCC – 200 mV	—	AVCC + 10 mV	V
V_{DOL}	Differential LOW level output voltage	TMDS	≤ 165 MHz TMDS clock	AVCC – 600 mV	—	AVCC – 400 mV	V
			> 165 MHz TMDS clock	AVCC – 700 mV	—	AVCC – 400 mV	V
I_{DOS}	Differential output short circuit current	TMDS	V_{OUT} = 0 V	—	—	5	µA

***Note:** Single-ended swing amplitude limits are defined by the HDMI Specification.

4.2.2. DC Power Supply Specifications

Table 4.5 shows the power consumption in the three power modes. Measurement uses Dot Moiré pattern with 8-chanel I²S audio and HDCP enabled.

Table 4.5. DC Specifications

Symbol	Parameter	Mode	Frequency[1]	IOVCC33		AVCC		CVCC12		Units
				Typ	Max	Typ	Max	Typ	Max	
I_{PON}	Power On Current	D0	74.25 MHz	1.8	1.7	10.9	12.2	36.3	40.0	mA
			148.5 MHz	3.6	3.1	18.2	20.3	68.4	75.6	mA
			225 MHz	4.7	3.8	25.4	28.3	83.9	92.9	mA
			297 MHz	3.8[2]	3.2[2]	33.1	37.3	94.9	105.2	mA
I_{PSTBY}	Power Standby Current	D2	—	4.70		0.50		9.10		mA
I_{POFF}	Power Off current	D3	—	4.70		0.50		5.10		mA

Notes:
1. TMDS clock frequency does not matter in D3 and D2 modes.
2. Current measurement for IOVCC33 is lower at 297 MHz since only 24-bits per pixel is used. At 225 MHz used for deep color, each pixel is 36-bits wide.

4.3. AC Specifications

4.3.1. Video/HDMI Timing Specifications

Under normal operating conditions unless otherwise specified.

Table 4.6. Video Input AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
T_{DDF}	VSYNC and HSYNC Delay from DE falling edge	—	1	—	—	T_{CIP}	Figure 4.6
T_{DDR}	VSYNC and HSYNC Delay to DE rising edge	—	1	—	—	T_{CIP}	Figure 4.6
T_{HDE}	DE HIGH Time	—	—	—	8191	T_{CIP}	Figure 4.7
T_{LDE}	DE LOW Time	—	138*	—	—	T_{CIP}	Figure 4.7

***Note:** T_{LDE} minimum is defined for HDMI mode carrying 480p video with 192 kHz audio, which requires at least 138 pixel clock cycles of blanking to carry the audio packets. If only HDCP is running, the minimum DE LOW time is 58 clock cycles, according to the HDCP Specification. If neither HDCP nor audio are running, the minimum DE LOW time is 12 clock cycles for TMDS. The minimum vertical blanking time is three horizontal line times.

Table 4.7. TMDS AC Output Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
S_{LHT}	Differential Swing LOW-to-HIGH Transition Time	REXT_SWING = 3.83 kΩ Internal Source Termination On	95.5	—	181.81	ps	Figure 4.10
S_{HLT}	Differential Swing HIGH-to-LOW Transition Time	REXT_SWING = 3.83 kΩ Internal Source Termination On	86.5	—	172.3	ps	Figure 4.10

Notes:
1. These limits are defined by the HDMI Specification.
2. Refer to the Source Termination section on page 31 for information about internal source termination.

4.3.2. Audio AC Timing Specifications

Table 4.8. S/PDIF Input Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
F_{S_SPDIF}	Sample Rate	2 Channel	32	—	192	kHz	—	—
T_{SPCYC}	S/PDIF Cycle Time	C_L = 10 pF	—	—	1.0	UI	Figure 4.12	1
T_{SPDUTY}	S/PDIF Duty Cycle	C_L = 10 pF	90%	—	110%	UI	Figure 4.12	1
$T_{MCLKCYC}$	MCLK Cycle Time	C_L = 10 pF	13.3	—	—	ns	Figure 4.13	3
F_{MCLK}	MCLK Frequency	C_L = 10 pF	—	—	75	MHz	—	3
$T_{MCLKDUTY}$	MCLK Duty Cycle	C_L = 10 pF	40%	—	60%	$T_{MCLKCYC}$	Figure 4.13	3
T_{AUDDLY}	Audio Pipeline Delay	—	—	30	70	µs	—	4

Note: Refer to the notes for Table 4.10.

Table 4.9. I²S Input Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
F_{S_I2S}	Sample Rate	—	32	—	192	kHz	—	—
T_{SCKCYC}	I²S Cycle Time	C_L = 10 pF	—	—	1.0	UI	Figure 4.11	1
$T_{SCKDUTY}$	I²S Duty Cycle	C_L = 10 pF	90%	—	110%	UI	Figure 4.11	—
T_{I2SSU}	I²S Setup Time	C_L = 10 pF	15	—	—	ns	Figure 4.11	2
T_{I2SHD}	I²S Hold Time	C_L = 10 pF	0	—	—	ns	Figure 4.11	2

Note: Refer to the notes for Table 4.10.

Table 4.10. DSD Input Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
F_{S_DSD}	Sample Rate	—	—	44.1	88.2	kHz	—	—
T_{DCKCYC}	DSD Cycle Time	C_L = 10 pF	—	—	2.0	UI	Figure 4.14	1
$T_{DCKDUTY}$	DSD Duty Cycle	C_L = 10 pF	90%	—	110%	UI	Figure 4.14	1
T_{DSDSU}	DSD Setup Time	C_L = 10 pF	20	—	—	ns	Figure 4.14	—
T_{DSDHD}	DSD Hold Time	C_L = 10 pF	20	—	—	ns	Figure 4.14	—

Notes:

1. Proportional to unit time (UI) according to sample rate. Refer to the I²S, S/PDIF, or DSD Specifications.
2. Setup and hold minimum times are based on 13.388 MHz sampling, which is adapted from Figure 3 of the Philips I²S Specification.
3. If a separate master clock input (MCLK) is used for time-stamping purposes, it has to be coherent with the audio input. *Coherent* means that the MCLK and audio input have been created from the same clock source. This requirement usually uses the original MCLK to strobe the audio out from the sourcing chip.
4. Audio pipeline delay is measured from the transmitter input pins to the TMDS output.

4.3.3. Video AC Timing Specifications

Under normal operating conditions unless otherwise specified.

Table 4.11. Video AC Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{CIP}	IDCK period, one pixel per clock	—	3.3	—	40	ns	Figure 4.2	1
F_{CIP}	IDCK frequency, one pixel per clock	—	25	—	300	MHz	—	1
T_{CIP12}	IDCK period, dual-edge clock	—	12.3	—	40	ns	Figure 4.2	2
F_{CIP12}	IDCK frequency, dual-edge clock	—	25	—	82.5	MHz	—	2
T_{DUTY}	IDCK duty cycle	—	45%	—	55%	T_{CIP}	Figure 4.2	—
T_{IJIT}	Worst case IDCK clock jitter, DJ	—	—	—	0.20	T_{BIT}	—	3, 4
	Worst case IDCK clock jitter, RJ	—	—	—	0.25	T_{BIT}	—	
T_{SIDF}	Setup time to IDCK falling edge	EDGE = 0	1.36	—	—	ns	Figure 4.4	5
T_{HIDF}	Hold time to IDCK falling edge		0.45	—	—	ns		
T_{SIDR}	Setup time to IDCK rising edge	EDGE = 1	1.57	—	—	ns	Figure 4.3	5
T_{HIDR}	Hold time to IDCK rising edge		1.16	—	—	ns		
T_{SIDD}	Setup time to IDCK rising or falling edge	Dual-edge clocking	1.57	—	—	ns	Figure 4.5	6
T_{HIDD}	Hold time to IDCK rising or falling edge		1.16	—	—	ns		

Notes:

1. T_{CIP} and F_{CIP} apply in single-edge clocking modes. T_{CIP} is the inverse of F_{CIP} and is not a controlling specification.
2. T_{CIP12} and F_{CIP12} apply in dual-edge mode. T_{CIP12} is the inverse of F_{CIP12} and is not a controlling specification.
3. T_{BIT} is the TMDS bit time.
4. Total jitter (TJ) is calculated from DJ (deterministic jitter), RJ (random jitter, rms) and required BER (Bit Error Rate). For BER of 1E-9, TJ = DJ + 12 • RJ = 3.2 T_{BIT}.
5. Setup and hold time specifications apply to Data, DE, VSYNC, and HSYNC input pins, relative to IDCK input clock.
6. Setup and hold limits are not affected by the setting of the EDGE bit for 12/15/18/24-bit dual-edge clocking mode.

4.3.4. Control Signal Timing Specifications

Under normal operating conditions unless otherwise specified.

Table 4.12. Control Signal Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Note
T_{RESET}	RESET# signal LOW time required for reset	—	50	—	—	µs	Figure 4.8 Figure 4.9	1, 5
T_{I2CDVD}	SDA Data Valid Delay from SCL falling edge on READ command	CL = 400pF	—	—	700	ns	Figure 4.15	2, 6
T_{HDDAT}	I^2C data hold time	0–400 kHz	2.0	—	—	ns	—	3, 6
T_{INT}	Response time for INT output pin from change in input condition (HPD, Receiver Sense, VSYNC change, etc.).	RESET# = HIGH	—	—	100	µs	—	—
F_{SCL}	Frequency on master DDC SCL signal	—	40	70	100	kHz	—	4
F_{CSCL}	Frequency on master CSCL signal	—	40	—	400	kHz	—	—

Notes:

1. Reset on RESET# signal can be LOW as the supply becomes stable (shown in Figure 4.8), or pulled LOW for at least T_{RESET} (shown in Figure 4.9).
2. All standard-mode (100 kHz) I^2C timing requirements are guaranteed by design. These timings apply to the slave I^2C port (pins CSDA and CSCL) and to the master I^2C port (pins DSDA and DSCL).
3. This minimum hold time is required by CSCL and CSDA signals as an I^2C slave. The device does not include the 300 ns internal delay required by the I^2C Specification (Version 2.1, Table 5, note 2).
4. The master DDC block provides an SCL signal for the E-DDC bus. The HDMI Specification limits this to I^2C Standard Mode or 100 kHz. Use of the Master DDC block does not require an active IDCK.
5. Not a Schmitt trigger.
6. Operation of I^2C pins above 100 kHz is defined by LVTTL levels V_{IH}, V_{IL}, V_{OH}, and V_{OL} (see Table 4.3 on page 15). For these levels, I^2C speeds up to 400 kHz are supported.

4.3.5. CEC Timing Specifications

See the HDMI 1.4 Specification – Supplement 1 Consumer Electronics Control (CEC).

4.4. Timing Diagrams

4.4.1. Input Timing Diagrams

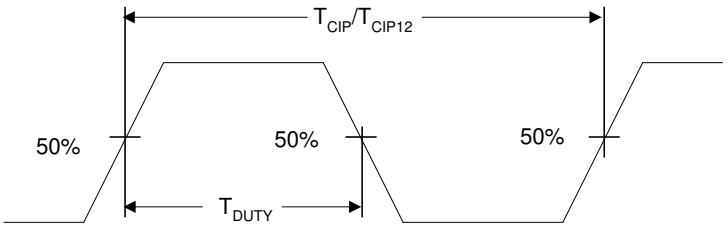
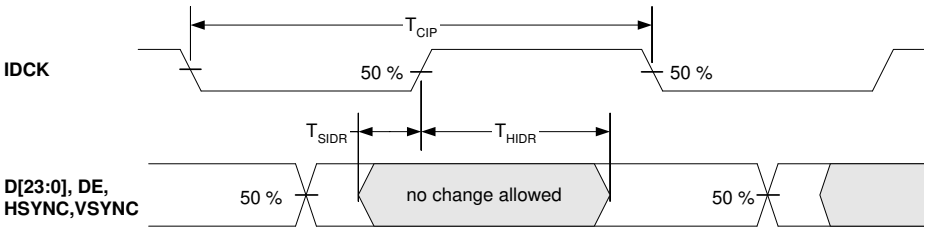
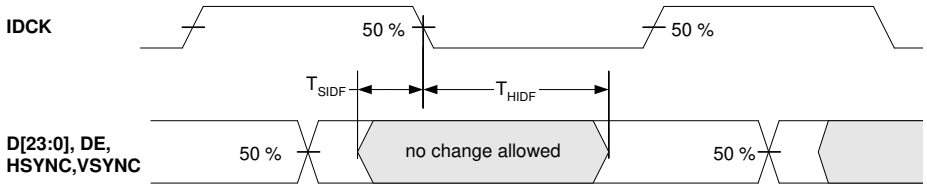


Figure 4.2. IDCK Clock Duty Cycle



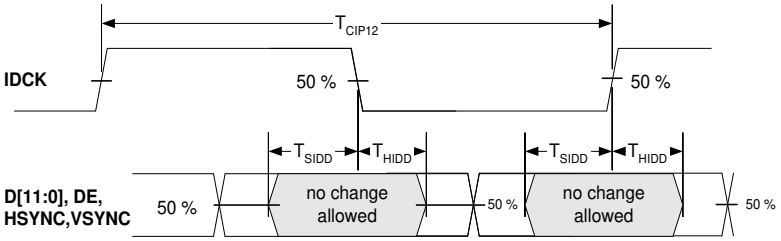
Signals may change only in the unshaded portion of the waveform, to meet both the minimum setup and minimum hold time specifications.

Figure 4.3. Control and Data Single-Edge Setup and Hold Times—EDGE = 1



Signals may change only in the unshaded portion of the waveform, to meet both the minimum setup and minimum hold time specifications.

Figure 4.4. Control and Data Single-Edge Setup and Hold Times—EDGE = 0



Signals may change only in the unshaded portion of the waveform, to meet both the minimum setup and minimum hold time specifications.

Figure 4.5. Control and Data Dual-Edge Setup and Hold Times

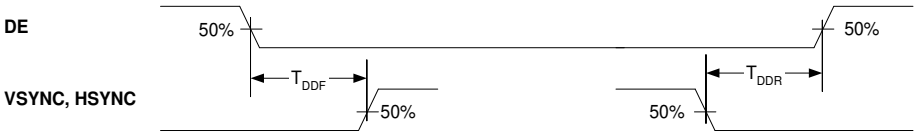


Figure 4.6. VSYNC and HSYNC Delay Times Based on DE

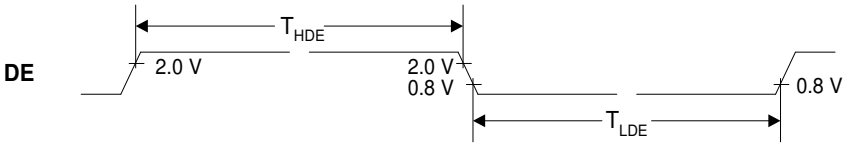


Figure 4.7. DE HIGH and LOW Times

4.4.2. Reset Timing Diagrams

VCC must be stable between its limits listed in the Normal Operating Conditions section on page 14 for T_{RESET} before RESET# goes HIGH, as shown in Figure 4.8. Before accessing registers, RESET# must be pulled LOW for T_{RESET}. This can be done by holding RESET# LOW until T_{RESET} after stable power, as described above, or by pulling RESET# LOW from a HIGH state for at least T_{RESET}, as shown in Figure 4.9.

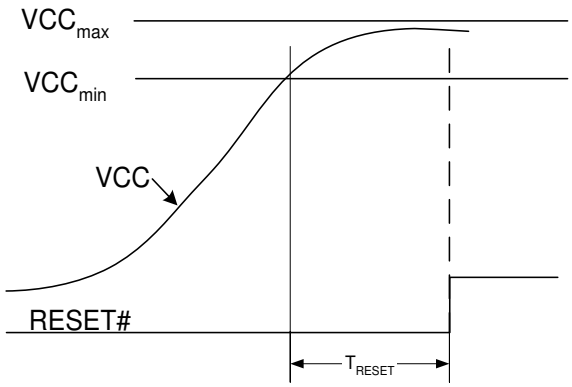


Figure 4.8. Conditions for Use of RESET#

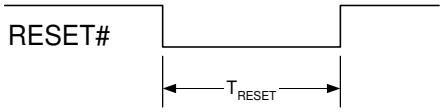


Figure 4.9. RESET# Minimum Timings

4.4.3. TMDS Timing Diagram

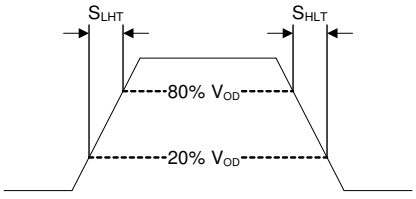


Figure 4.10. Differential Transition Times

4.4.4. Audio Timing Diagrams

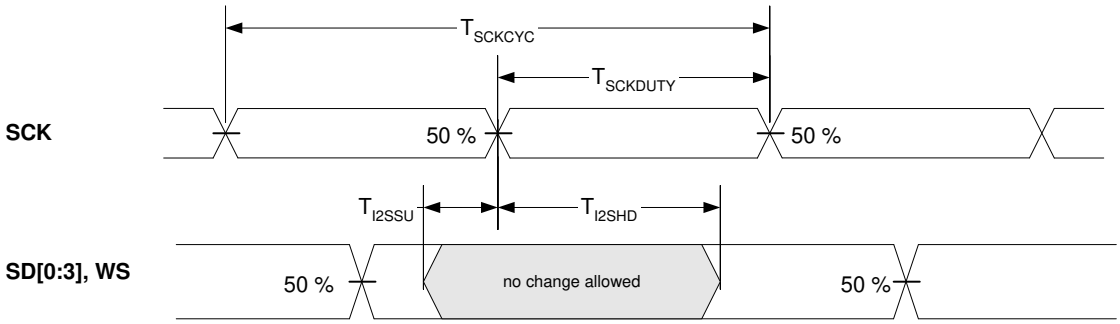


Figure 4.11. I²S Input Timings

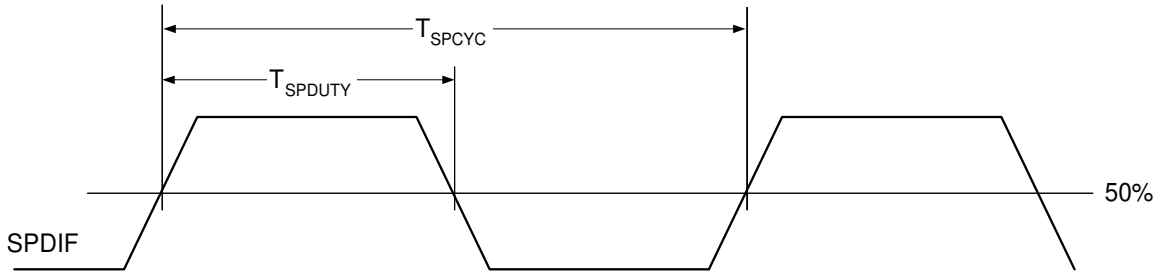


Figure 4.12. S/PDIF Input Timings

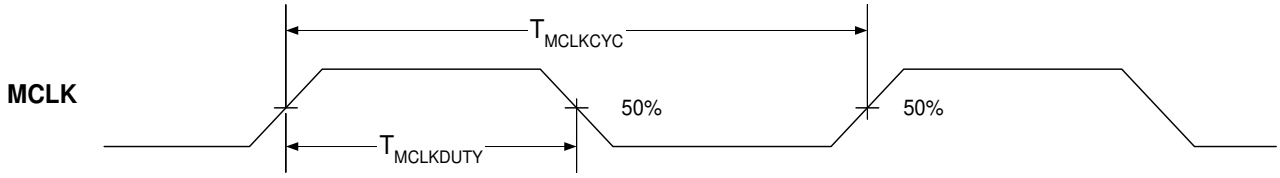


Figure 4.13. MCLK Timings

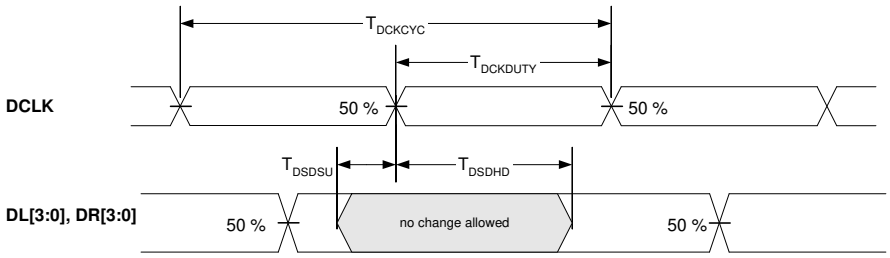


Figure 4.14. DSD Input Timings

4.4.5. I²C Timing Diagrams

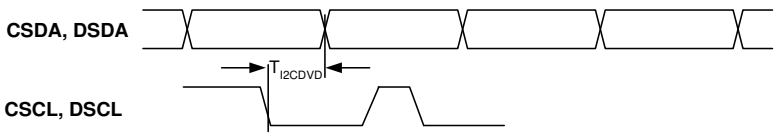


Figure 4.15. I²C Data Valid Delay (Driving Read Cycle Data)

5. Pin Diagram and Descriptions

5.1. Pin Diagram

Figure 5.1 shows the pin diagram for the SiI9136-3/SiI1136 transmitter. A description of the pin functions begins on the next page.

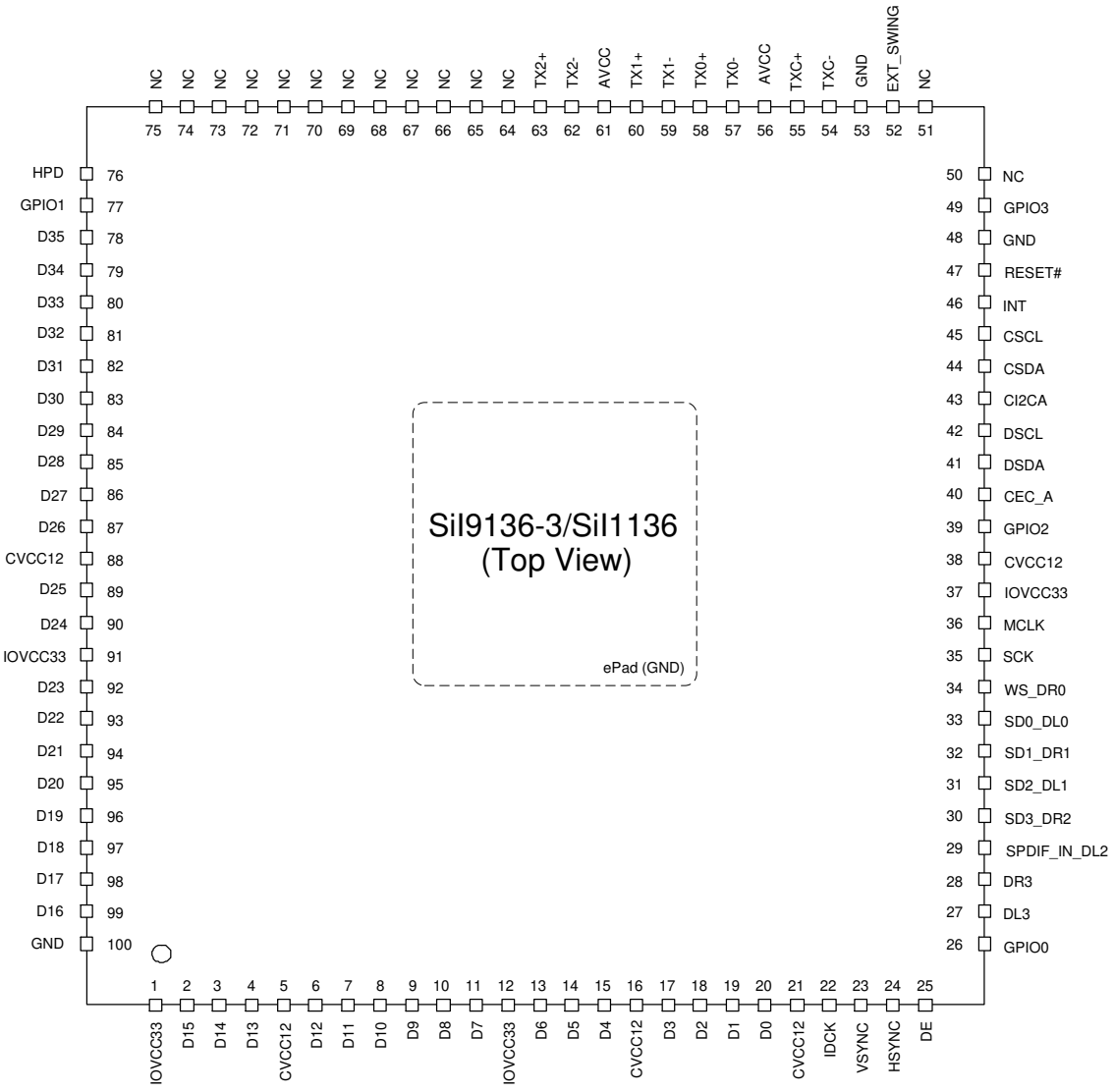


Figure 5.1. Pin Diagram

5.2. Pin Descriptions

5.2.1. Video Data Input

Name	Pin	Type	Dir	Description
D0	20	LVTTL 5 V tolerant	Input	Video Data Inputs. The video data inputs can be configured to support a wide variety of input formats, including multiple RGB and YCbCr bus formats, using the VID_CONFIG registers. See the Common Video Input Formats section on page 33 for details.
D1	19			
D2	18			
D3	17			
D4	15			
D5	14			
D6	13			
D7	11			
D8	10			
D9	9			
D10	8			
D11	7			
D12	6			
D13	4			
D14	3			
D15	2			
D16	99			
D17	98			
D18	97			
D19	96			
D20	95			
D21	94			
D22	93			
D23	92			
D24	90			
D25	89			
D26	87			
D27	86			
D28	85			
D29	84			
D30	83			
D31	82			
D32	81			
D33	80			
D34	79			
D35	78			
IDCK	22	LVTTL 5 V tolerant	Input	Input Data Clock. Input configurable using the VID_CONFIG registers.
DE	25	LVTTL 5 V tolerant	Input	Data Enable. This signal is HIGH when the transmitter input pixel data is valid and LOW otherwise. DE is optional for some input formats, such as ITU-R BT.656.
HSYNC	24	LVTTL 5 V tolerant	Input	Horizontal Sync input control signal. HSYNC is optional for some input formats, such as ITU-R BT.656.
VSYNC	23	LVTTL 5 V tolerant	Input	Vertical Sync input control signal. VSYNC is optional for some input formats, such as ITU-R BT.656.

5.2.2. TMDS Output

Name	Pin	Type	Dir	Description
TX0+	58	TMDS	Output	HDMI Transmitter Output Port Data. TMDS low voltage differential signal output data pairs.
TX0-	57			
TX1+	60			
TX1-	59			
TX2+	63			
TX2-	62			
TXC+	55	TMDS	Output	HDMI Transmitter Output Port Clock. TMDS low voltage differential signal output clock pair.
TXC-	54			
EXT_SWING	52	Analog	Input Output	External Swing Voltage Control. Recommended values (actual value depends on board design): • 5.6 kΩ resistor to ground without using internal termination. • 4.02 kΩ resistor to ground using internal termination.

5.2.3. Audio Input

Name	Pin	Type	Dir	Description	
				I²S Mode; S/PDIF Mode	DSD Mode
MCLK	36	LVTTL 5 V tolerant	Input	Audio Input Master Clock.	—
SCK	35	LVTTL 5 V tolerant	Input	I²S Serial Clock.	DSD Clock.
WS_DR0	34	LVTTL 5 V tolerant	Input	I²S Word Select.	DSD Data Right Bit 0.
SD0_DL0	33	LVTTL 5 V tolerant	Input	I²S Data 0.	DSD Data Left Bit 0.
SD1_DR1	32	LVTTL 5 V tolerant	Input	I²S Data 1.	DSD Data Right Bit 1.
SD2_DL1	31	LVTTL 5 V tolerant	Input	I²S Data 2.	DSD Data Left Bit 1.
SD3_DR2	30	LVTTL 5 V tolerant	Input	I²S Data 3.	DSD Data Right Bit 2.
SPDIF_IN_DL2	29	LVTTL 5 V tolerant	Input	S/PDIF Input.	DSD Data Left Bit 2.
DR3	28	LVTTL 5 V tolerant	Input	—	DSD Data Right Bit 3.
DL3	27	LVTTL 5 V tolerant	Input	—	DSD Data Left Bit 3.

5.2.4. DDC, CEC, Configuration, and Control

Name	Pin	Type	Dir	Description
INT	46	LVTTL	Output	Interrupt Output.
RESET#	47	Schmitt	Input	Reset signal. Active LOW asynchronous reset input for entire chip.
HPD	76	LVTTL	Input	Hot Plug Detect.
GPIO0	26	LVTTL	Input Output	General Purpose I/O Data 0.
GPIO1	77	LVTTL	Input Output	General Purpose I/O Data 1.
GPIO2	39	LVTTL	Input Output	General Purpose I/O Data 2.
GPIO3	49	LVTTL	Input Output	General Purpose I/O Data 3.
DSCL	42	Schmitt Open drain 5 V tolerant	Input Output	DDC I2C Clock. HDCP KSV, An, and Ri values are exchanged over this I2C port during authentication. True open drain, so does not pull to ground if power not applied.
DSDA	41	Schmitt Open drain 5 V tolerant	Input Output	DDC I2C Data. HDCP KSV, An, and Ri values are exchanged over this I2C port during authentication. True open drain, it does not pull to ground if power not applied.
CI2CA	43	LVTTL 5 V tolerant	Input	Selects base address group for CSCL/CSDA interface. See Table 6.3 on page 27.
CSCL	45	Schmitt 5 V tolerant	Input	Local Configuration/Status I2C Clock. Chip configuration/status registers are accessed through this I2C port.
CSDA	44	Schmitt Open drain 5 V tolerant	Input Output	Local Configuration/Status I2C Data. Chip configuration/status registers are accessed through this I2C port.
CEC_A	40	CEC Compliant 5 V tolerant	Input Output	HDMI compliant CEC I/O. As an input, this pin acts as a LVTTL Schmitt-triggered input and is 5 V tolerant. As an output, the pin acts as an NMOS driver with resistive pull-up. This pin has an internal pull-up resistor.

5.2.5. Power and Ground

Name	Pin	Type	Description	Supply
CVCC12	5, 16, 21, 38, 88	Power	Digital Core VCC.	1.2 V
IOVCC33	1, 12, 37, 91	Power	I/O VCC.	3.3 V
AVCC	56, 61	Power	Analog VCC.	1.2 V
GND	48, 53, 100	Ground	These pins must be connected to ground.	Ground

5.2.6. Not Connected and Reserved

Name	Pin	Type	Description	Supply
NC	50, 51, 64–75	Not connected	These pins should be left unconnected.	None

6. Feature Information

6.1. RGB to YCbCr Color Space Converter

The RGB→YCbCr color space converter can convert from video data RGB to standard definition or to high definition YCbCr formats. Table 6.1 shows the conversion formulas that are used. The HDMI AVI packet defines the color space of the incoming video.

Table 6.1. RGB to YCbCr Conversion Formulas

Video Format	Conversion	Formulas
		CE Mode 16-235 RGB
640 x 480	ITU-R BT.601	Y = 0.299R′ + 0.587G′ + 0.114B′ Cb = –0.172R′ – 0.339G′ + 0.511B′ + 128 Cr = 0.511R′ – 0.428G′ – 0.083B′ + 128
480i	ITU-R BT.601	
576i	ITU-R BT.601	
480p	ITU-R BT.601	
576p	ITU-R BT.601	
240p	ITU-R BT.601	
288p	ITU-R BT.601	
720p	ITU-R BT.709	Y = 0.213R′ + 0.715G′ + 0.072B′ Cb = –0.117R′ – 0.394G′ + 0.511B′ + 128 Cr = 0.511R′ – 0.464G′ – 0.047B′ + 128
1080i	ITU-R BT.709	
1080p	ITU-R BT.709	

6.2. YCbCr to RGB Color Space Converter

The YCbCr→RGB color space converter allows MPEG decoders to interface with RGB-only inputs. The CSC can convert from YCbCr in standard-definition (ITU.601) or high-definition (ITU.709) to RGB. See the detailed formulas in Table 6.2. Note the difference between RGB range for CE modes and PC modes.

Table 6.2. YCbCr-to-RGB Conversion Formula

Format change	Conversion	YCbCr Input Color Range[2, 3]
YCbCr 16-235 Input[2, 3, 4] to RGB 16-235 Output[2, 3, 4]	601[1]	R′ = Y + 1.371(Cr – 128) G′ = Y – 0.698(Cr – 128) – 0.336(Cb – 128) B′ = Y + 1.732(Cb – 128)
	709[1]	R′ = Y + 1.540(Cr – 128) G′ = Y – 0.459(Cr – 128) – 0.183(Cb – 128) B′ = Y + 1.816(Cb – 128)
YCbCr 16-235 Input[2, 3, 4] to RGB 0-255 Output[2, 3, 4]	601	R′ = 1.164((Y-16) + 1.371(Cr – 128)) G′ = 1.164((Y-16) – 0.698(Cr – 128) – 0.336(Cb – 128)) B′ = 1.164((Y-16) + 1.732(Cb – 128))
	709	R′ = 1.164((Y-16) + 1.540(Cr – 128)) G′ = 1.164((Y-16) – 0.459(Cr – 128) – 0.183(Cb – 128)) B′ = 1.164((Y-16) + 1.816(Cb – 128))

Notes:
1. No clipping can be done.
2. For 10-bit deep color, multiply all occurrences of the values 16, 128, 235, and 255 by 4.
3. For 12-bit deep color, multiply all occurrences of the values 16, 128, 235, and 255 by 16.
4. For 16-bit deep color, multiply all occurrences of the values 16, 128, 235, and 255 256.

6.3. I²C Register Information

I²C registers monitor and control all functions of the transmitter. The four local I²C slave addresses can be altered by setting the CI2CA signal LOW or HIGH as shown in Table 6.3. An external pull-up or pull-down resistor, depending on the desired set of I²C addresses, is used to set the level on the CI2CA pin. Refer to the Programmer Reference (see the Lattice Semiconductor Documents section on page 52) for complete information. *The Programmer's Reference requires an NDA with Lattice Semiconductor.*

Table 6.3. Control of the Default I²C Addresses with the CI2CA Pin

Block	CI2CA = 0	CI2CA = 1
Configuration Registers	0x7A	0x7E
TPI	0x72	0x76
CPI	0xC0	0xC4

6.4. I²S Audio Input

The I²S input has four I²S data signals to support up to eight channels of linear pulse code modulation (LPCM) audio. The I²S interface also supports high bit rate audio formats such as Dolby® TrueHD and DTS HD Master Audio. Two-channel PCM audio can be downsampled by a factor of 2 or 4 to support 32, 44.1, or 48 kHz basic sample rates as required by the HDMI standard.

6.5. Direct Stream Digital Input

Nine pins are used for the Direct Stream Digital interface that provides 8-channel one-bit audio data (DSD). This interface is for SACD applications. Seven of the nine pins of this interface (four data left, four data right, and one clock) share the I²S and S/PDIF pins.

The one-bit audio inputs are sampled on the positive edge of the DSD clock, assembled into 56-bit packets, and mapped to the appropriate FIFO. The Audio InfoFrame, instead of the Channel Status bits, carries the sampling information for one-bit audio. The one-bit audio interface supports an input clock frequency of 2.882 MHz (64 • 44.1 kHz).

6.6. S/PDIF Input

The Sony/Philips Digital Interface Format (S/PDIF) interface is usually associated with compressed audio formats such as Dolby® Digital (AC-3), DTS, and the more advanced variants of these formats.

6.7. I²S and S/PDIF Supported MCLK Frequencies

The transmitter includes an integrated MCLK generator for operation without an external clock PLL, although an external MCLK can be used. The I²S and S/PDIF interfaces support sampling frequencies of 32, 44.1, 48, 64, 88.2, 96, 128, 176.4, and 192 kHz. The 64 and 128 kHz sampling rates, however, are not part of the HDMI standard; and must be downsampled to 32 kHz before transmitting across the HDMI link. Table 6.4 lists the supported MCLK frequencies.

Table 6.4. Supported MCLK Frequencies

Multiple of Fs	Audio Sample Rate, Fs						
	I²S and S/PDIF Supported Rates						
	32 kHz	44.1 kHz	48 kHz	88.2 kHz	96 kHz	176.4 kHz	192 kHz
128	4.096 MHz	5.645 MHz	6.144 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz
192	6.144 MHz	8.467 MHz	9.216 MHz	16.934 MHz	18.432 MHz	33.868 MHz	36.864 MHz
256	8.192 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz
384	12.288 MHz	16.934 MHz	18.432 MHz	33.864 MHz	36.864 MHz	67.737 MHz	73.728 MHz
512	16.384 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz		
768	24.576 MHz	33.869 MHz	36.864 MHz	67.738 MHz	73.728 MHz		
1024	32.768 MHz	45.158 MHz	49.152 MHz				
1152	36.864 MHz	50.803 MHz	55.296 MHz				

6.8. Audio Downsampler Limitations

The SiI9136-3/SiI1136 transmitter has an audio downsampler function that downsamples the incoming two-channel audio data and sends the result over the HDMI link. The audio data can be downsampled by one-half or one-fourth with register control. Supported conversions are: from 192 kHz to 48 kHz, 176.4 kHz to 44.1 kHz, 96 kHz to 48 kHz, and 88.2 kHz to 44.1 kHz. Some limitations in the audio sample word length when using this feature may need special consideration in a real application.

When enabling the audio downsampler, the Channel Status registers for the audio sample word lengths sent over the HDMI link always indicate the maximum possible length. For example, if the input S/PDIF stream was in 20-bit mode with 16 bits valid, after enabling the downsampler the Channel Status indicates 20-bit mode with 20 bits valid.

Audio sample word length is carried in bits 33 through 35 of the Channel Status register over the HDMI link, as shown in Table 6.5. These bits are always set to 0b101 when enabling the downsampler feature. Audio data is not affected because 0s are placed into the LSBs of the data, and the wider word length is sent across the HDMI link.

Table 6.5. Channel Status Bits Used for Word Length

Bit				Sample Word Length (bits)	Note
Audio Sample Word Length			Maximum Word Length[1]		
35	34	33	32		
0	0	0	0	Not indicated	
0	0	1	0	16	2
0	1	0	0	18	2
1	0	0	0	19	2
1	0	1	0	20	2, 4
1	1	0	0	17	2
0	0	0	1	Not indicated	3
0	0	1	1	20	3
0	1	0	1	22	3
1	0	0	1	23	3
1	0	1	1	24	3, 4
1	1	0	1	21	3

Notes:

1. Maximum audio sample word length (MAXLEN) is 20 bits if MAXLEN = 0 and 24 bits if MAXLEN = 1.
2. Maximum audio sample word length is 20.
3. Maximum audio sample word length is 24.
4. Bits [35:33] are always 0b101 when the downsampler is enabled

6.9. High Bitrate Audio on HDMI

The high bitrate compression standards such as Dolby TrueHD and DTS-HD transmit data at bit rates as high as 18 or 24 Mb/s. Because these bit rates are so high, DVD decoders and HDMI transmitters operating as source devices, and DSP and HDMI receivers as sink devices, must carry the data using four I^2S lines rather than a single very-high-speed S/PDIF interface or I^2S bus. See Figure 6.1.

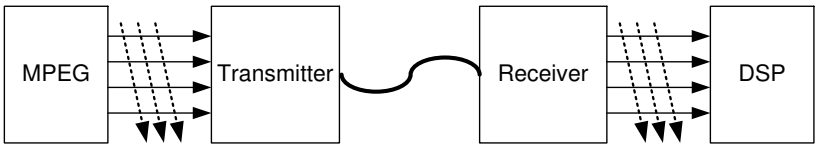


Figure 6.1. High Speed Data Transmission

The High Bitrate audio stream is originally encoded as a single stream. To send the stream over four I^2S lines, the DVD decoder splits it into four streams. Figure 6.2 shows the High Bitrate stream before it has been split into four I^2S lines, and Figure 6.3 shows the same audio stream after being split. Each sample requires 16 cycles of the I^2S clock (SCK).

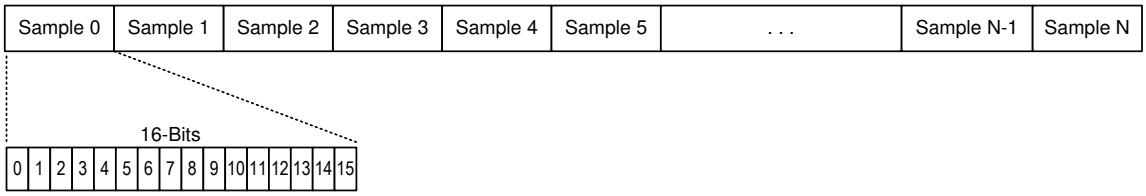


Figure 6.2. High Bitrate Stream Before and After Reassembly and Splitting

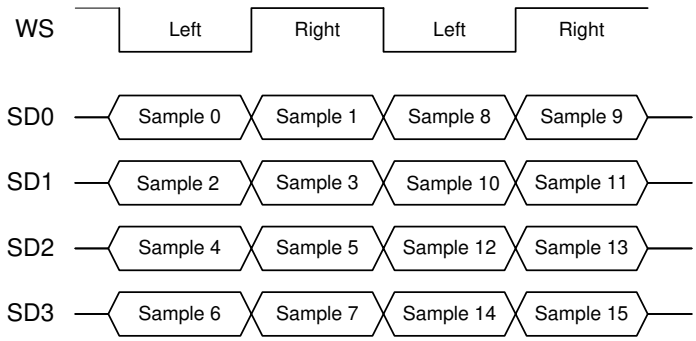


Figure 6.3. High Bitrate Stream After Splitting

6.10. Power Domains

To reduce standby power, the SiI9136-3/SiI1136 transmitter supports three power modes. Each mode complies with the ACPI Specification.

- **Power-On mode (D0):** The System is powered up and running completely. All functions are available.
- **Power-Standby mode (D2):** Some sub-systems are enabled, but the audio and video processing pipelines are disabled. The configuration interface, CEC, GPIO, and DDC master are active. The TMDS core is configured independently. The Host is able to perform the following functions during this mode:
  - CEC: send and receive messages
  - DDC: read EDID from HDMI receiver
  - optional: TMDS core enabled for generating receiver-sense interrupt requests
- **Power-Off mode (D3):** The chip is in its lowest power-state. All clocks are disabled. No register access is possible. The only active function is the interrupt request generation for Hot-plug events, if that function has been configured before entering this mode. An IRQ is asserted in this mode, but cannot be deasserted, as register access is not possible. The host must assert RESET# to the chip to properly leave Power-Off mode.

6.11. Internal DDC Master

Figure 6.4 illustrates how the transmitter contains a master I²C port for direct connection to the HDMI cable. A pass-through mechanism allows direct control of the DDC lines by the host I²C controller.

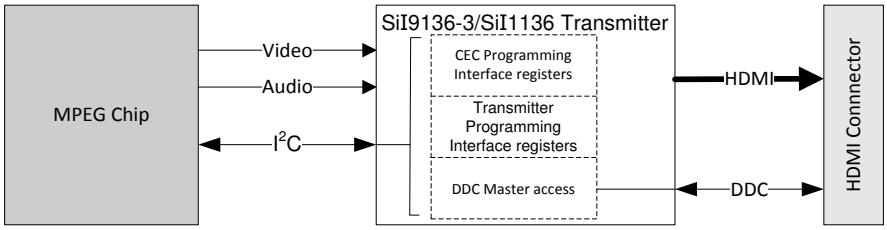
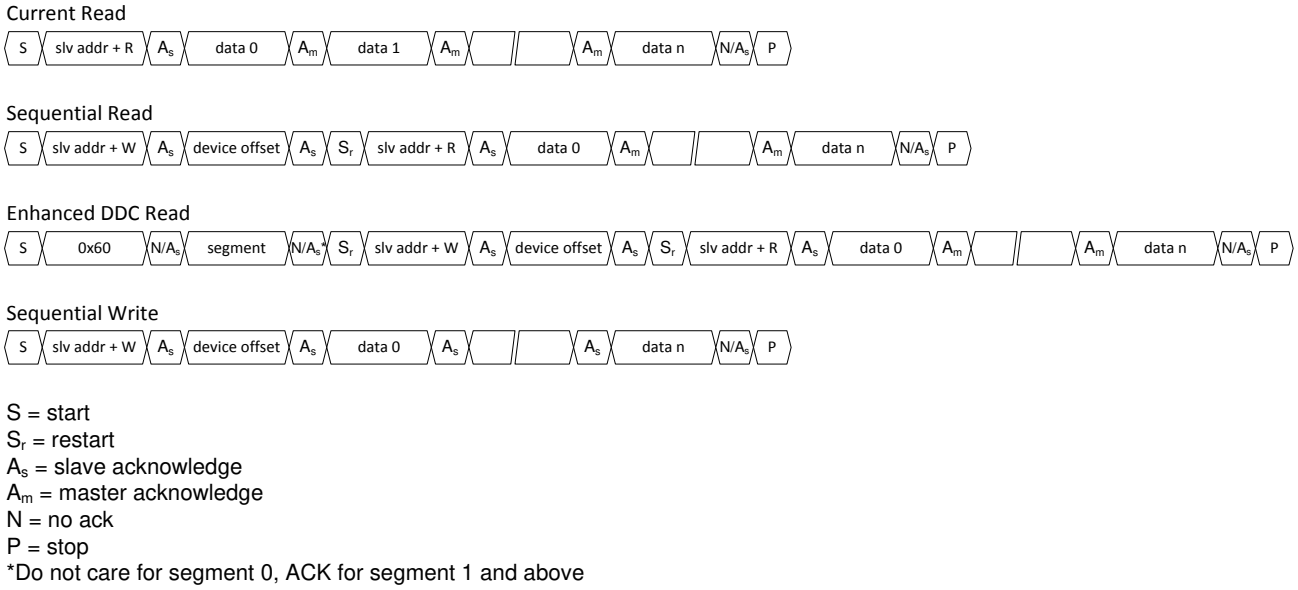


Figure 6.4. Simplified Host I²C Interface Using Master DDC Port

The DDC Master Interface supports the I²C transactions specified by the VESA Enhanced Display Data Channel Standard. The DDC master block complies with the 100 kHz Standard Mode timing of the I²C Specification and supports slave clock stretching, as required by E-DDC. Figure 6.5 shows the supported transactions and timing sequences.



S = start
S_r = restart
A_s = slave acknowledge
A_m = master acknowledge
N = no ack
P = stop
*Do not care for segment 0, ACK for segment 1 and above

Figure 6.5. Master I²C Supported Transactions

6.12. Deep Color Support

The SiI9136-3/SiI1136 transmitter provides support for Deep Color video data up to the maximum specified link speed of 2.25 Gb/s, at a 225 MHz internal clock rate for the Deep Color packetized data. It supports 30-bit, 36-bit, and 48-bit video input formats, and converts the data to 8-bit packets for encryption and encoding for transferring across the TMDS link.

When the input data width is wider than desired, the device can be programmed to dither or truncate the video data to the desired size. For instance, if the input data width is 12 bits per pixel component, but the sink device only supports 10 bits, the transmitter can be programmed either to dither or to truncate the 12-bit input data to the desired 10-bit output data. Dither processing is the final block in the video processing path and occurs after all other video processing has been performed; refer to the Video Data Input and Conversion section on page 9. Note that the actual maximum link speed for 3D FP or 4K formats is 300 MHz. However, Deep Color is only supported up to 1080p60. Thus, for Deep Color the maximum link speed is 225 MHz.

6.13. Source Termination

TMDS transmitters use a current source to develop the low-voltage differential signal at the receiver end of the DC-coupled TMDS transmission line, which constitutes open termination for reflected waveforms. Thus, signal reflections created by traces, packaging, connectors, and the cable can arrive at the transmitter with increased amplitude.

To reduce these reflections, the transmitter chip has an internal termination option of 150 Ω for single-ended termination and 300 Ω for differential termination. This termination reduces the amplitude of the reflected signal, but it also lowers the common-mode input voltage at the sink. As a result, Lattice Semiconductor recommends turning internal source termination off when the transmitter operates at less than or equal to 165 MHz and turning it on for frequencies above 165 MHz Using internal source termination at the higher frequencies while still maintaining conformance to the HDMI Specification is possible because the sink input voltage range tolerance is wider above 165 MHz.

6.14. 3D and 4K Video Formats

The SiI9136-3/SiI1136 transmitter supports the 3D and 4K video modes described in the HDMI Specification. All modes support RGB 4:4:4, YCbCr 4:2:2, and YCbCr 4:4:4 color formats, and 8-, 10-, and 12-bit data width per color component. External separate HSYNC, VSYNC, and DE signals can be supplied, or these signals can be supplied as embedded EAV/SAV sequences in the video stream. Table 6.6 shows only the maximum possible resolution with a given frame rate. For example, Side-by-Side mode is defined for 1080p60, which implies that 720p60 and 480p60 are also supported. Furthermore, a frame rate of 24 Hz also means that a frame rate of 23.98 Hz is supported, and a frame rate of 60 Hz also means that a frame rate of 59.94 Hz is supported. Input pixel clock changes accordingly.

When using Side-by-Side format, 4:4:4 to 4:2:2 downsampling and 4:2:2 dithering and upsampling to 4:4:4 should be avoided because these combinations may result in visible artifacts. Dithering should also be avoided when using frame packing formats. Video processing should be bypassed in the case of L + depth format. The SiI9136-3/SiI1136 device supports transmission of the Vendor Specific InfoFrame (VSIF), which carries 3D and 4K information to the receiver.

Table 6.6. Supported 3D and 4K Video Formats

3D Format	Extended Definition	Resolution	Frame Rate (Hz)	Input Pixel Clock (MHz)
Frame Packing	progressive	1080p	50/60	297.00
		1080p	24	148.5
		720p	50/60	
	interlaced	1080i	50/60	
L + depth	progressive	1080p	50/60	297.00
Side-by-Side	full	1080p	50/60	297.00
	half	1080p	50/60	
		1080i	50/60	74.25
Top and Bottom	progressive	1080p	50/60	148.5
	interlaced	1080i	50/60	74.25
	progressive	720p	50/60	

4K Format	Extended Definition	Resolution	Frame Rate (Hz)	Input Pixel Clock (MHz)
4K	—	3840 x 2160	29.97/30	296.703/297.000
			25	297.000
			23.98/24	296.703/297.000
	SMPTE	4096 x 2160	24	297.000

6.15. Control Signal Connections

Figure 6.6 shows the interconnection between the host processor and transmitter. The INT output can be connected as an interrupt to the processor, or the processor can poll a register to determine if any of the enabled interrupts have occurred.

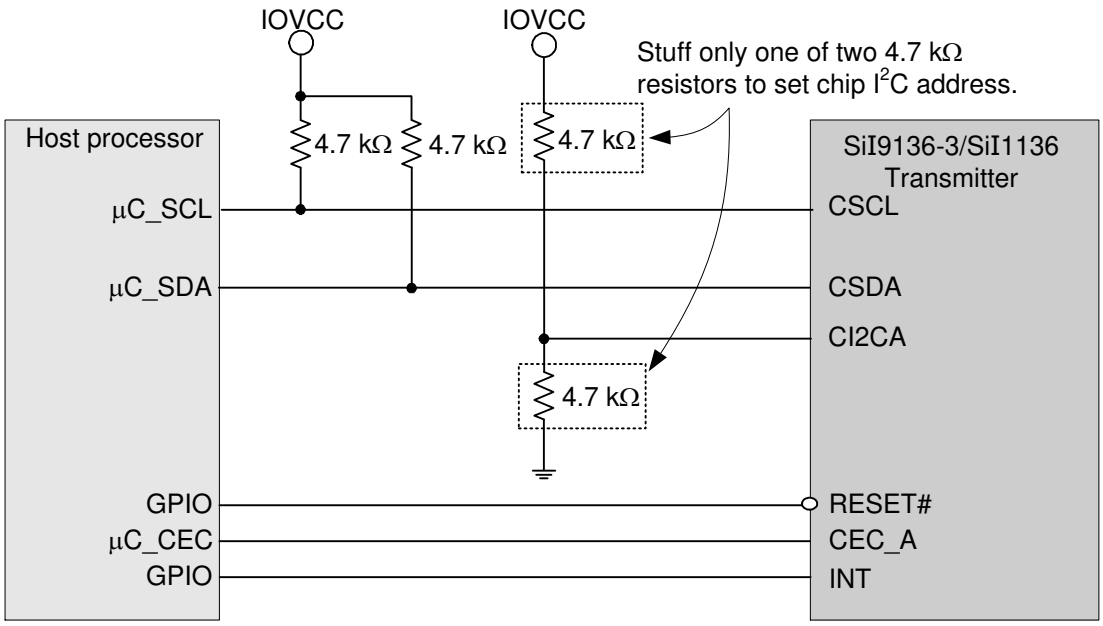


Figure 6.6. Controller Connections Schematic

6.16. Input Data Bus Mapping

6.16.1. Common Video Input Formats

The video data capture block receives uncompressed 8- to 16-bit color depth, or bits per color component, digital video from the digital video input interface and provides a data path width of 8 to 36 bits. The data path is divided internally into three 16-bit data channels, which are configured for one of the video formats listed in Table 6.7.

Table 6.7. Video Input Formats

Color Space	Video Format	Clock Edge Mode	Bus Width/ Color Depth	SYNC[6]	Input Pixel Clock (MHz)									Notes	Page
					480i[2, 3]	VGA 480p[2]	XGA	720p	1080i	SXGA	1080p	UXGA	4K		
RGB	4:4:4	Single	36/12	Sep	27	25/27	65	74.25	74.25	108	148.5	—	—	1	30
		Single	30/10	Sep	27	25/27	65	74.25	74.25	108	148.5	162	—	1	30
		Single	24/8	Sep	27	25/27	65	74.25	74.25	108	148.5	162	297	1, 7	30
		Dual	12/8	Sep	27	25/27	65	74.25	74.25	—	—	—	—	4	44
		Dual	15/10	Sep	27	25/27	65	74.25	74.25	—	—	—	—	4	44
		Dual	18/12	Sep	27	25/27	65	74.25	74.25	—	—	—	—	4	44
		Dual	24/16	Sep	27	25/27	65	74.25	74.25	—	—	—	—	4	44
YCbCr xvYCC	4:4:4	Single	36/12	Sep	27	25/27	65	74.25	74.25	108	148.5	—	—	1	30
		Single	30/10	Sep	27	25/27	65	74.25	74.25	108	148.5	162	—	1	30
		Single	24/8	Sep	27	25/27	65	74.25	74.25	108	148.5	162	297	1, 7	30
		Dual	12/8	Sep	27	25/27	65	74.25	74.25	—	—	—	—	4	44
		Dual	15/10	Sep	27	25/27	65	74.25	74.25	—	—	—	—	4	44
		Dual	18/12	Sep	27	25/27	65	74.25	74.25	—	—	—	—	4	44
		Dual	24/16	Sep	27	25/27	65	74.25	74.25	—	—	—	—	4	44
	4:2:2	Single	16/8 20/10 24/12	Sep	27	25/27	65	74.25	74.25	108	148.5	162	297	1, 7	36
				Emb	27	25/27	65	74.25	74.25	108	148.5	162	297	1, 4, 7	38
		Single/ YC Mux	8/8 10/10 12/12	Sep	27	50/54	130	148.5	148.5	—	—	—	—	1	40
				Emb	27	50/54	130	148.5	148.5	—	—	—	—	1, 4	42
				T1004	—	50/54	130	—	—	—	—	—	—	1, 4, 5	—

Notes:

1. Latching edge is programmable.
2. 480i/p support also encompasses 576i/p support.
3. 480i must be provided at 27 MHz, using pixel replication, to be transmitted across the HDMI link.
4. If embedded syncs are provided, DE is generated internally from SAV/EAV sequences. Embedded syncs use ITU-R BT.656 SAV/EAV sequences of FF, 00, 00, XY.
5. BTA-T1004 format is defined for a single-channel (8/10/12-bit) bus.
6. Sep = separate sync; Emb = embedded sync; T1004 = BTA-T1004 encoded sync.
7. 4K resolution only supports capturing data at the falling edge of IDCK.

The system configures registers that set the bus width, video format, and rising or falling edge latching, according to the format of the video data received by the transmitter. The logic also supports dual-edge clocking.

Relevant format information must also be programmed into registers to be formed into AVI InfoFrame packets for passing over the HDMI link.

In the tables which follow in this section, shaded cells labeled LOW should be held LOW when not used for a selected video format. When not used, they should be tied to ground.

In the timing diagrams which follow in this chapter, data bits labeled *val* do not convey pixel information and contain values defined by the relevant specification. In the diagrams showing embedded sync, the SAV and EAV sequence FF, 00, 00, XY is specified by ITU-R BT.656.

6.16.2. RGB and YCbCr 4:4:4 Separate Sync

The pixel clock runs at the pixel rate and a complete definition of each pixel is received on each clock cycle. Each column in Table 6.8 shows the first pixel of n + 1 pixels in the line of video. The figures below the table show RGB and YCbCr data; the YCbCr 4:4:4 data is given in braces {}.

Table 6.8. RGB/YCbCr 4:4:4 Separate Sync Data Mapping

Pin Name	24-bit Data Bus 8-bit Color Depth		30-bit Data Bus 10-bit Color Depth		36-bit Data Bus 12-bit Color Depth	
	RGB	YCbCr	RGB	YCbCr	RGB	YCbCr
D0	LOW	LOW	LOW	LOW	B0[0]	Cb0[0]
D1	LOW	LOW	LOW	LOW	B0[1]	Cb0[1]
D2	LOW	LOW	B0[0]	Cb0[0]	B0[2]	Cb0[2]
D3	LOW	LOW	B0[1]	Cb0[1]	B0[3]	Cb0[3]
D4	B0[0]	Cb0[0]	B0[2]	Cb0[2]	B0[4]	Cb0[4]
D5	B0[1]	Cb0[1]	B0[3]	Cb0[3]	B0[5]	Cb0[5]
D6	B0[2]	Cb0[2]	B0[4]	Cb0[4]	B0[6]	Cb0[6]
D7	B0[3]	Cb0[3]	B0[5]	Cb0[5]	B0[7]	Cb0[7]
D8	B0[4]	Cb0[4]	B0[6]	Cb0[6]	B0[8]	Cb0[8]
D9	B0[5]	Cb0[5]	B0[7]	Cb0[7]	B0[9]	Cb0[9]
D10	B0[6]	Cb0[6]	B0[8]	Cb0[8]	B0[10]	Cb0[10]
D11	B0[7]	Cb0[7]	B0[9]	Cb0[9]	B0[11]	Cb0[11]
D12	LOW	LOW	LOW	LOW	G0[0]	Y0[0]
D13	LOW	LOW	LOW	LOW	G0[1]	Y0[1]
D14	LOW	LOW	G0[0]	Y0[0]	G0[2]	Y0[2]
D15	LOW	LOW	G0[1]	Y0[1]	G0[3]	Y0[3]
D16	G0[0]	Y0[0]	G0[2]	Y0[2]	G0[4]	Y0[4]
D17	G0[1]	Y0[1]	G0[3]	Y0[3]	G0[5]	Y0[5]
D18	G0[2]	Y0[2]	G0[4]	Y0[4]	G0[6]	Y0[6]
D19	G0[3]	Y0[3]	G0[5]	Y0[5]	G0[7]	Y0[7]
D20	G0[4]	Y0[4]	G0[6]	Y0[6]	G0[8]	Y0[8]
D21	G0[5]	Y0[5]	G0[7]	Y0[7]	G0[9]	Y0[9]
D22	G0[6]	Y0[6]	G0[8]	Y0[8]	G0[10]	Y0[10]
D23	G0[7]	Y0[7]	G0[9]	Y0[9]	G0[11]	Y0[11]
D24	LOW	LOW	LOW	LOW	R0[0]	Cr0[0]
D25	LOW	LOW	LOW	LOW	R0[1]	Cr0[1]
D26	LOW	LOW	R0[0]	Cr0[0]	R0[2]	Cr0[2]
D27	LOW	LOW	R0[1]	Cr0[1]	R0[3]	Cr0[3]
D28	R0[0]	Cr0[0]	R0[2]	Cr0[2]	R0[4]	Cr0[4]
D29	R0[1]	Cr0[1]	R0[3]	Cr0[3]	R0[5]	Cr0[5]
D30	R0[2]	Cr0[2]	R0[4]	Cr0[4]	R0[6]	Cr0[6]
D31	R0[3]	Cr0[3]	R0[5]	Cr0[5]	R0[7]	Cr0[7]
D32	R0[4]	Cr0[4]	R0[6]	Cr0[6]	R0[8]	Cr0[8]
D33	R0[5]	Cr0[5]	R0[7]	Cr0[7]	R0[9]	Cr0[9]
D34	R0[6]	Cr0[6]	R0[8]	Cr0[8]	R0[10]	Cr0[10]
D35	R0[7]	Cr0[7]	R0[9]	Cr0[9]	R0[11]	Cr0[11]
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

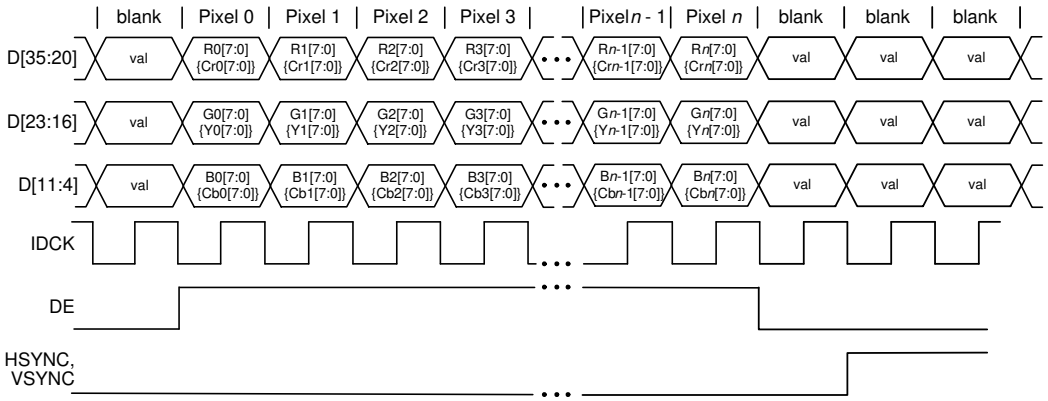


Figure 6.7. 8-Bit Color Depth RGB/YCbCr/xvYCC 4:4:4 Timing

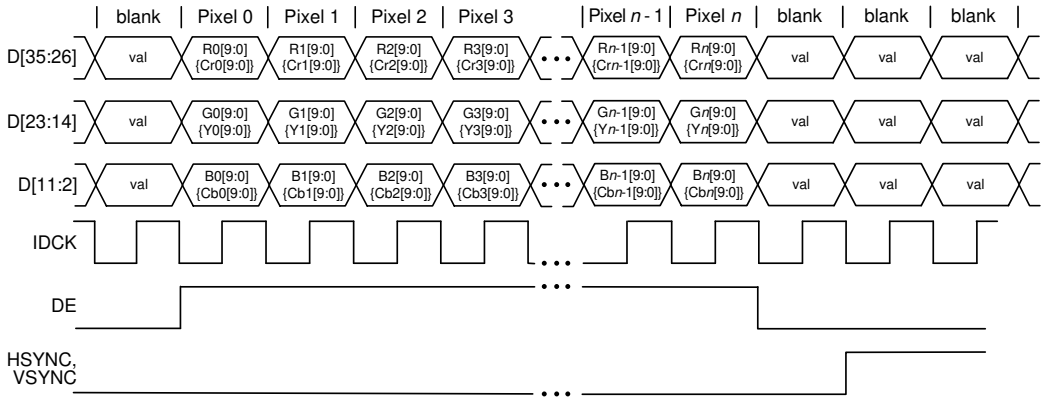


Figure 6.8. 10-Bit Color Depth RGB/YCbCr/xvYCC 4:4:4 Timing

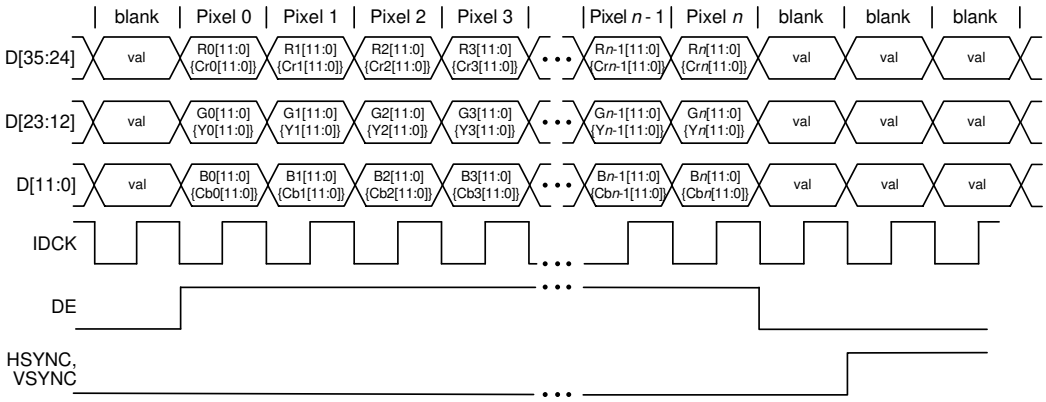


Figure 6.9. 12-Bit Color Depth RGB/YCbCr/xvYCC 4:4:4 Timing

6.16.3. YC 4:2:2 Separate Sync Formats

The YC 4:2:2 formats receive one pixel for every pixel clock period. A luma (Y) value is carried for every pixel, but the chroma values (Cb and Cr) change only every second pixel. The data bus can be 16, 20, or 24 bits. HSYNC and VSYNC are driven explicitly on their own signals. Each pair of columns in Table 6.9 shows the first and second pixel of n + 1 pixels in the line of video. The DE HIGH time must contain an even number of pixel clocks.

Table 6.9. YC 4:2:2 Separate Sync Data Mapping

Pin Name	16-bit Data Bus 8-bit Color Depth		20-bit Data Bus 10-bit Color Depth		24-bit Data Bus 12-bit Color Depth	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
D[3:0]	LOW	LOW	LOW	LOW	LOW	LOW
D4	LOW	LOW	LOW	LOW	Y0[0]	Y1[0]
D5	LOW	LOW	LOW	LOW	Y0[1]	Y1[1]
D6	LOW	LOW	Y0[0]	Y1[0]	Y0[2]	Y1[2]
D7	LOW	LOW	Y0[1]	Y1[1]	Y0[3]	Y1[3]
D8	LOW	LOW	LOW	LOW	Cb0[0]	Cr0[0]
D9	LOW	LOW	LOW	LOW	Cb0[1]	Cr0[1]
D10	LOW	LOW	Cb0[0]	Cr0[0]	Cb0[2]	Cr0[2]
D11	LOW	LOW	Cb0[1]	Cr0[1]	Cb0[3]	Cr0[3]
D[15:12]	LOW	LOW	LOW	LOW	LOW	LOW
D16	Y0[0]	Y1[0]	Y0[2]	Y1[2]	Y0[4]	Y1[4]
D17	Y0[1]	Y1[1]	Y0[3]	Y1[3]	Y0[5]	Y1[5]
D18	Y0[2]	Y1[2]	Y0[4]	Y1[4]	Y0[6]	Y1[6]
D19	Y0[3]	Y1[3]	Y0[5]	Y1[5]	Y0[7]	Y1[7]
D20	Y0[4]	Y1[4]	Y0[6]	Y1[6]	Y0[8]	Y1[8]
D21	Y0[5]	Y1[5]	Y0[7]	Y1[7]	Y0[9]	Y1[9]
D22	Y0[6]	Y1[6]	Y0[8]	Y1[8]	Y0[10]	Y1[10]
D23	Y0[7]	Y1[7]	Y0[9]	Y1[9]	Y0[11]	Y1[11]
D[27:24]	LOW	LOW	LOW	LOW	LOW	LOW
D28	Cb0[0]	Cr0[0]	Cb0[2]	Cr0[2]	Cb0[4]	Cr0[4]
D29	Cb0[1]	Cr0[1]	Cb0[3]	Cr0[3]	Cb0[5]	Cr0[5]
D30	Cb0[2]	Cr0[2]	Cb0[4]	Cr0[4]	Cb0[6]	Cr0[6]
D31	Cb0[3]	Cr0[3]	Cb0[5]	Cr0[5]	Cb0[7]	Cr0[7]
D32	Cb0[4]	Cr0[4]	Cb0[6]	Cr0[6]	Cb0[8]	Cr0[8]
D33	Cb0[5]	Cr0[5]	Cb0[7]	Cr0[7]	Cb0[9]	Cr0[9]
D34	Cb0[6]	Cr0[6]	Cb0[8]	Cr0[8]	Cb0[10]	Cr0[10]
D35	Cb0[7]	Cr0[7]	Cb0[9]	Cr0[9]	Cb0[11]	Cr0[11]
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

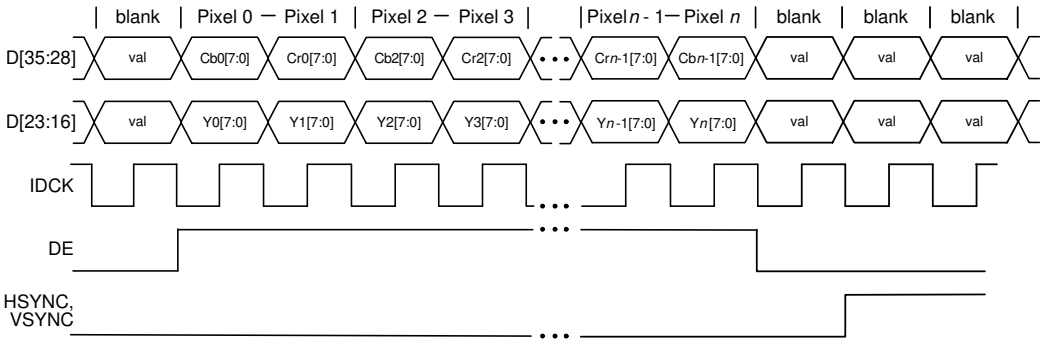


Figure 6.10. 8-Bit Color Depth YC 4:2:2 Timing

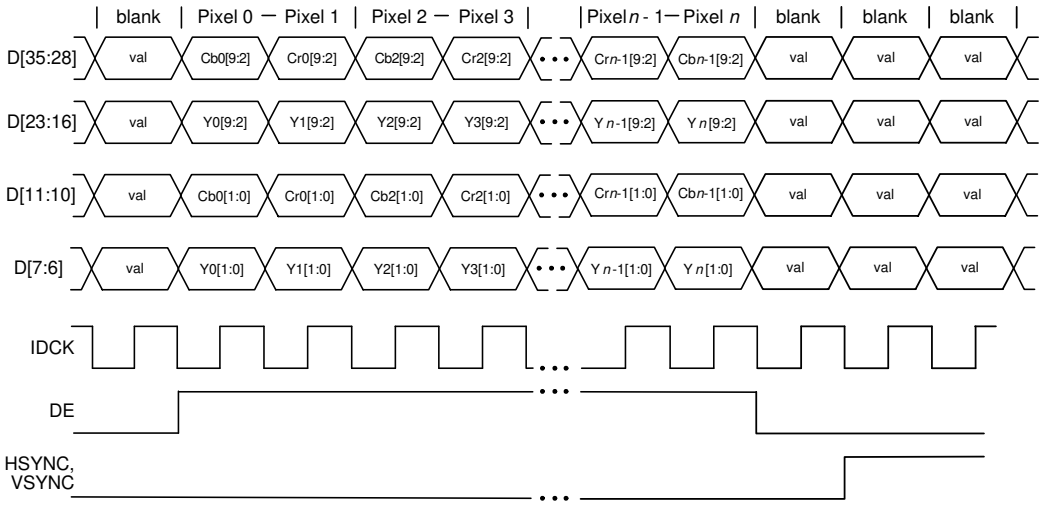


Figure 6.11. 10-Bit Color Depth YC 4:2:2 Timing

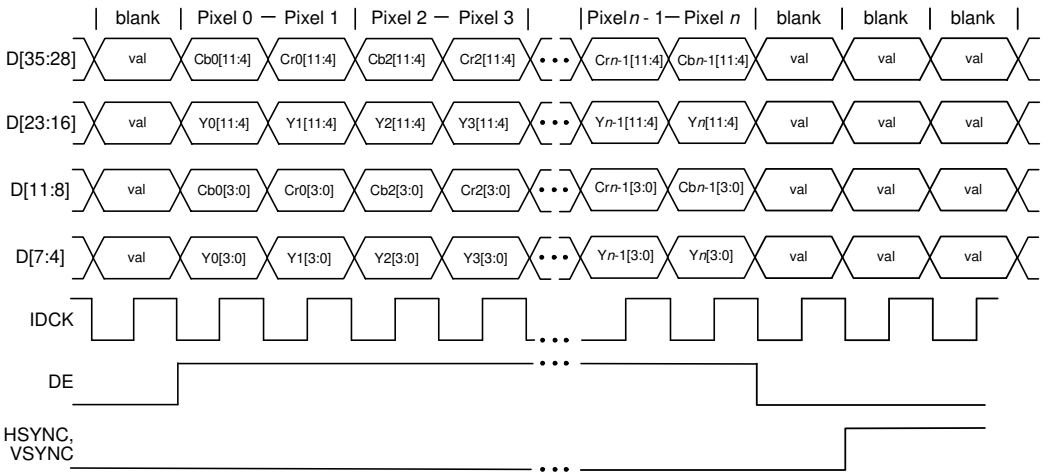


Figure 6.12. 12-Bit Color Depth YC 4:2:2 Timing

6.16.4. YC 4:2:2 Embedded Syncs Formats

The Embedded Sync format is identical to the YC 4:2:2 formats with Separate Syncs, except that the syncs are embedded and not explicit. The data bus can be 16, 20, or 24 bits. Each pair of columns in Table 6.10 shows the first and second pixel of n + 1 pixels in the line of video.

Table 6.10. YC 4:2:2 Embedded Sync Data Mapping

Pin Name	16-bit Data Bus 8-bit Color Depth		20-bit Data Bus 10-bit Color Depth		24-bit Data Bus 12-bit Color Depth	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
D[3:0]	LOW	LOW	LOW	LOW	LOW	LOW
D4	LOW	LOW	LOW	LOW	Y0[0]	Y1[0]
D5	LOW	LOW	LOW	LOW	Y0[1]	Y1[1]
D6	LOW	LOW	Y0[0]	Y1[0]	Y0[2]	Y1[2]
D7	LOW	LOW	Y0[1]	Y1[1]	Y0[3]	Y1[3]
D8	LOW	LOW	LOW	LOW	Cb0[0]	Cr0[0]
D9	LOW	LOW	LOW	LOW	Cb0[1]	Cr0[1]
D10	LOW	LOW	Cb0[0]	Cr0[0]	Cb0[2]	Cr0[2]
D11	LOW	LOW	Cb0[1]	Cr0[1]	Cb0[3]	Cr0[3]
D[15:12]	LOW	LOW	LOW	LOW	LOW	LOW
D16	Y0[0]	Y1[0]	Y0[2]	Y1[2]	Y0[4]	Y1[4]
D17	Y0[1]	Y1[1]	Y0[3]	Y1[3]	Y0[5]	Y1[5]
D18	Y0[2]	Y1[2]	Y0[4]	Y1[4]	Y0[6]	Y1[6]
D19	Y0[3]	Y1[3]	Y0[5]	Y1[5]	Y0[7]	Y1[7]
D20	Y0[4]	Y1[4]	Y0[6]	Y1[6]	Y0[8]	Y1[8]
D21	Y0[5]	Y1[5]	Y0[7]	Y1[7]	Y0[9]	Y1[9]
D22	Y0[6]	Y1[6]	Y0[8]	Y1[8]	Y0[10]	Y1[10]
D23	Y0[7]	Y1[7]	Y0[9]	Y1[9]	Y0[11]	Y1[11]
D[27:24]	LOW	LOW	LOW	LOW	LOW	LOW
D28	Cb0[0]	Cr0[0]	Cb0[2]	Cr0[2]	Cb0[4]	Cr0[4]
D29	Cb0[1]	Cr0[1]	Cb0[3]	Cr0[3]	Cb0[5]	Cr0[5]
D30	Cb0[2]	Cr0[2]	Cb0[4]	Cr0[4]	Cb0[6]	Cr0[6]
D31	Cb0[3]	Cr0[3]	Cb0[5]	Cr0[5]	Cb0[7]	Cr0[7]
D32	Cb0[4]	Cr0[4]	Cb0[6]	Cr0[6]	Cb0[8]	Cr0[8]
D33	Cb0[5]	Cr0[5]	Cb0[7]	Cr0[7]	Cb0[9]	Cr0[9]
D34	Cb0[6]	Cr0[6]	Cb0[8]	Cr0[8]	Cb0[10]	Cr0[10]
D35	Cb0[7]	Cr0[7]	Cb0[9]	Cr0[9]	Cb0[11]	Cr0[11]
HSYNC	LOW	LOW	LOW	LOW	LOW	LOW
VSYNC	LOW	LOW	LOW	LOW	LOW	LOW
DE	LOW	LOW	LOW	LOW	LOW	LOW

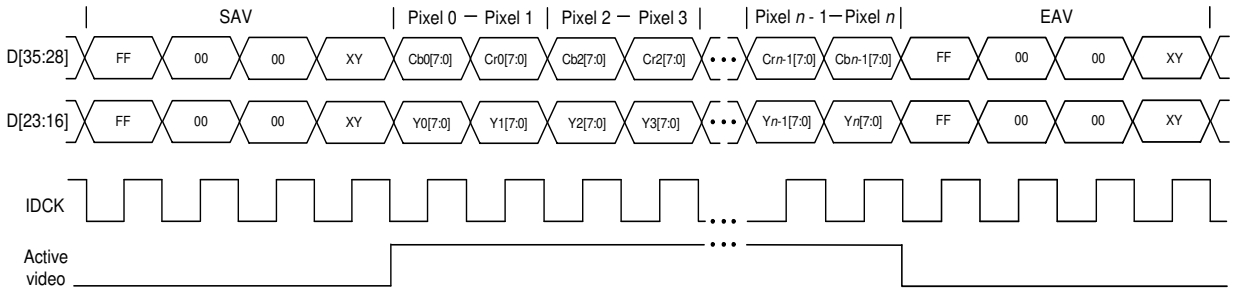


Figure 6.13. 8-Bit Color Depth YC 4:2:2 Embedded Sync Timing

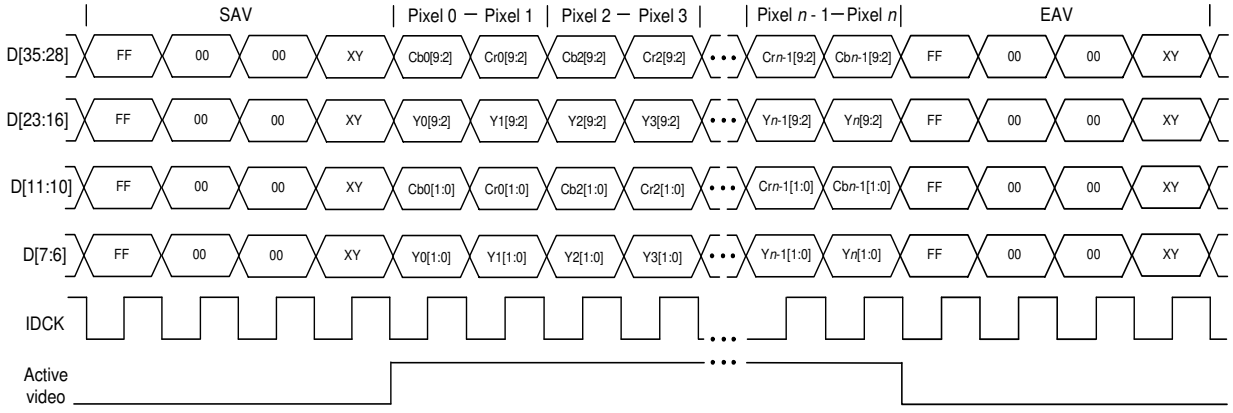


Figure 6.14. 10-Bit Color Depth YC 4:2:2 Embedded Sync Timing

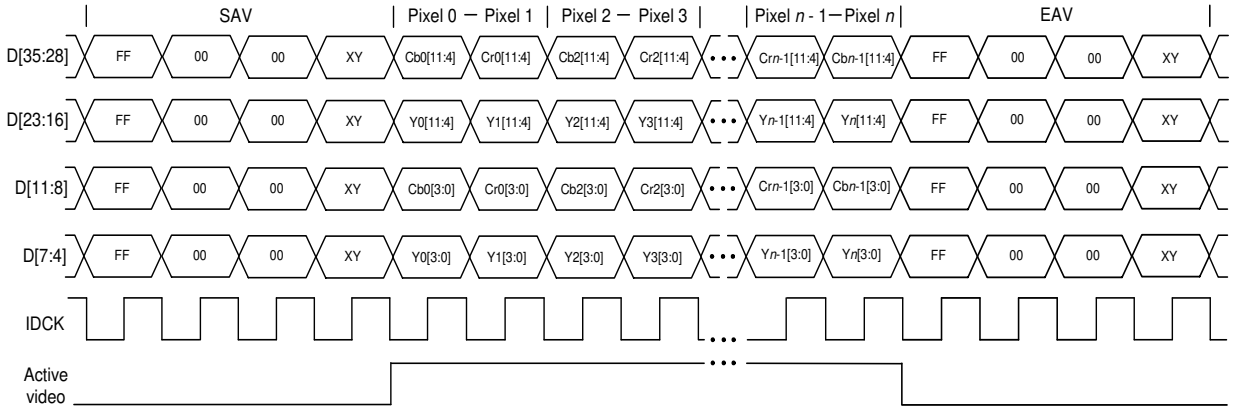


Figure 6.15. 12-Bit Color Depth YC 4:2:2 Embedded Sync Timing

6.16.5. YC Mux 4:2:2 Separate Sync Formats

The video data is multiplexed onto fewer pins than the mapping described in the YC 4:2:2 Separate Sync Formats on page 36. The clock rate is doubled so a chroma value is sent for each pixel, followed by a corresponding luma value for the same pixel. Thus, a luma (Y) value is provided for each pixel, while the Cb and Cr values alternate on successive pixels. Each group of four columns in Table 6.11 shows the four clock cycles for the first two pixels of the line. Pixel values for Cb0 and Y0 values are sent with the first pixel (first two clock cycles). Then the Cr0 and Y1 values are sent with the second pixel (next two clock cycles). The figures below the table show how this pattern is extended for the rest of the pixels in a video line of n + 1 pixels.

Table 6.11. YC Mux 4:2:2 Separate Sync Data Mapping

Pin Name	8-bit Data Bus 8-bit Color Depth				10-bit Data Bus 10-bit Color Depth				12-bit Data Bus 12-bit Color Depth			
	Clock cycle				Clock cycle				Clock cycle			
	First	Second	Third	Fourth	First	Second	Third	Fourth	First	Second	Third	Fourth
D[3:0]	LOW				LOW				LOW			
D4	LOW				LOW				Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D5	LOW				LOW				Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D6	LOW				Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D7	LOW				Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D[15:8]	LOW				LOW				LOW			
D16	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D17	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D18	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D19	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D20	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]
D21	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]
D22	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]	Cb0[10]	Y0[10]	Cr0[10]	Y1[10]
D23	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]	Cb0[11]	Y0[11]	Cr0[11]	Y1[11]
D[35:24]	LOW				LOW				LOW			
HSYNC	HSYNC		HSYNC		HSYNC		HSYNC		HSYNC		HSYNC	
VSYNC	VSYNC		VSYNC		VSYNC		VSYNC		VSYNC		VSYNC	
DE	DE		DE		DE		DE		DE		DE	

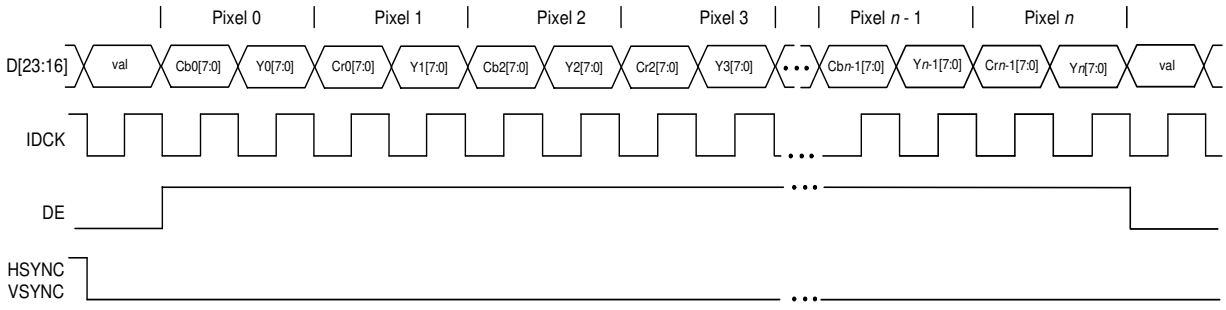


Figure 6.16. 8-Bit Color Depth YC Mux 4:2:2 Timing

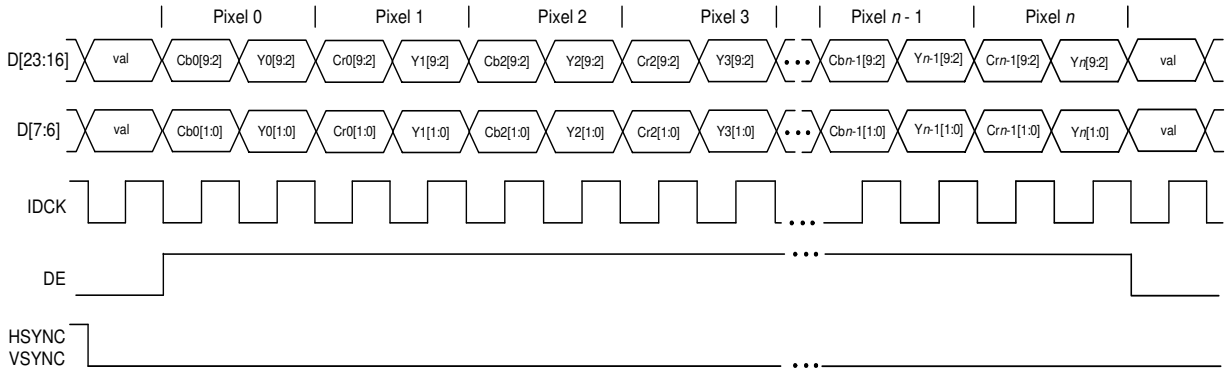


Figure 6.17. 10-Bit Color Depth YC Mux 4:2:2 Timing

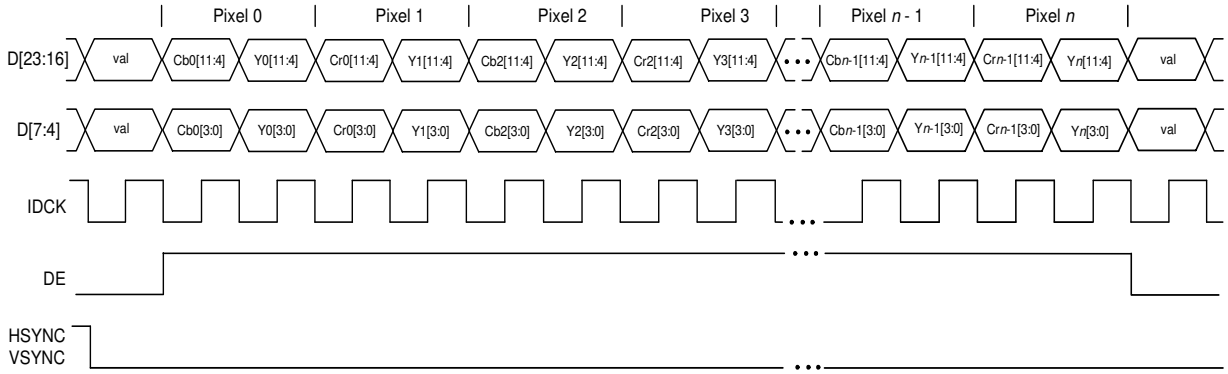


Figure 6.18. 12-Bit Color Depth YC Mux 4:2:2 Timing

6.16.6. YC Mux 4:2:2 Embedded Sync Formats

This format is similar to the one described in the YC Mux 4:2:2 Separate Sync Formats section on page 40, except the syncs are embedded. A luma (Y) value is provided for each pixel, while the Cb and Cr values alternate on successive pixels. Each group of four columns in Table 6.12 shows the four clock cycles for the first two pixels of the line. Pixel values for Cb0 and Y0 values are sent with the first pixel (first two clock cycles). Then the Cr0 and Y1 values are sent with the second pixel (next two clock cycles). The figures following this table show only the first two pixels and last pixel of the line to make room to show the SAV and EAV sequences, but the remaining pixels are similar to those shown in the figures of the previous section.

Table 6.12. YC Mux 4:2:2 Embedded Sync Data Mapping

Pin Name	8-bit Data Bus 8-bit Color Depth				10-bit Data Bus 10-bit Color Depth				12-bit Data Bus 12-bit Color Depth			
	Clock cycle				Clock cycle				Clock cycle			
	First	Second	Third	Fourth	First	Second	Third	Fourth	First	Second	Third	Fourth
D[3:0]	LOW				LOW				LOW			
D4	LOW				LOW				Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D5	LOW				LOW				Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D6	LOW				Cb0[0]	Cb0[2]	Cr0[0]	Cr0[2]	Cr0[2]	Y0[2]	Cb0[2]	Y1[2]
D7	LOW				Cb0[1]	Cb0[3]	Cr0[1]	Cr0[3]	Cr0[3]	Y0[3]	Cb0[3]	Y1[3]
D[15:8]	LOW				LOW				LOW			
D16	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D17	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D18	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D19	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D20	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]
D21	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]
D22	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]	Cb0[10]	Y0[10]	Cr0[10]	Y1[10]
D23	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]	Cb0[11]	Y0[11]	Cr0[11]	Y1[11]
D[35:24]	LOW				LOW				LOW			
HSYNC	LOW				LOW				LOW			
VSYNC	LOW				LOW				LOW			
DE	LOW				LOW				LOW			

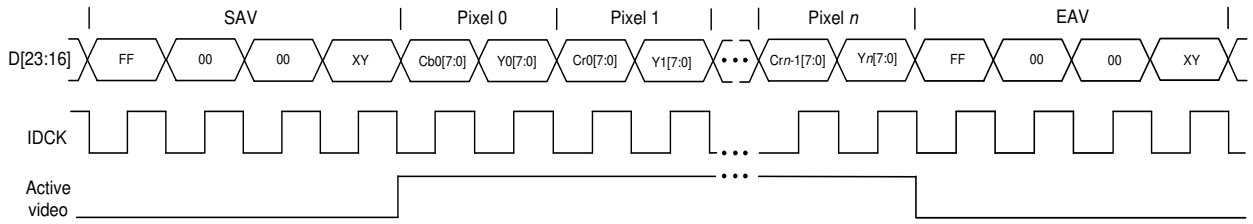


Figure 6.19. 8-Bit Color Depth YC Mux 4:2:2 Embedded Sync Timing

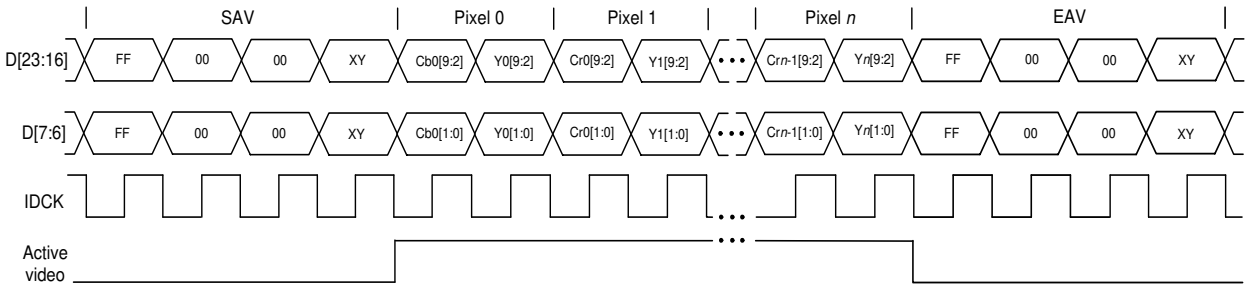


Figure 6.20. 10-Bit Color Depth YC Mux 4:2:2 Embedded Sync Timing

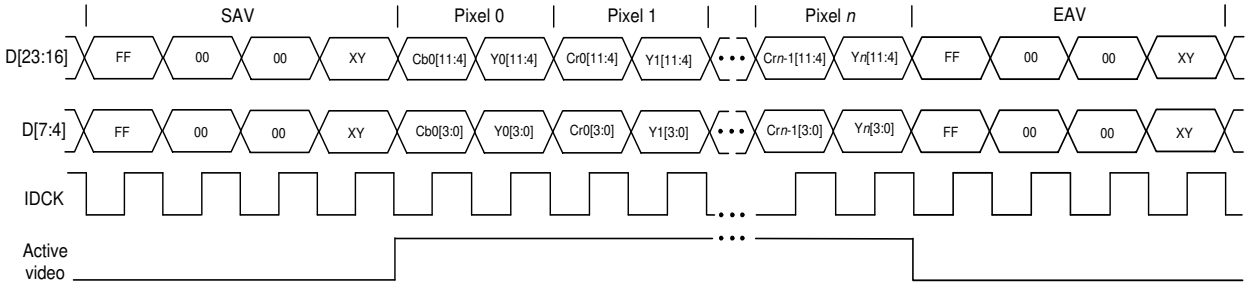


Figure 6.21. 12-Bit Color Depth YC Mux 4:2:2 Embedded Sync Timing

6.16.7. RGB and YCbCr 4:4:4 Dual Edge Mode Formats

The pixel clock runs at the pixel rate and a complete definition of each pixel is received on each clock cycle. One clock edge latches in half the pixel data. The opposite clock edge latches in the remaining half of the pixel data on the same pins. The same timing format is used for RGB and YCbCr 4:4:4. Each pair of columns in Table 6.13 shows the first pixel of *n + 1* pixels in the line of video. The figures below the table show RGB and YCbCr data; the YCbCr 4:4:4 data is given in braces {}. Data and control signals (D*x*, DE, HSYNC, and VSYNC) must change state to meet the setup and hold times specified for the dual edge mode, with respect to the *first* edge of IDCK as defined by the setting of the Edge Select bit. Refer to the Programmer Reference (see the Lattice Semiconductor Documents section on page 52). The figures show IDCK latching input data when the Edge Select bit is set to *1* (first edge is the rising edge). See Table 4.11 on page 18 for the required timing relationships.

Table 6.13. RGB/YCbCr 4:4:4 Separate Sync Dual-Edge Data Mapping

Pin Name	12-bit Data Bus 8-bit Color Depth				15-bit Data Bus 10-bit Color Depth				18-bit Data Bus 12-bit Color Depth				24-bit Data Bus 16-bit Color Depth			
	RGB		YCbCr		RGB		YCbCr		RGB		YCbCr		RGB		YCbCr	
	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge
D0	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	B0[0]	G0[6]	Cb0[0]	Y0[6]	B0[0]	G0[8]	Cb0[0]	Y[08]
D1	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	B0[1]	G0[7]	Cb0[1]	Y0[7]	B0[1]	G0[9]	Cb0[1]	Y[09]
D2	LOW	LOW	LOW	LOW	B0[0]	G0[5]	Cb0[0]	Y0[5]	B0[2]	G0[8]	Cb0[2]	Y0[8]	B0[2]	G0[10]	Cb0[2]	Y[010]
D3	LOW	LOW	LOW	LOW	B0[1]	G0[6]	Cb0[1]	Y0[6]	B0[3]	G0[9]	Cb0[3]	Y0[9]	B0[3]	G0[11]	Cb0[3]	Y[011]
D4	B0[0]	G0[4]	Cb0[0]	Y0[4]	B0[2]	G0[7]	Cb0[2]	Y0[7]	B0[4]	G0[10]	Cb0[4]	Y0[10]	B0[4]	G0[12]	Cb0[4]	Y[012]
D5	B0[1]	G0[5]	Cb0[1]	Y0[5]	B0[3]	G0[8]	Cb0[3]	Y0[8]	B0[5]	G0[11]	Cb0[5]	Y0[11]	B0[5]	G0[13]	Cb0[5]	Y[013]
D6	B0[2]	G0[6]	Cb0[2]	Y0[6]	B0[4]	G0[9]	Cb0[4]	Y0[9]	B0[6]	R0[0]	Cb0[6]	Cr0[0]	B0[6]	G0[14]	Cb0[6]	Y[014]
D7	B0[3]	G0[7]	Cb0[3]	Y0[7]	B0[5]	R0[0]	Cb0[5]	Cr0[0]	B0[7]	R0[1]	Cb0[7]	Cr0[1]	B0[7]	G0[15]	Cb0[7]	Y[015]
D8	B0[4]	R0[0]	Cb0[4]	Cr0[0]	B0[6]	R0[1]	Cb0[6]	Cr0[1]	B0[8]	R0[2]	Cb0[8]	Cr0[2]	B0[8]	R0[0]	Cb0[8]	Cr[00]
D9	B0[5]	R0[1]	Cb0[5]	Cr0[1]	B0[7]	R0[2]	Cb0[7]	Cr0[2]	B0[9]	R0[3]	Cb0[9]	Cr0[3]	B0[9]	R0[1]	Cb0[9]	Cr[01]
D10	B0[6]	R0[2]	Cb0[6]	Cr0[2]	B0[8]	R0[3]	Cb0[8]	Cr0[3]	B0[10]	R0[4]	Cb0[10]	Cr0[4]	B0[10]	R0[2]	Cb0[10]	Cr[02]
D11	B0[7]	R0[3]	Cb0[7]	Cr0[3]	B0[9]	R0[4]	Cb0[9]	Cr0[4]	B0[11]	R0[5]	Cb0[11]	Cr0[5]	B0[11]	R0[3]	Cb0[11]	Cr[03]
D12	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	G0[0]	R0[6]	Y0[0]	Cr0[6]	B0[12]	R0[4]	Cb0[12]	Cr[04]
D13	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	G0[1]	R0[7]	Y0[1]	Cr0[7]	B0[13]	R0[5]	Cb0[13]	Cr[05]
D14	LOW	LOW	LOW	LOW	G0[0]	R0[5]	Y0[0]	Cr0[5]	G0[2]	R0[8]	Y0[2]	Cr0[8]	B0[14]	R0[6]	Cb0[14]	Cr[06]
D15	LOW	LOW	LOW	LOW	G0[1]	R0[6]	Y0[1]	Cr0[6]	G0[3]	R0[9]	Y0[3]	Cr0[9]	B0[15]	R0[7]	Cb0[15]	Cr[07]
D16	G0[0]	R0[4]	Y0[0]	Cr0[4]	G0[2]	R0[7]	Y0[2]	Cr0[7]	G0[4]	R0[10]	Y0[4]	Cr0[10]	G0[0]	R0[8]	Y0[0]	Cr[08]
D17	G0[1]	R0[5]	Y0[1]	Cr0[5]	G0[3]	R0[8]	Y0[3]	Cr0[8]	G0[5]	R0[11]	Y0[5]	Cr0[11]	G0[1]	R0[9]	Y0[1]	Cr[09]
D18	G0[2]	R0[6]	Y0[2]	Cr0[6]	G0[4]	R0[9]	Y0[4]	Cr0[9]	LOW	LOW	LOW	LOW	G0[2]	R0[10]	Y0[2]	Cr[010]
D19	G0[3]	R0[7]	Y0[3]	Cr0[7]	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	G0[3]	R0[11]	Y0[3]	Cr[011]
D20	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	G0[4]	R0[12]	Y0[4]	Cr[012]
D21	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	G0[5]	R0[13]	Y0[5]	Cr[013]
D22	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	G0[6]	R0[14]	Y0[6]	Cr[014]
D23	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	G0[7]	R0[15]	Y0[7]	Cr[015]
HS	HS	HS	HS	HS	HS	HS	HS	HS	HS	HS	HS	HS	HS	HS	HS	HS
VS	VS	VS	VS	VS	VS	VS	VS	VS	VS	VS	VS	VS	VS	VS	VS	VS
DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE

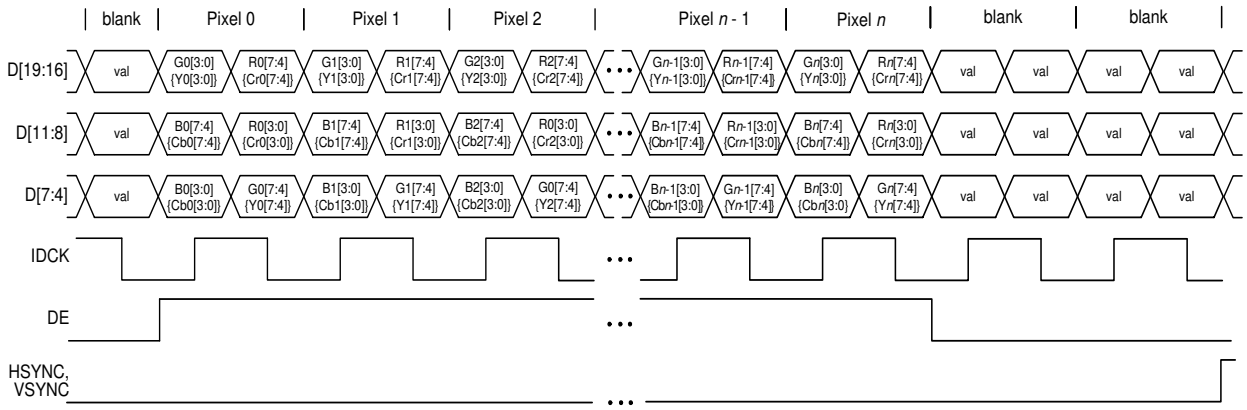


Figure 6.22. 8-Bit Color Depth 4:4:4 Dual Edge Timing

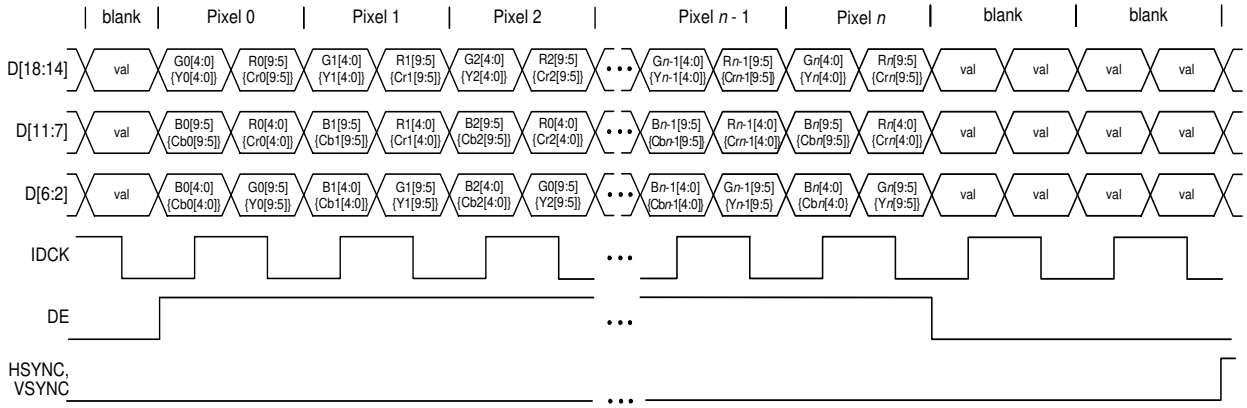


Figure 6.23. 10-Bit Color Depth 4:4:4 Dual Edge Timing

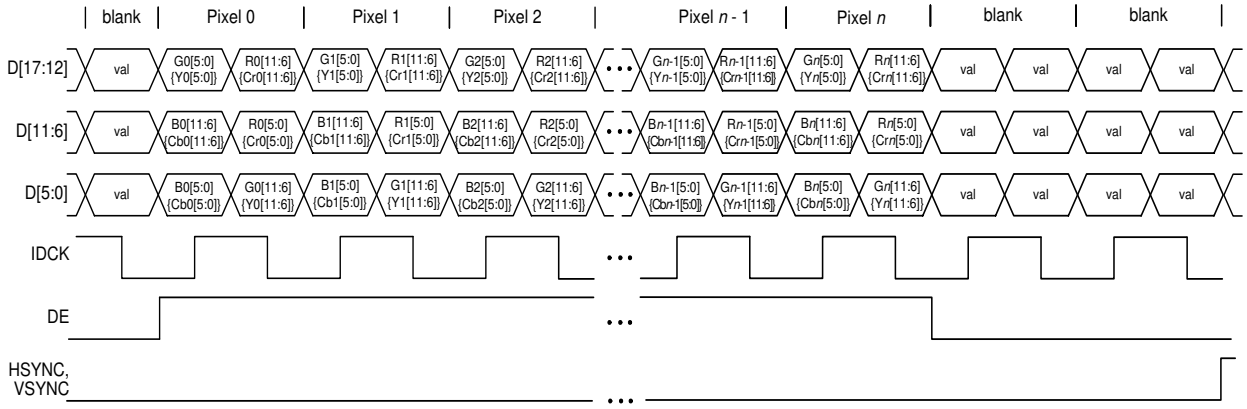


Figure 6.24. 12-Bit Color Depth 4:4:4 Dual Edge Timing

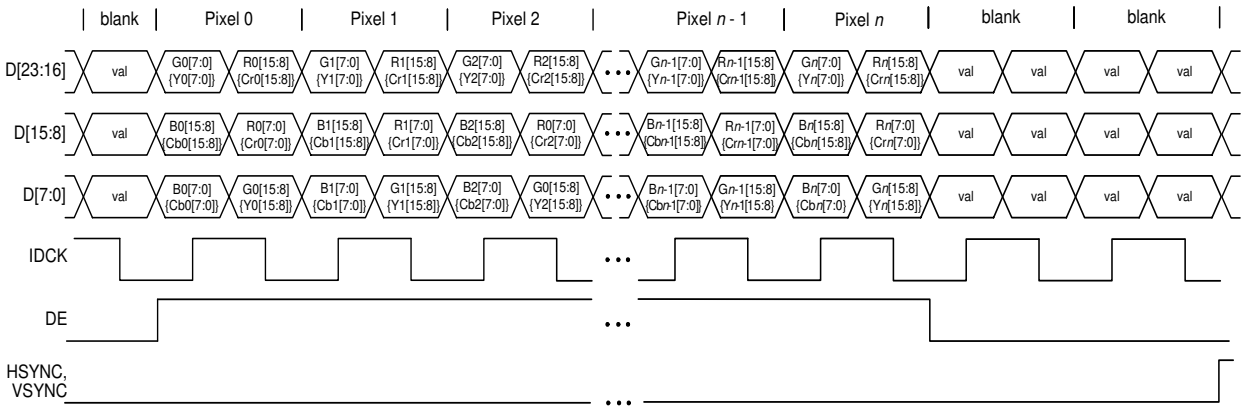


Figure 6.25. 16-Bit Color Depth 4:4:4 Dual Edge Timing

7. Design Recommendations

7.1. Power Supply Decoupling

Designers should include decoupling and bypass capacitors at each power pin in the layout. Figure 7.1 shows this schematically. Figure 7.2 shows a representative layout of the various types of power connections on the transmitter. Connections in any one group, such as all the CVCC12 pins, can share C2, C3, and the ferrite. Locate a separate C1 as close as possible to the VCC pin. The recommended impedance of the ferrite is 10 Ω or more in the frequency range of 1 MHz to 2 MHz.

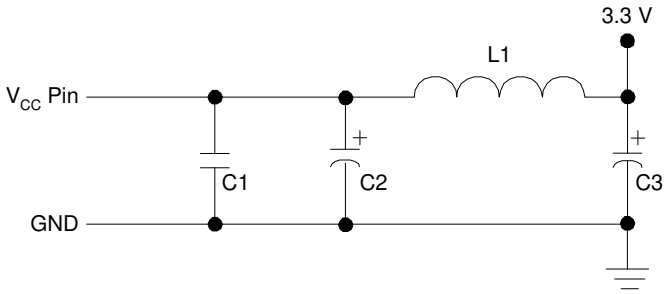


Figure 7.1. Decoupling and Bypass Schematic

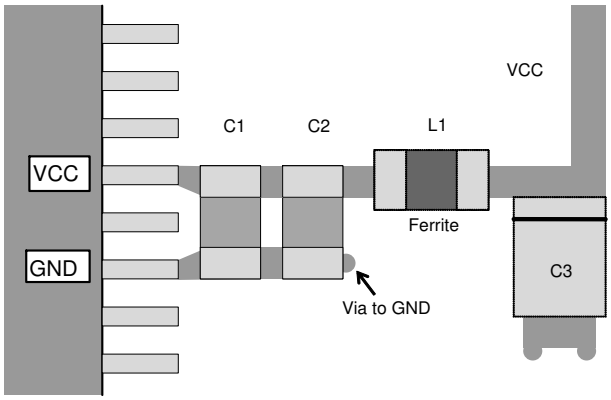


Figure 7.2. Decoupling and Bypass Capacitor Placement

7.2. Power Supply Sequencing

All power supplies in the SiI9136-3/SiI1136 transmitter are independent. However, identical supplies must be provided at the same time. Independent supplies do not have any sequencing requirements.

7.3. ESD Recommendations

The SiI9136-3/SiI1136 transmitter can withstand electrostatic discharges due to handling during manufacture up to 4 kV HBM. In applications where higher protection levels are required, ESD-limiting components can be placed on the pins of the device. These components typically have a capacitive effect that reduces the signal quality on the differential lines at higher clock frequencies, so use the lowest capacitance devices possible on these lines. In no case should the capacitance value exceed 1 pF.

7.4. High-Speed TMDS Signals

7.4.1. Layout Guidelines

These layout guidelines help to ensure signal integrity. Lattice Semiconductor encourages the board designer to follow these guidelines as closely as possible.

- Locate the output connector that carries the TMDS signals as close as possible to the device.
- Route the differential lines as directly as possible from the connector to the device pins.
- Route the two traces of each differential pair together.
- Minimize the number of vias through which the signal lines pass.
- Lay out the two traces of each differential pair with a controlled differential impedance of 100 Ω.

Because Lattice Semiconductor devices are tolerant of skews between differential pairs, spiral skew compensation for path length differences is not required.

7.4.2. TMDS Output Recommendation

The SiI9136-3/SiI1136 transmitter is capable of sending frequencies of up to 300 MHz over the TMDS clock line.

If the output of the transmitter is connected to an HDMI connector, the output port must be HDMI-compliant. The TMDS output is designed to give the maximum horizontal eye opening by speeding up the rise and fall time to the minimum value of 75 ps allowed by the HDMI Specification. Depending on the design layout and with light loading, it is possible to see rise times slightly faster than 75 ps. Adding components such as common mode filters and ESD suppression devices slows down the rise and fall time to well within the specification. If these components are not in the design, adding a discrete capacitor of approximately 1 pF from each of the differential signal traces to ground can solve this compliance issue.

The following external components have been tested for output compliance. Components with similar capacitance can also be used:

- Common mode filter: TDK ACM2012H
- ESD suppression diode: Semtech RClamp0524P. Semtech also makes a pin-compatible device, Semtech SRV05, that Lattice Semiconductor has not tested but for which similar compliance performance is expected.

7.4.3. EMI Considerations

Electromagnetic interference is a function of board layout, shielding, operating voltage and frequency, and so on. When attempting to control emissions, do not place any passive components on the differential signal lines, except for the ESD protection described earlier. The differential signals used in HDMI are inherently low in EMI if the routing recommendations noted in the Layout Guidelines section are followed.

The PCB ground plane should extend unbroken under as much of the transmitter chip and associated circuitry as possible, with all ground signals of the chip using a common ground.

8. Packaging

8.1. ePad Requirements

The SiI9136-3/SiI1136 HDMI Deep Color Transmitter chip is packaged in a 100-pin, 14 mm x 14mm TQFP package with an ePad that is used for the electrical ground of the device and for improved thermal transfer characteristics. The ePad dimensions are 5 mm x 5 mm ±0.20 mm. Soldering the ePad to the ground plane of the PCB is **required** to meet package power dissipation requirements at full speed operation, and to correctly connect the chip circuitry to electrical ground. A clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical shorts.

The thermal land area on the PCB may use thermal vias to improve heat removal from the package. These thermal vias also double as the ground connections of the chip and must attach internally in the PCB to the ground plane. An array of vias should be designed into the PCB beneath the package. For optimum thermal performance, the via diameter should be 12 mils to 13 mils (0.30 mm to 0.33 mm) and the via barrel should be plated with 1-ounce copper to plug the via. This design helps to avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be tented with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

Package stand-off when mounting the device also needs to be considered. For a nominal stand-off of approximately 0.1 mm the stencil thickness of 5 mils to 8 mils should provide a good solder joint between the ePad and the thermal land.

8.2. PCB Layout Guidelines

PCB layout designers should refer to Lattice Semiconductor Application Note *PCB Layout Guidelines: Designing with Exposed Pads* (SiI-AN-0129) for basic design guidelines when designing with thermally enhanced packages using ePad.

8.3. Package Dimensions

These drawings are not to scale.

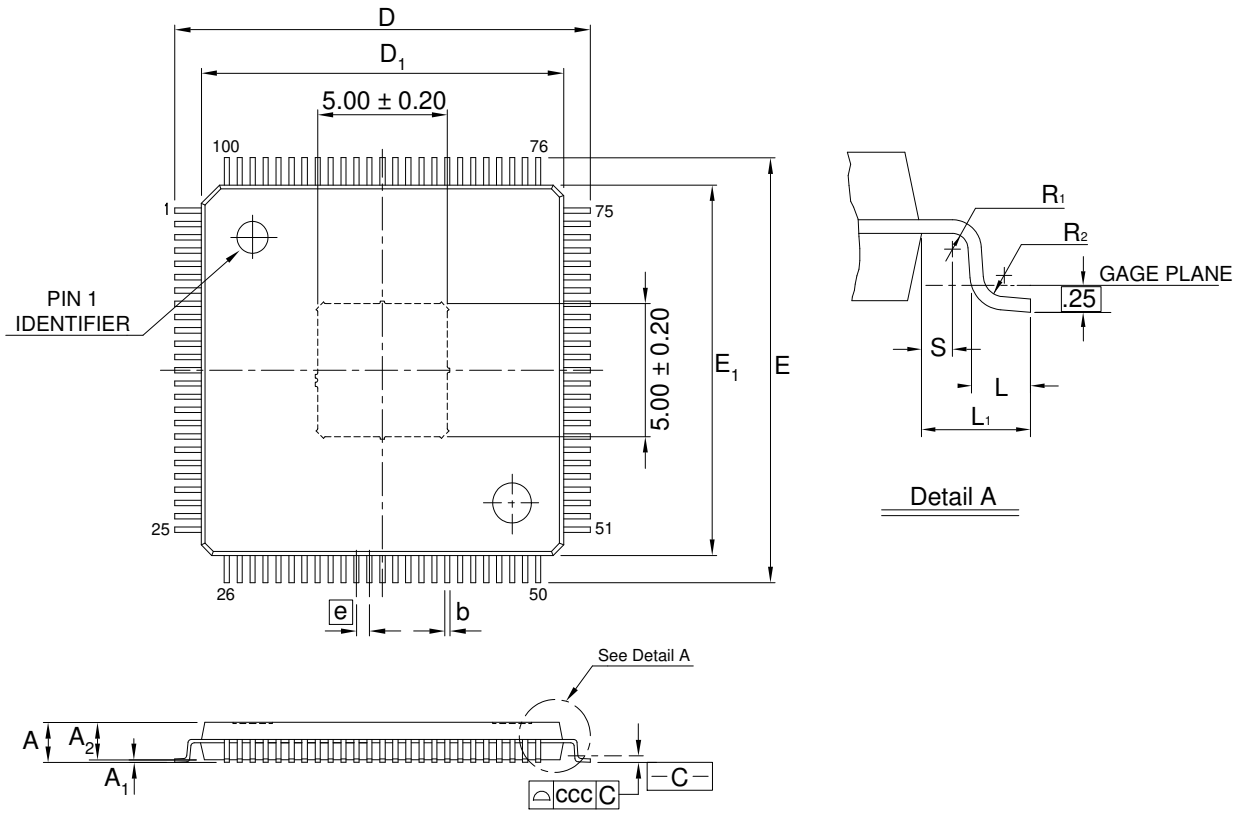


Figure 8.1. 100-Pin Package Diagram

JEDEC Package Code MS-026

Item	Description	Min	Typ	Max
A	Thickness	—	—	1.20
A1	Stand-off	0.05	—	0.15
A2	Body thickness	0.95	1.00	1.05
D	Footprint		16.00 BSC	
E	Footprint		16.00 BSC	
D_1	Body size		14.00 BSC	
E_1	Body size		14.00 BSC	
b	Lead width	0.17	0.22	0.27

Item	Description	Min	Typ	Max
C	Lead thickness	0.09	—	0.20
e	Lead pitch		0.50 BSC	
L	Lead foot length	0.45	0.60	0.75
L_1	Total lead length		1.00 REF	
R_1	Lead radius, inside	0.08	—	—
R_2	Lead radius, outside	0.08	—	0.20
S	Lead horizontal run	0.20	—	—
ccc	Lead coplanarity		0.08	

Dimensions given in mm.

8.4. Marking Specification

This marking drawing is not to scale.

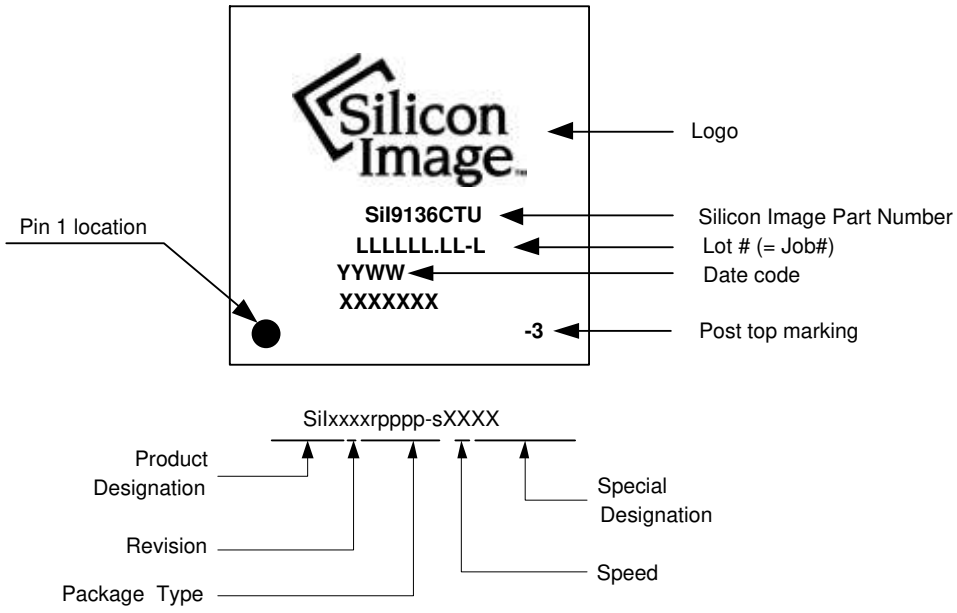


Figure 8.2. Marking Diagram

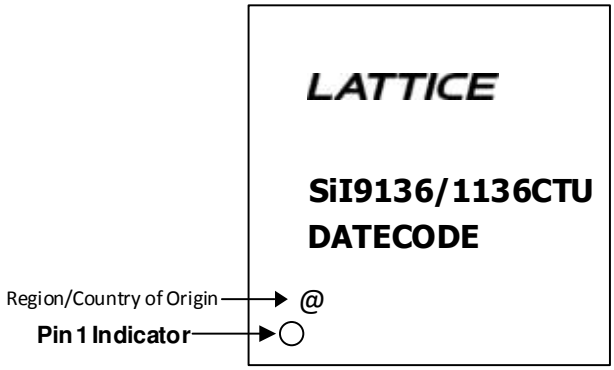


Figure 8.3. Alternate Topside Marking

8.5. Ordering Information

Production Part Numbers:

Device	Part Number
Standard	SiI9136CTU-3
Non-HDCP	SiI1136CTU

The universal package can be used in lead-free and ordinary process lines.

References

Standards Documents

This is a list of standards abbreviations appearing in this document, and references to their respective specifications documents.

Abbreviation	Standards publication, organization, and date
HDMI	*High Definition Multimedia Interface, Revision 1.4a,* HDMI Consortium, March 2010
HCTS	*HDMI Compliance Test Specification, Revision 1.4a,* HDMI Consortium, March 2010
HDCP	*High-bandwidth Digital Content Protection, Revision 1.4*, Digital Content Protection, LLC; July 2009
E-EDID	*Enhanced Extended Display Identification Data Standard,* Release A Revision 1, VESA; Feb. 2000
E-DID IG	*VESA EDID Implementation Guide*, VESA, June 2001
CEA-861-D	*A DTV Profile for Uncompressed High Speed Digital Interfaces,* EIA/CEA; July 2006
EDDC	*Enhanced Display Data Channel Standard, Version 1.1,* VESA; March 2004
ITU-R BT.601	*Studio encoding parameters of digital television for standard 4:3 and wide screen 16:9 aspect ratios*, International Telecommunications Union, January 2007
ITU-R BT.656	*Interface for digital component video signals in 525-line and 625-line television systems operating at the 4:2:2 level of Recommendation ITU-R BT.601*, International Telecommunications Union, December 2007
ITU-R BT.709	*Parameter values for the HDTV standards for production and international programme exchange*, International Telecommunications Union, April 2002
IEC 61966-2-4	*Multimedia systems and equipment - Colour measurement and management - Part 2-4: Colour management - Extended-gamut YCC colour space for video applications – xvYCC*, International Electrotechnical Commission, January 2006
ACPI	*Advanced Configuration and Power Interface*, Revision 4.0, Hewlett-Packard/Intel/Microsoft/Phoenix/ Toshiba, June, 2009
BTA T-1004	*Video Signal Interfaces for EDTV-II Studio Equipment*, Version 1.0, ARIB; June 1995

Standards Groups

For information on the specifications that apply to this document, contact the responsible standards groups appearing on this list.

Standards Organization	Web URL
ANSI/EIA/CEA	http://global.ihs.com
VESA	http://www.vesa.org
HDCP	http://www.digital-cp.com
DVI	http://www.ddwg.org
HDMI	http://www.hdmi.org
ITU	http://www.itu.int
IEC	http://www.iec.org
ARIB	http://www.arib.or.jp

Lattice Semiconductor Documents

This is a list of the related documents that are available from your Lattice Semiconductor sales representative. *The Programmer's Reference requires an NDA with Lattice Semiconductor.*

Document	Title
SiI-PR-1032	*Transmitter Programming Interface (TPI) Programmer Reference*
SiI-PR-0041	*CEC Programming Interface (CPI) Programmer Reference*
SiI-AN-1029	*PCB Layout Guidelines: Designing with Exposed Pads*
SiI-PR-1018	*Repeater Programming Interface (RTPI) Programmer Reference*
SiI-UG-1068	*CP9136-3/CP1136 Transmitter/Repeater Starter Kit User Guide*

Technical Support

For technical support questions, contact your regional sales manufacturer representative or distributor. For contact information, visit the Lattice Semiconductor web site at www.latticesemi.com.

Revision History

Revision D, June 2017

Marking spec changed as per PCN13A16. Added Figure 8.3. Alternate Topside Marking.

Revision C, February 2016

Added SiI1136 transmitter support and updated to latest template.

Revision B, July 2013

1. Add YC Mux 480i support.
2. Update to 300 MHz maximum frequency in Deep Color Support section.
3. Update Table 19 for 4K formats.
4. Update Table 24 and Table 25 for correct order of sending Cr0 and Cb1.

Revision A, October 2010

First Production release.

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