BLC9G27LS-150AV

Power LDMOS transistor

Rev. 4 — 24 May 2017

AMPLEON

Product data sheet

1. Product profile

1.1 General description

150 W LDMOS packaged asymmetrical Doherty power transistor for base station applications at frequencies from 2496 MHz to 2690 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in the Doherty application demo circuit.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
IS-95	2500 to 2690	28	28.2	14.8	48	–40 [1]

[1] Test signal: IS-95 with pilot, paging, sync, 6 traffic channels with Walsh codes 8 - 13; PAR = 9.7 dB at 0.01 % probability.

1.2 Features and benefits

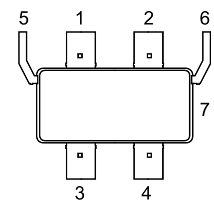
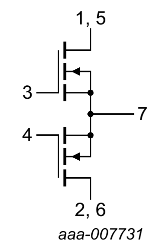
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Decoupling leads to enable improved video bandwidth
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

1.3 Applications

- RF power amplifier for W-CDMA base stations and multi carrier applications in the 2496 MHz to 2690 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1 (main)		
2	drain2 (peak)		
3	gate1 (main)		
4	gate2 (peak)		
5	video decoupling (main)		
6	video decoupling (peak)		
7	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC9G27LS-150AV	-	air cavity plastic earless flanged package; 6 leads	SOT1275-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	T_{case} = 80 °C; V_{DS} = 28 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = 0.7 V		
		P_L = 28 W	0.381	K/W
		P_L = 80 W	0.299	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.6 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 60 mA	1.5	2.1	3.1	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 360 mA	1.7	2.3	3.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	12	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 60 mA	-	0.55	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 2.1 A	-	174	385	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.9 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 90 mA	1.5	2.2	3.1	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 540 mA	1.7	2.4	3.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	18	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 90 mA	-	0.77	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 3.15 A	-	145	260	mΩ

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 - 64 DPCH; f_1 = 2496 MHz; f_2 = 2690 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 400 mA (main); $V_{GS(amp)peak}$ = 0.7 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at 2496 MHz to 2690 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 28 W	13.3	15	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 28 W	-	−9	−6	dB
η_D	drain efficiency	$P_{L(AV)}$ = 28 W	39	44	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 28 W	-	−26	−22	dBc

Table 8. RF characteristics

Test signal: pulsed CW; t_p = 100 μs; δ = 10 %; f = 2690 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 300 mA (main); $V_{GS(amp)peak}$ = 0.7 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at 2496 MHz to 2690 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression		116	149	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLC9G27LS-150AV is capable of withstanding a load mismatch corresponding to a VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 250 mA (main); $V_{GS(amp)peak}$ = 0.7 V; P_L = 90 W (CW); f = 2500 MHz.

7.2 Impedance information

Table 9. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 350 mA (main); V_{DS} = 28 V.

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
2500	2.8 – j8.4	2.7 – j8.3	92	60.7	14.4
2600	3.2 – j8.4	2.7 – j8.3	89	60.3	15.3
2700	3.7 – j8.8	2.7 – j8.3	90	62.6	16.4
Maximum drain efficiency load					
2500	2.8 – j8.4	4.8 – j5.9	64	69.2	16.8
2600	3.2 – j8.4	4.0 – j5.6	61	69.4	17.9
2700	3.7 – j8.8	3.0 – j6.0	61	69.6	19.0

[1] Z_S and Z_L defined in Figure 1.

[2] at 3 dB gain compression.

Table 10. Typical impedance of peak device

Measured load-pull data of peak device; I_{Dq} = 550 mA (peak); V_{DS} = 28 V.

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
2500	2.5 – j8.9	4.7 – j7.4	123	62.8	15.1
2600	3.2 – j9.4	4.0 – j7.6	126	62.6	15.4
2700	3.8 – j10.6	4.8 – j8.2	120	60.6	16.0
Maximum drain efficiency load					
2500	2.5 – j8.9	3.2 – j4.3	85	70.1	16.6
2600	3.2 – j9.4	3.1 – j4.9	84	70.2	18.0
2700	3.8 – j10.6	3.5 – j5.8	92	68.4	18.6

[1] Z_S and Z_L defined in Figure 1.

[2] at 3 dB gain compression.

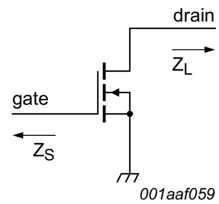


Fig 1. Definition of transistor impedance

7.3 Recommended impedances for Doherty design

Table 11. Typical impedance of main device at 1 : 1 load
Measured load-pull data of main device; I_{Dq} = 350 mA (main); V_{DS} = 28 V.

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [3]	G_p [3]
(MHz)	(Ω)	(Ω)	(dBm)	(%)	(dB)
2500	2.8 – j8.4	3.8 – j6.9	49.0	44.4	19.0
2600	3.2 – j8.4	3.8 – j6.9	48.8	46.3	20.2
2700	3.7 – j8.8	3.2 – j7.1	48.8	46.5	21.1

[1] Z_S and Z_L defined in Figure 1.

[2] at 3 dB gain compression.

[3] at $P_{L(AV)}$ = 44.5 dBm.

Table 12. Typical impedance of main device at 1 : 2.5 load
Measured load-pull data of main device; I_{Dq} = 350 mA (main); V_{DS} = 28 V.

f	Z_S [1]	Z_L [1]	P_L [3]	η_D [3]	G_p [3]
(MHz)	(Ω)	(Ω)	(dBm)	(%)	(dB)
2500	2.8 – j8.4	3.6 – j3.4	44.5	52.9	20.1
2600	3.2 – j8.4	3.6 – j3.4	44.5	53.2	21.4
2700	3.7 – j8.8	3.3 – j3.7	44.5	54.1	22.2

[1] Z_S and Z_L defined in Figure 1.

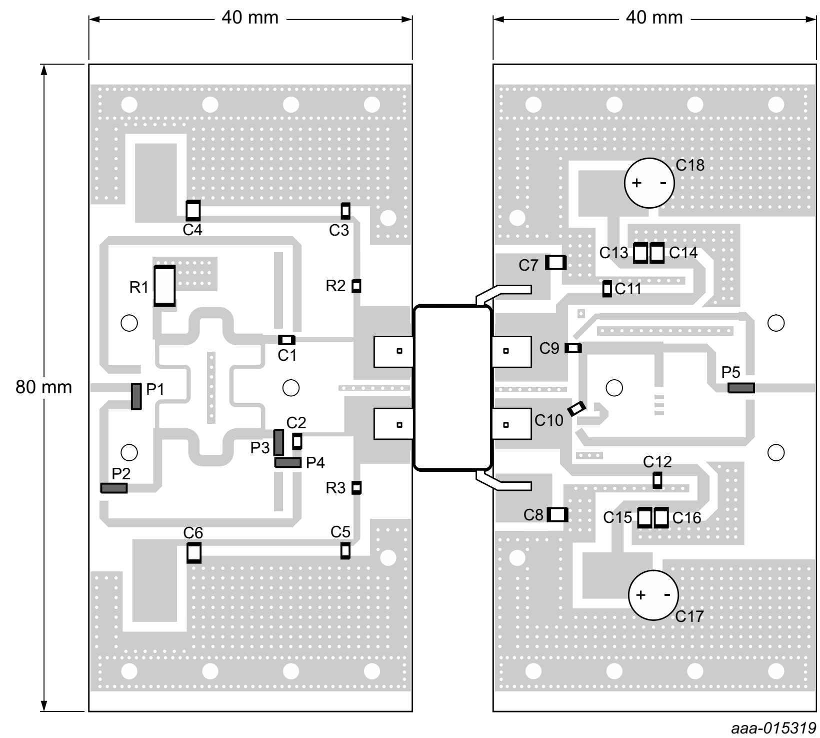
[2] at 3 dB gain compression.

[3] at $P_{L(AV)}$ = 44.5 dBm.

7.4 VBW in Doherty operation

The BLC9G27LS-150AV shows 100 MHz (typical) video bandwidth in Doherty demo board in 2600 MHz at V_{DS} = 28 V; I_{Dq} = 250 mA and $V_{GS(amp)peak}$ = 0.7 V.

7.5 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; ε_r = 3.5; thickness = 0.508 mm; thickness copper plating = 35 μm.

See Table 13 for a list of components.

Fig 2. Component layout

Table 13. List of components

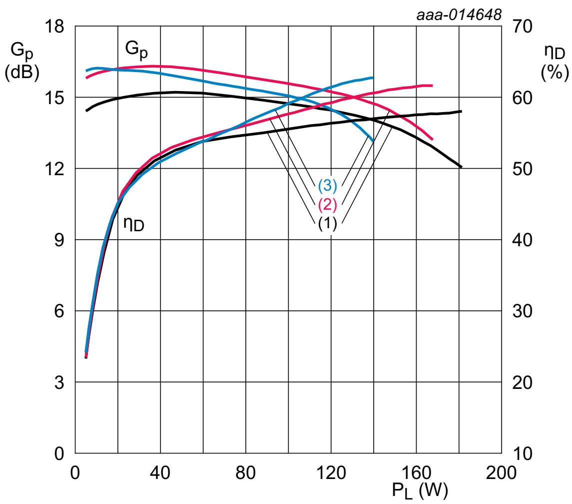
See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C2, C3, C5, C11, C12	multilayer ceramic chip capacitor	12 pF	ATC 600F
C4, C6, C7, C8, C13, C14, C15, C16	multilayer ceramic chip capacitor	10 μF	Murata, SMD 1206
C9	multilayer ceramic chip capacitor	3.0 pF	ATC 600F
C10	multilayer ceramic chip capacitor	18 pF	ATC 600F
C17, C18	electrolytic capacitor	2200 μF, 63 V	BCcomponents
P1, P2, P3, P4, P5	copper foil strip	-	needed for tuning
R1	resistor	50 Ω	SMD 2512
R2, R3	resistor	5.1 Ω	SMD 0805

7.6 Graphical data

All data are measured on a demo application circuit.

7.6.1 Pulsed CW



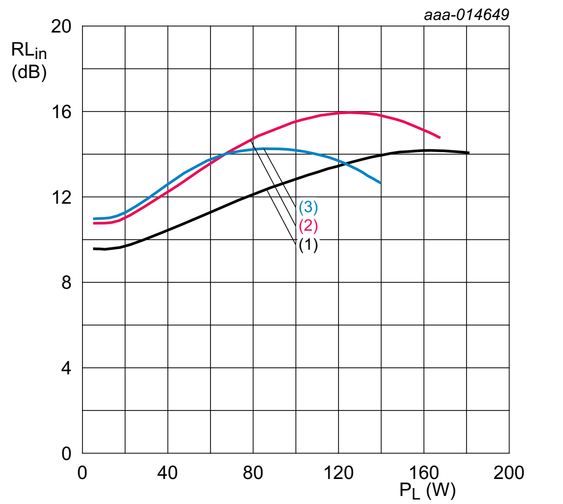
V_{DS} = 28 V; I_{Dq} = 250 mA (main device); $V_{GS(amp)peak}$ = 0.7 V; t_p = 100 μs; δ = 10 %.

(1) f = 2496 MHz

(2) f = 2600 MHz

(3) f = 2690 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 250 mA (main device); $V_{GS(amp)peak}$ = 0.7 V; t_p = 100 μs; δ = 10 %.

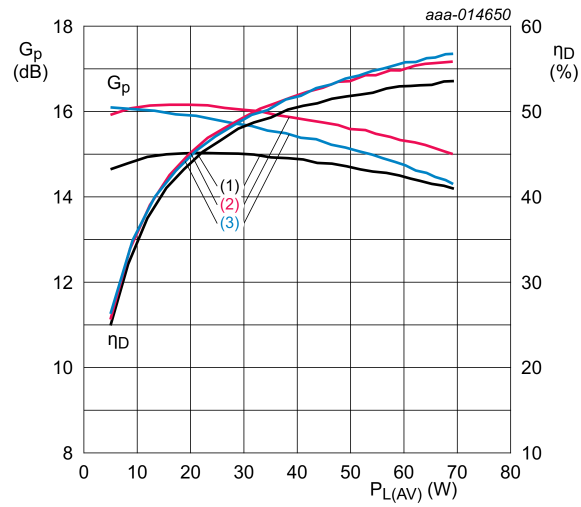
(1) f = 2496 MHz

(2) f = 2600 MHz

(3) f = 2690 MHz

Fig 4. Input return loss as a function of output power; typical values

7.6.2 1-Carrier W-CDMA



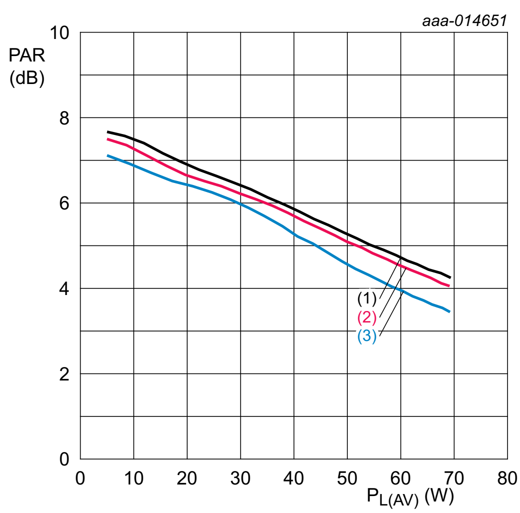
V_{DS} = 28 V; I_{Dq} = 250 mA (main device); $V_{GS(amp)peak}$ = 0.7 V.

(1) f = 2496 MHz

(2) f = 2600 MHz

(3) f = 2690 MHz

Fig 5. Power gain and drain efficiency as function of average output power; typical values



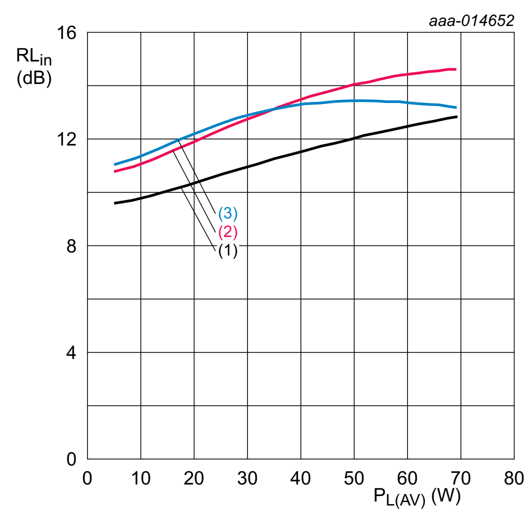
V_{DS} = 28 V; I_{Dq} = 250 mA (main device); $V_{GS(amp)peak}$ = 0.7 V.

(1) f = 2496 MHz

(2) f = 2600 MHz

(3) f = 2690 MHz

Fig 6. Peak-to-average power ratio as a function of average output power; typical values



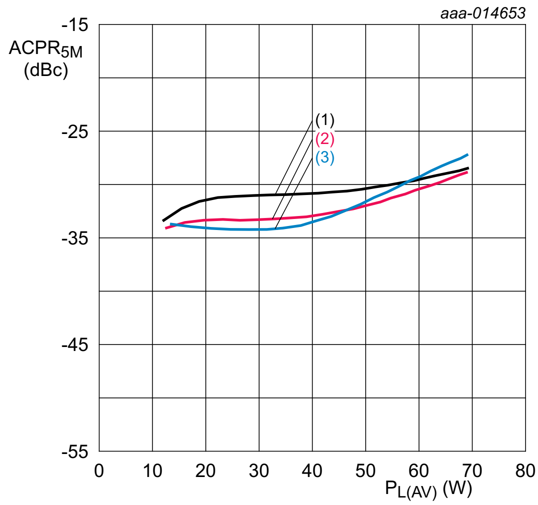
V_{DS} = 28 V; I_{Dq} = 250 mA (main device); $V_{GS(amp)peak}$ = 0.7 V.

(1) f = 2496 MHz

(2) f = 2600 MHz

(3) f = 2690 MHz

Fig 7. Input return loss as a function of average output power; typical values



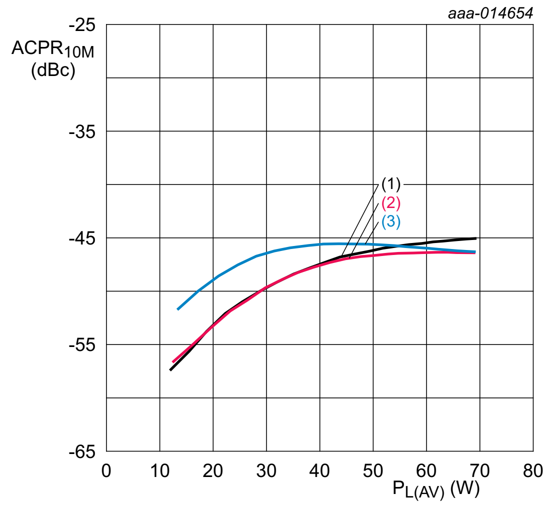
V_{DS} = 28 V; I_{Dq} = 250 mA (main device); $V_{GS(amp)peak}$ = 0.7 V.

(1) f = 2496 MHz

(2) f = 2600 MHz

(3) f = 2690 MHz

Fig 8. Adjacent channel power ratio (5 MHz) as a function of average output power; typical values



V_{DS} = 28 V; I_{Dq} = 250 mA (main device); $V_{GS(amp)peak}$ = 0.7 V.

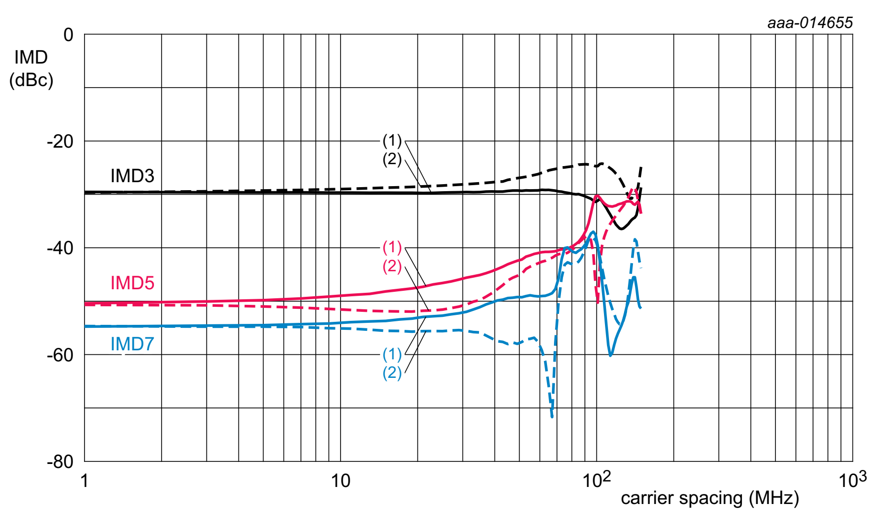
(1) f = 2496 MHz

(2) f = 2600 MHz

(3) f = 2690 MHz

Fig 9. Adjacent channel power ratio (10 MHz) as a function of average output power; typical values

7.6.3 2-Tone VBW



V_{DS} = 28 V; I_{Dq} = 250 mA (main device); f_c = 2600 MHz.

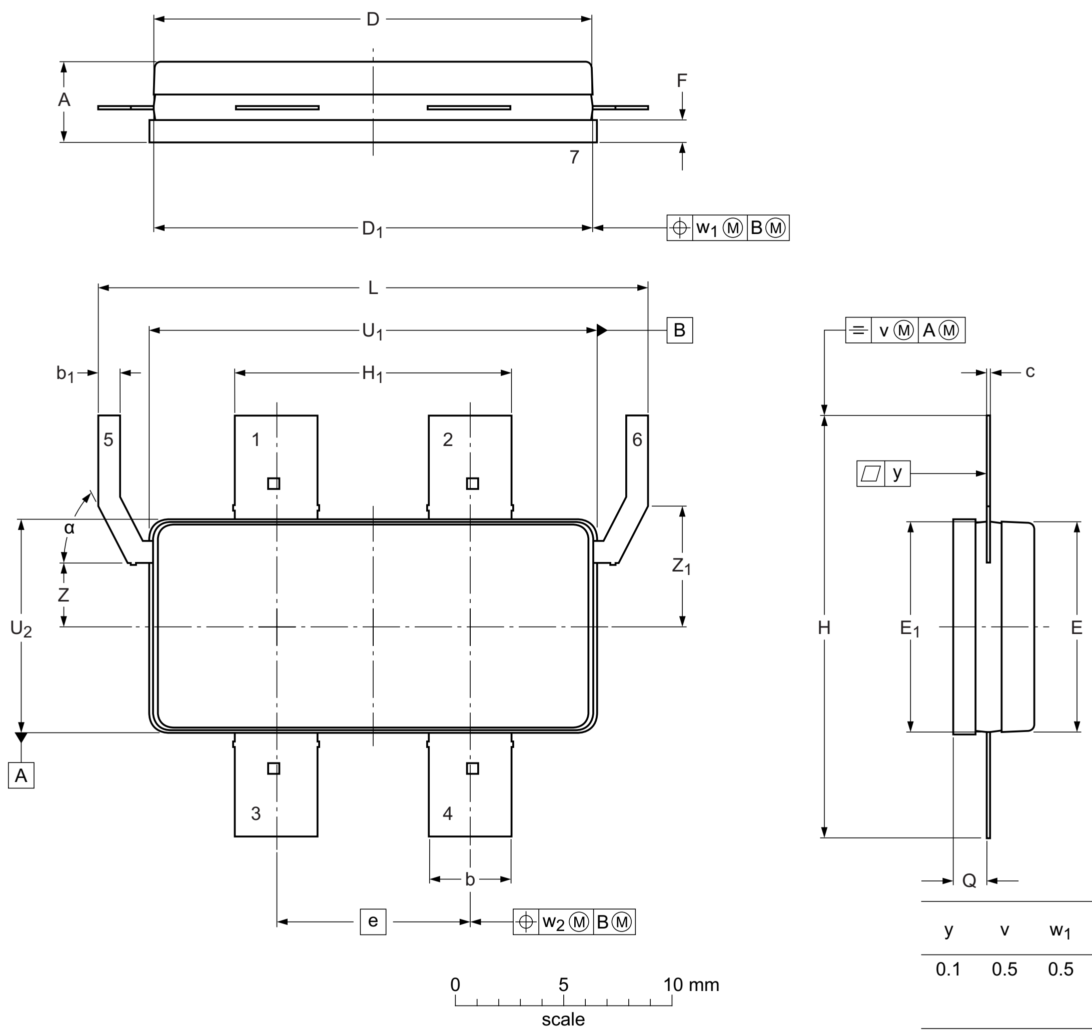
(1) IMD low

(2) IMD high

Fig 10. VBW capability on Doherty application demo circuit

8. Package outline

Air cavity plastic earless flanged package; 6 leads **SOT1275-1**



y	v	w_1	w_2
0.1	0.5	0.5	0.5

Dimensions

Unit		A	b	b_1	c	D	D_1	E	E_1	e	F	H	H_1	L	Q(1)	U_1	U_2	Z	Z_1	α
mm	max	4.01	3.94	1.14	0.178	20.42	20.37	9.80	9.75		1.14	19.53	12.80	25.40	1.68	20.70	9.91	3.17	5.79	65°
	nom									8.89										
	min	3.40	3.68	0.89	0.127	20.12	20.17	9.50	9.55		0.94	19.33	12.60	25.20	1.45	20.50	9.70	2.67	5.29	61°

Note

1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1275-1_po

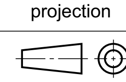
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1275-1						~~16-11-15~~ 17-04-13

Fig 11. Package outline SOT1275-1

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 14. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

10. Abbreviations

Table 15. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
IS-95	Interim Standard 95
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC9G27LS-150AV v.4	20170524	Product data sheet	-	BLC9G27LS-150AV v.3
Modifications:	• Figure 11 on page 10: updated package outline drawing SOT1275-1			
BLC9G27LS-150AV v.3	20161220	Product data sheet	-	BLC9G27LS-150AV v.2
BLC9G27LS-150AV v.2	20150901	Product data sheet	-	BLC9G27LS-150AV v.1
BLC9G27LS-150AV v.1	20141106	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

12.2 Definitions

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