

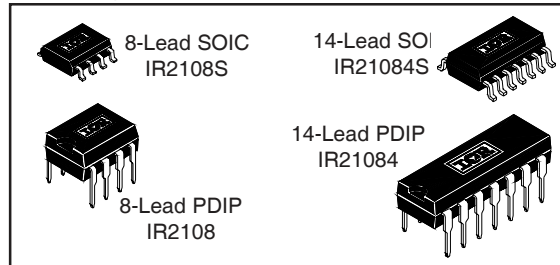
IR2108(4) (S) & (PbF)

HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation Fully operational to +600V Tolerant to negative transient voltage dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- High side output in phase with HIN input
- Low side output out of phase with LIN input
- Logic and power ground +/- 5V offset.
- Internal 540ns dead-time, and programmable up to 5us with one external R_{DT} resistor (IR21084)
- Lower di/dt gate driver for better noise immunity
- Available in Lead-Free

Packages



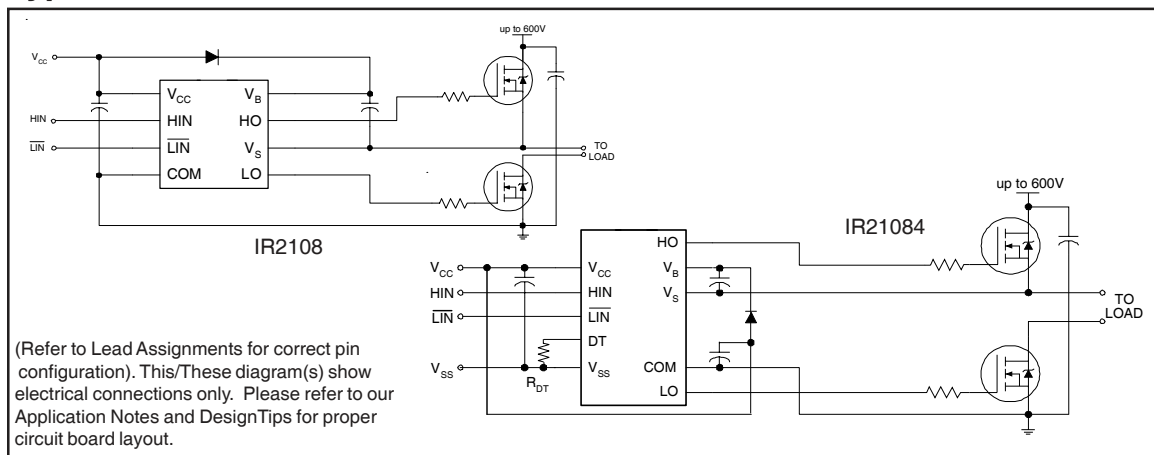
2106/2301//2108//2109/2302/2304 Feature Comparison

| Part | Input logic | Cross-conduction prevention logic | Dead-Time | Ground Pins |
|-----------|-------------|-----------------------------------|----------------|-------------|
| 2106/2301 | HIN/LIN | no | none | COM |
| 21064 | | | | VSS/COM |
| 2108 | HIN/LIN | yes | Internal 540ns | COM |
| 21084 | | | | VSS/COM |
| 2109/2302 | IN/SD | yes | Internal 540ns | COM |
| 21094 | | | | VSS/COM |
| 2304 | HIN/LIN | yes | Internal 100ns | COM |

Description

The IR2108(4)(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Typical Connection



IR2108(4) (S) & (PbF)

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | Min. | Max. | Units | |
|---------------------|--|-----------------------|-----------------------|-------|------|
| V _B | High side floating absolute voltage | -0.3 | 625 | V | |
| V _S | High side floating supply offset voltage | V _B - 25 | V _B + 0.3 | | |
| V _{HO} | High side floating output voltage | V _S - 0.3 | V _B + 0.3 | | |
| V _{CC} | Low side and logic fixed supply voltage | -0.3 | 25 | | |
| V _{LO} | Low side output voltage | -0.3 | V _{CC} + 0.3 | | |
| DT | Programmable dead-time pin voltage (IR21084 only) | V _{SS} - 0.3 | V _{CC} + 0.3 | | |
| V _{IN} | Logic input voltage (HIN & LIN) | V _{SS} - 0.3 | V _{CC} + 0.3 | | |
| V _{SS} | Logic ground (IR21084 only) | V _{CC} - 25 | V _{CC} + 0.3 | | |
| dV _S /dt | Allowable offset supply voltage transient | — | 50 | V/ns | |
| P _D | Package power dissipation @ T _A ≤ +25°C | (8 lead PDIP) | — | 1.0 | W |
| | | (8 lead SOIC) | — | 0.625 | |
| | | (14 lead PDIP) | — | 1.6 | |
| | | (14 lead SOIC) | — | 1.0 | |
| R _{thJA} | Thermal resistance, junction to ambient | (8 lead PDIP) | — | 125 | °C/W |
| | | (8 lead SOIC) | — | 200 | |
| | | (14 lead PDIP) | — | 75 | |
| | | (14 lead SOIC) | — | 120 | |
| T _J | Junction temperature | — | 150 | °C | |
| T _S | Storage temperature | -50 | 150 | | |
| T _L | Lead temperature (soldering, 10 seconds) | — | 300 | | |

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

| Symbol | Definition | Min. | Max. | Units | |
|-----------------|---|---------------------|---------------------|-------|-----------------|
| V _B | High side floating supply absolute voltage | V _S + 10 | V _S + 20 | V | |
| V _S | High side floating supply offset voltage | Note 1 | 600 | | |
| V _{HO} | High side floating output voltage | V _S | V _B | | |
| V _{CC} | Low side and logic fixed supply voltage | 10 | 20 | | |
| V _{LO} | Low side output voltage | 0 | V _{CC} | | |
| V _{IN} | Logic input voltage | IR2108 | COM | | V _{CC} |
| | | IR21084 | V _{SS} | | V _{CC} |
| DT | Programmable dead-time pin voltage (IR21084 only) | V _{SS} | V _{CC} | | |
| V _{SS} | Logic ground (IR21084 only) | -5 | 5 | °C | |
| T _A | Ambient temperature | -40 | 125 | | |

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C, DT = V_{SS} unless otherwise specified.

| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|------------------|--|------|------|------|-------|-----------------------------|
| t _{on} | Turn-on propagation delay | — | 220 | 300 | nsec | V _S = 0V |
| t _{off} | Turn-off propagation delay | — | 200 | 280 | | V _S = 0V or 600V |
| MT | Delay matching t _{on} - t _{off} | — | 0 | 30 | | |
| t _r | Turn-on rise time | — | 150 | 220 | nsec | V _S = 0V |
| t _f | Turn-off fall time | — | 50 | 80 | | V _S = 0V |
| DT | Deadtime: LO turn-off to HO turn-on(DT _{LO-HO}) & HO turn-off to LO turn-on (DT _{HO-LO}) | 400 | 540 | 680 | usec | RDT= 0 |
| | | 4 | 5 | 6 | | RDT = 200k (IR21084) |
| MDT | Deadtime matching = DT _{LO-HO} - DT _{HO-LO} | — | 0 | 60 | nsec | RDT=0 |
| | | — | 0 | 600 | | RDT = 200k (IR21084) |

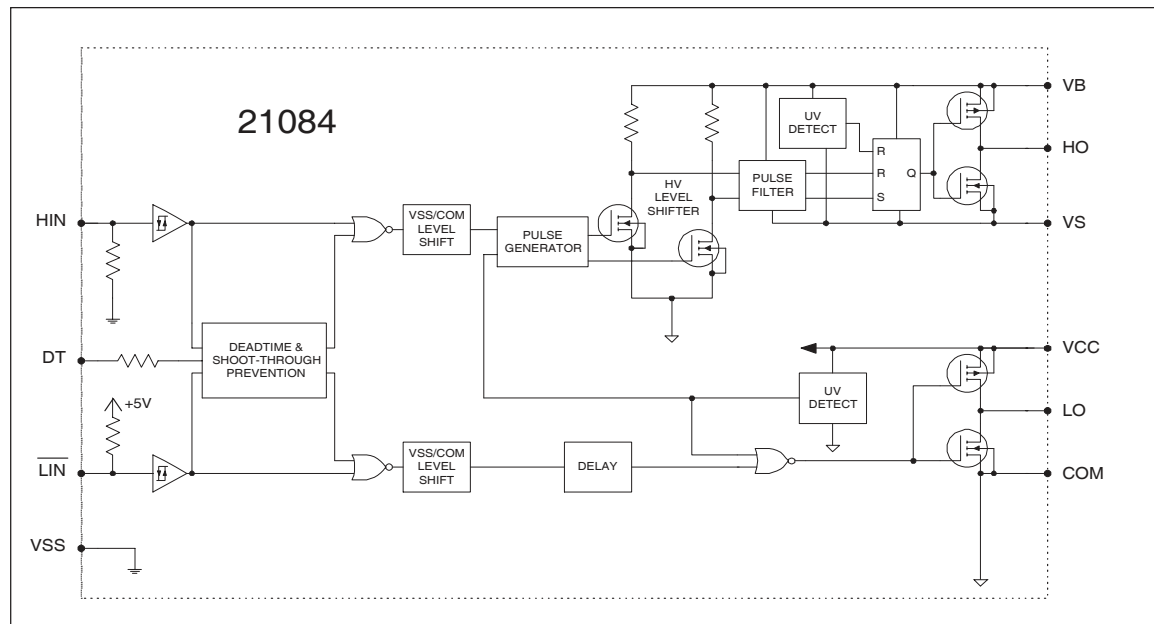
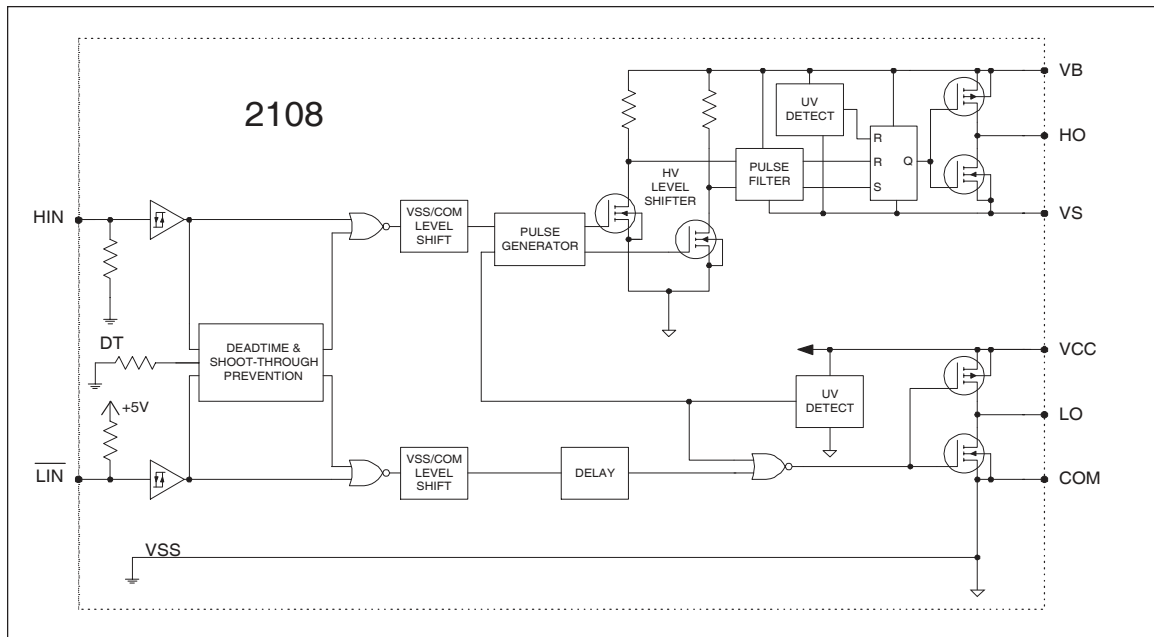
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, DT= V_{SS} and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads: H_{IN} and L_{IN}. The V_O, I_O and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|--|--|------|------|------|-------|--|
| V _{IH} | Logic "1" input voltage for H _{IN} & logic "0" for L _{IN} | 2.9 | — | — | V | V _{CC} = 10V to 20V |
| V _{IL} | Logic "0" input voltage for H _{IN} & logic "1" for L _{IN} | — | — | 0.8 | | V _{CC} = 10V to 20V |
| V _{OH} | High level output voltage, V _{BIAS} - V _O | — | 0.8 | 1.4 | | I _O = 20 mA |
| V _{OL} | Low level output voltage, V _O | — | 0.3 | 0.6 | μA | I _O = 20 mA |
| I _{LK} | Offset supply leakage current | — | — | 50 | | V _B = V _S = 600V |
| I _{QBS} | Quiescent V _{BS} supply current | 20 | 75 | 130 | mA | V _{IN} = 0V or 5V |
| I _{QCC} | Quiescent V _{CC} supply current | 0.4 | 1.0 | 1.6 | | RDT=0 |
| I _{IN+} | Logic "1" input bias current | — | 5 | 20 | μA | H _{IN} = 5V, L _{IN} = 0V |
| I _{IN-} | Logic "0" input bias current | — | — | 2 | | H _{IN} = 0V, L _{IN} = 5V |
| V _{CCUV+} V _{BSUV+} | V _{CC} and V _{BS} supply undervoltage positive going threshold | 8.0 | 8.9 | 9.8 | V | |
| V _{CCUV-} V _{BSUV-} | V _{CC} and V _{BS} supply undervoltage negative going threshold | 7.4 | 8.2 | 9.0 | | |
| V _{CCUVH} V _{BSUVH} | Hysteresis | 0.3 | 0.7 | — | | |
| I _{O+} | Output high short circuit pulsed current | 120 | 200 | — | mA | V _O = 0V, PW ≤ 10 μs |
| I _{O-} | Output low short circuit pulsed current | 250 | 350 | — | | V _O = 15V, PW ≤ 10 μs |

IR2108(4) (S) & (PbF)

Functional Block Diagram



Lead Definitions

| Symbol | Description |
|-----------------|---|
| HIN | Logic input for high side gate driver output (HO), in phase (referenced to COM for IR2108 and VSS for IR21084) |
| LIN | Logic input for low side gate driver output (LO), out of phase (referenced to COM for IR2108 and VSS for IR21084) |
| DT | Programmable dead-time lead, referenced to VSS. (IR21084 only) |
| VSS | Logic Ground (21084 only) |
| V _B | High side floating supply |
| HO | High side gate driver output |
| V _S | High side floating supply return |
| V _{CC} | Low side and logic fixed supply |
| LO | Low side gate driver output |
| COM | Low side return |

Lead Assignments

| | |
|--------------------|--------------------|
| <p>8 Lead PDIP</p> | <p>8 Lead SOIC</p> |
| IR2108 | IR2108S |

| | |
|---------------------|---------------------|
| <p>14 Lead PDIP</p> | <p>14 Lead SOIC</p> |
| IR21084 | IR21084S |

IR2108(4) (S) & (PbF)

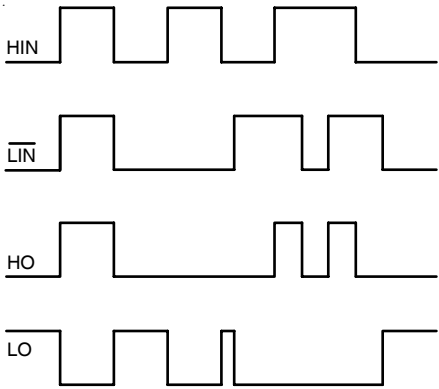


Figure 1. Input/Output Timing Diagram

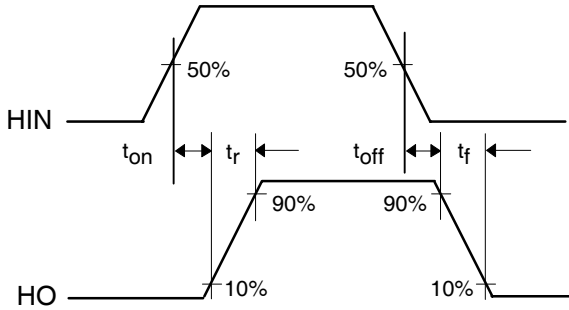
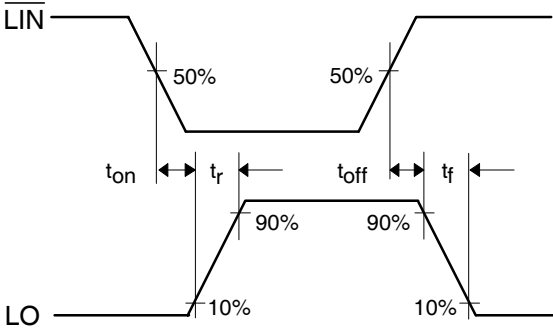


Figure 2. Switching Time Waveform Definitions

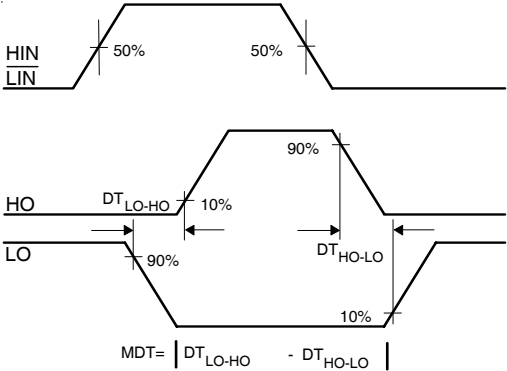


Figure 3. Deadtime Waveform Definitions

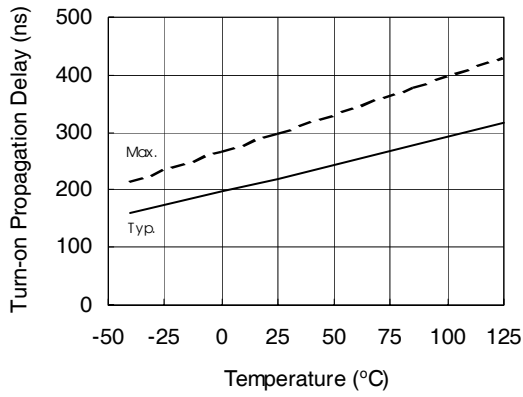


Figure 4A. Turn-on Propagation Delay vs. Temperature

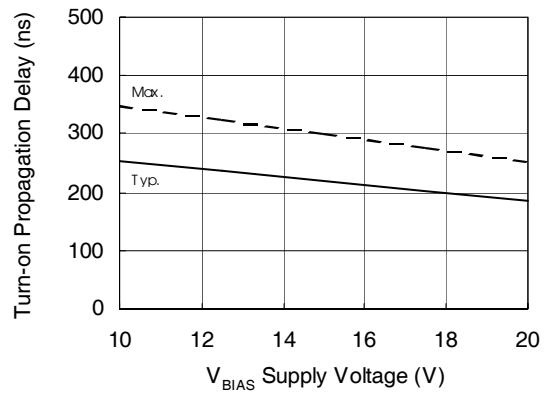


Figure 4B. Turn-on Propagation Delay vs. Supply Voltage

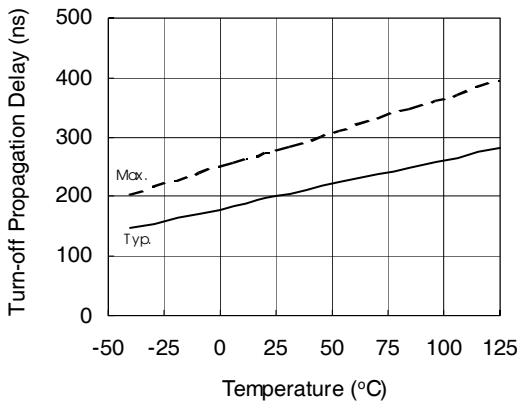


Figure 5A. Turn-off Propagation Delay vs. Temperature

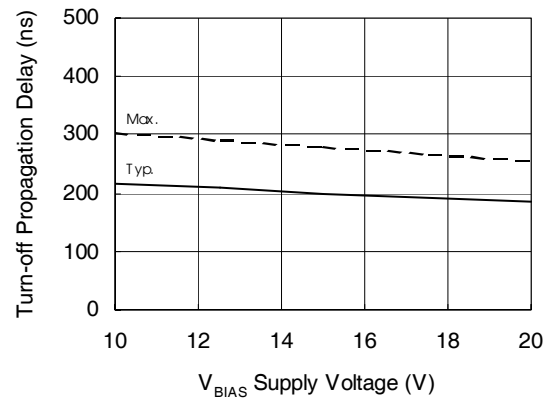


Figure 5B. Turn-off Propagation Delay vs. Supply Voltage

IR2108(4) (S) & (PbF)

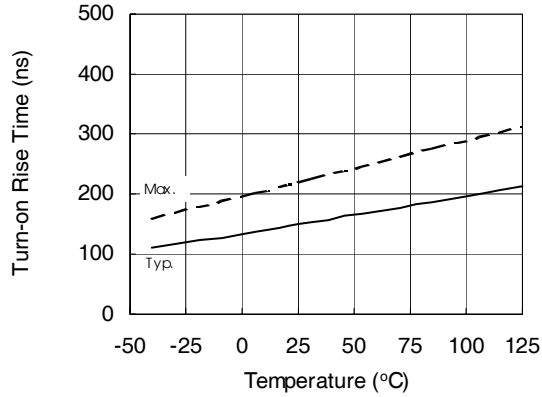


Figure 6A. Turn-on Rise Time vs. Temperature

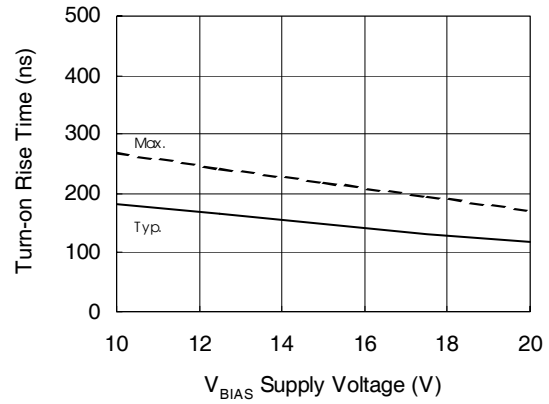


Figure 6B. Turn-on Rise Time vs. Supply Voltage

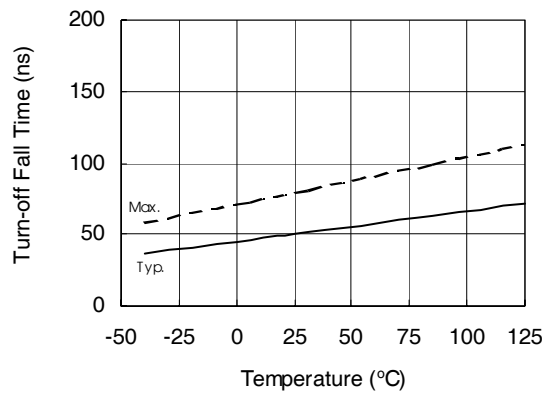


Figure 7A. Turn-off Fall Time vs. Temperature

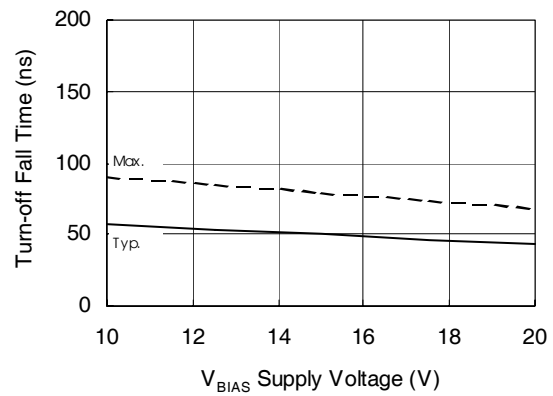


Figure 7B. Turn-off Fall Time vs. Supply Voltage

IR2108(4) (S) & (PbF)

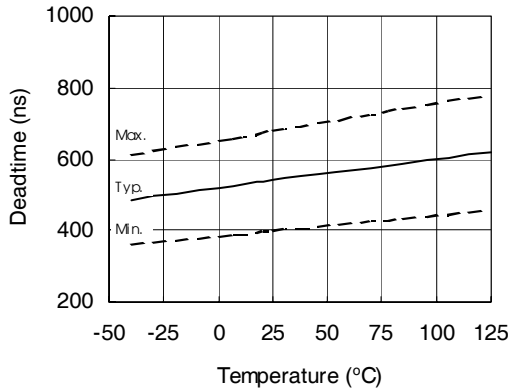


Figure 8A. Deadtime vs. Temperature

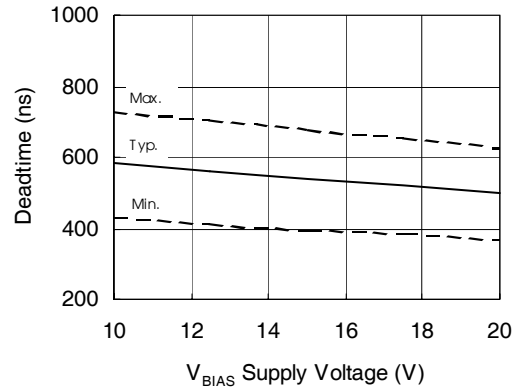


Figure 8B. Deadtime vs. Supply Voltage

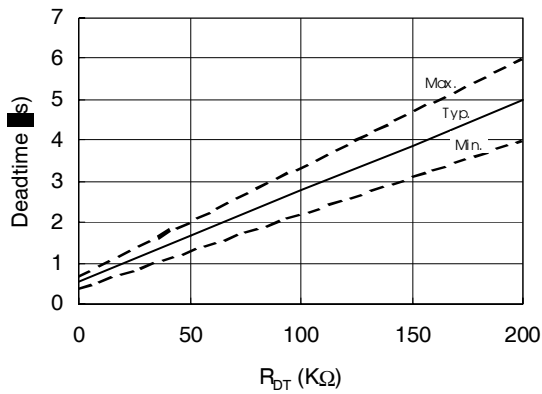


Figure 8C. Deadtime vs. R_{DT}
 (IR21084 Only)

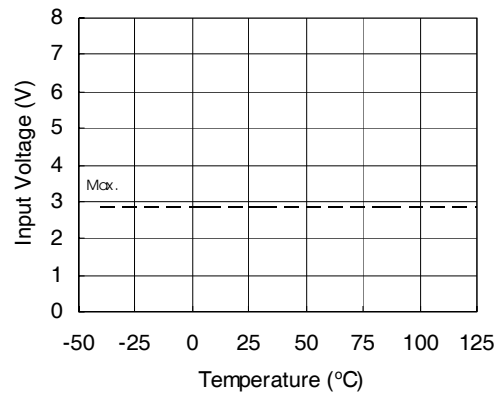


Figure 9A. Logic "1" Input Voltage
 vs. Temperature

IR2108(4) (S) & (PbF)

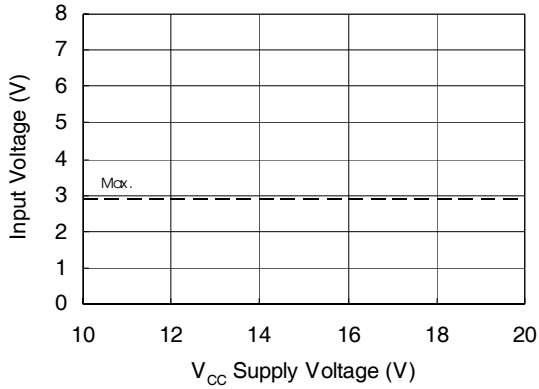


Figure 9B. Logic "1" Input Voltage vs. Supply Voltage

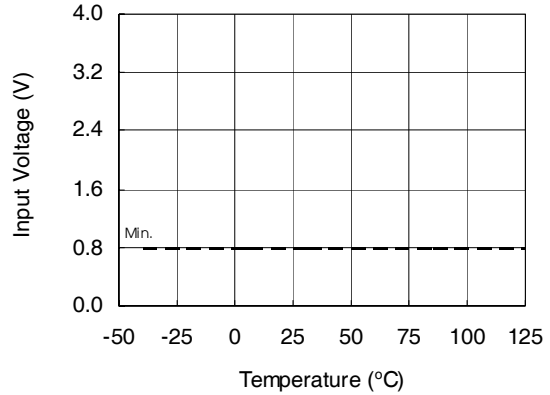


Figure 10A. Logic "0" Input Voltage vs. Temperature

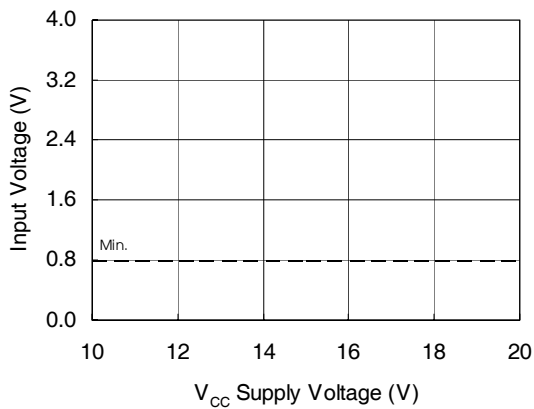


Figure 10B. Logic "0" Input Voltage vs. Supply Voltage

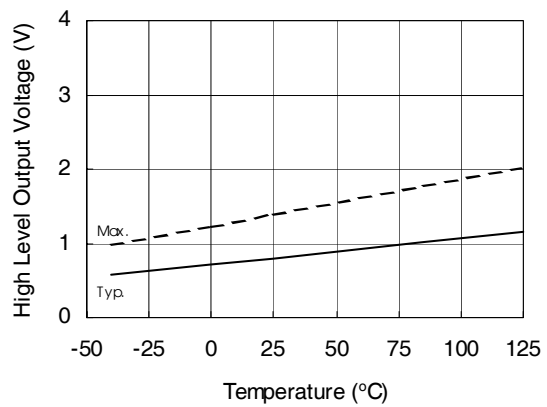


Figure 11A. High Level Output vs. Temperature

IR2108(4) (S) & (PbF)

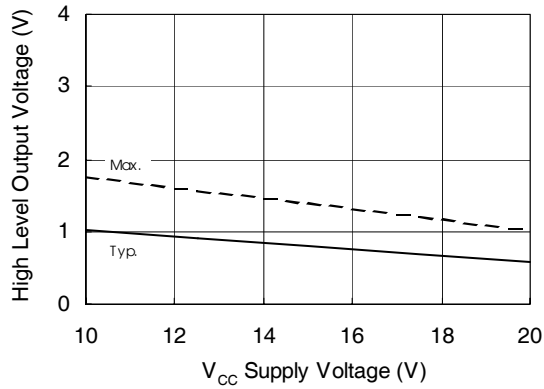


Figure 11B. High Level Output vs. Supply Voltage

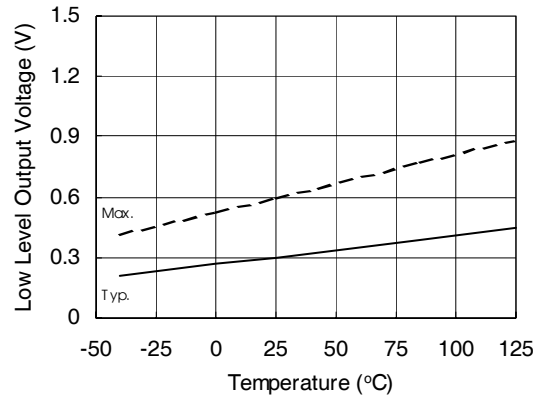


Figure 12A. Low Level Output vs. Temperature

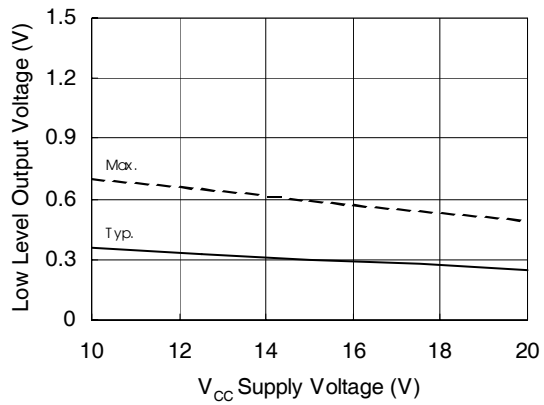


Figure 12B. Low Level Output vs. Supply Voltage

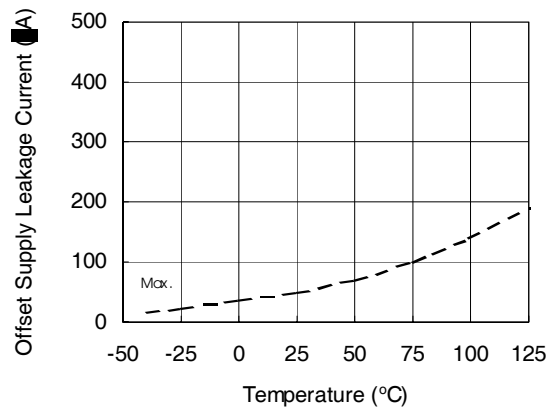


Figure 13A. Offset Supply Leakage Current vs. Temperature

IR2108(4) (S) & (PbF)

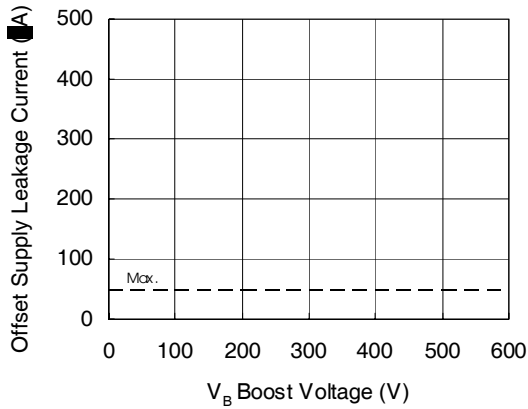


Figure 13B. Offset Supply Leakage Current vs. Temperature

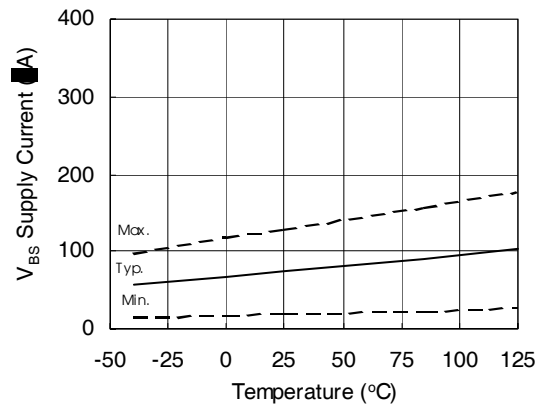


Figure 14A. V_{BS} Supply Current vs. Temperature

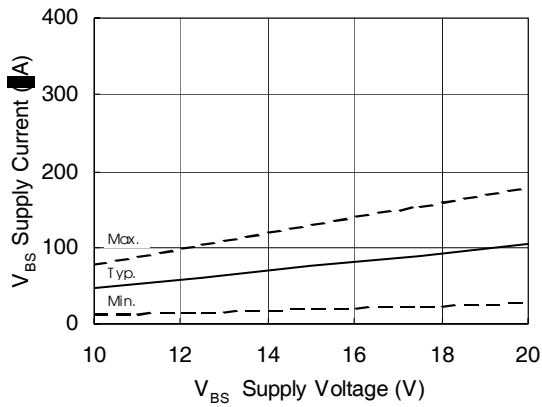


Figure 14B. V_{BS} Supply Current vs. Supply Voltage

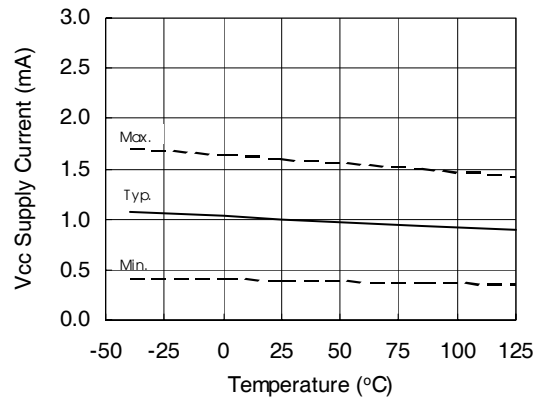


Figure 15A. V_{CC} Supply Current vs. Temperature

IR2108(4) (S) & (PbF)

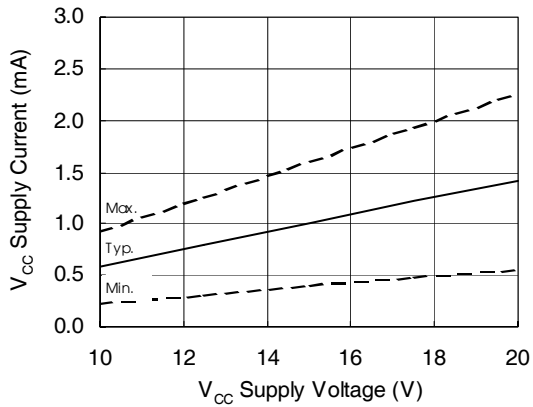


Figure 15B. V_{CC} Supply Current vs. Supply Voltage

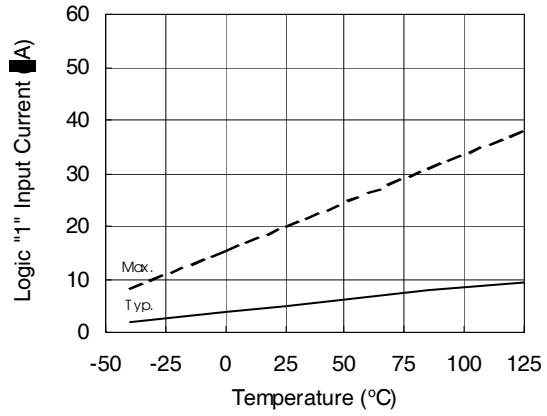


Figure 16A. Logic "1" Input Current vs. Temperature

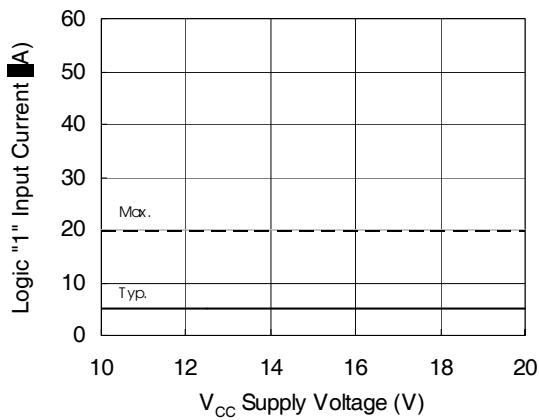


Figure 16B. Logic "1" Input Current vs. Supply Voltage

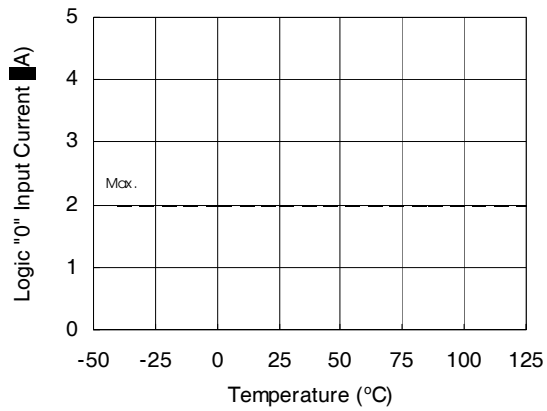


Figure 17A. Logic "0" Input Current vs. Temperature

IR2108(4) (S) & (PbF)

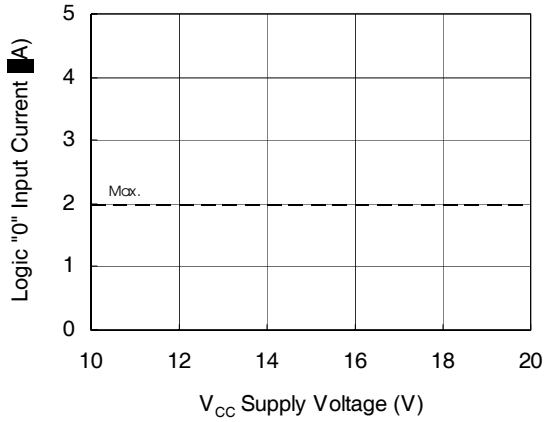


Figure 17B. Logic "0" Input Current vs. Supply Voltage

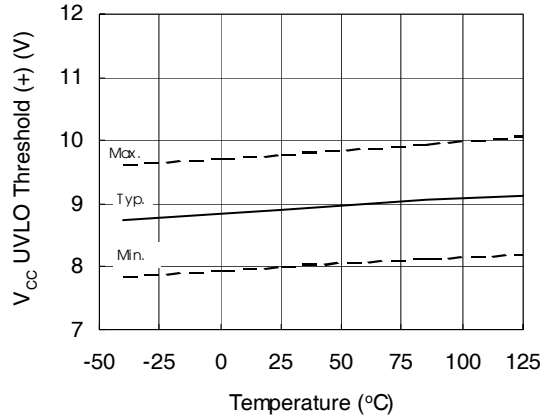


Figure 18. V_{CC} Undervoltage Threshold (+) vs. Temperature

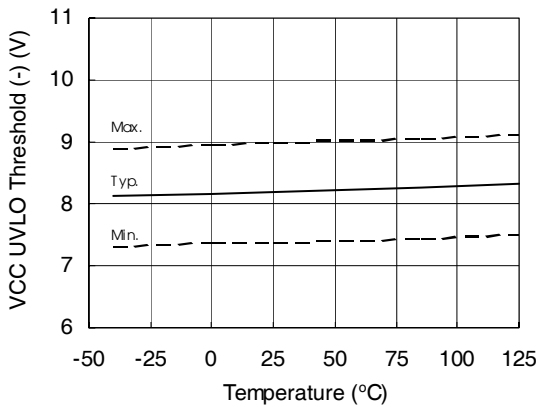


Figure 19. V_{CC} Undervoltage Threshold (-) vs. Temperature

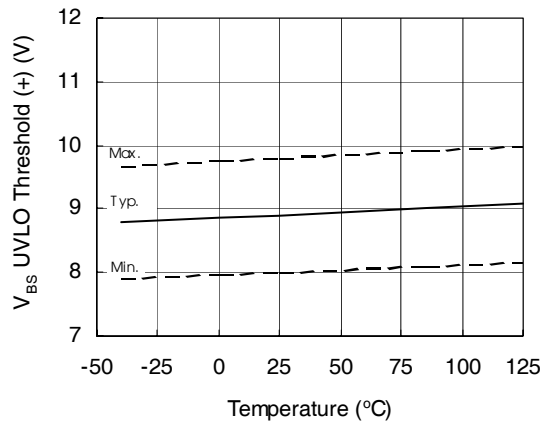


Figure 20. V_{BS} Undervoltage Threshold (+) vs. Temperature

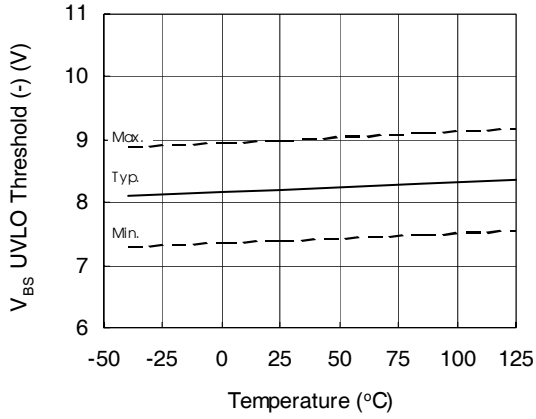


Figure 21. V_{BS} Undervoltage Threshold (-) vs. Temperature

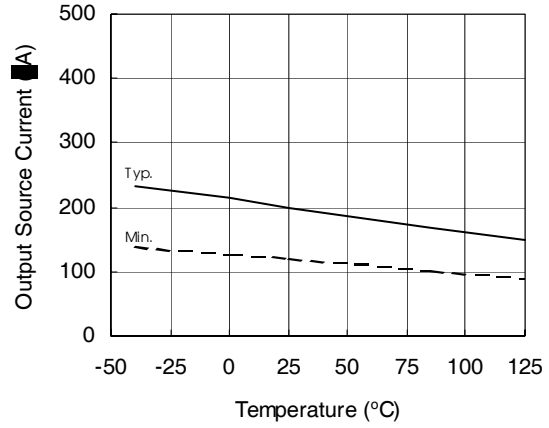


Figure 22A. Output Source Current vs. Temperature

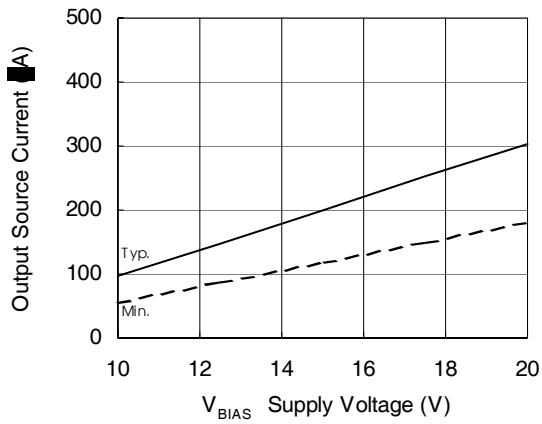


Figure 22B. Output Source Current vs. Supply Voltage

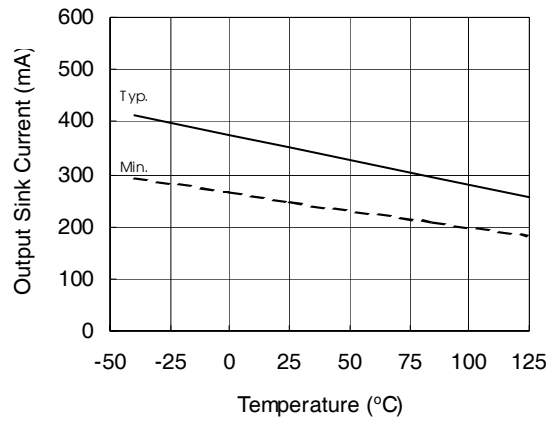


Figure 23A. Output Sink Current vs. Temperature

IR2108(4) (S) & (PbF)

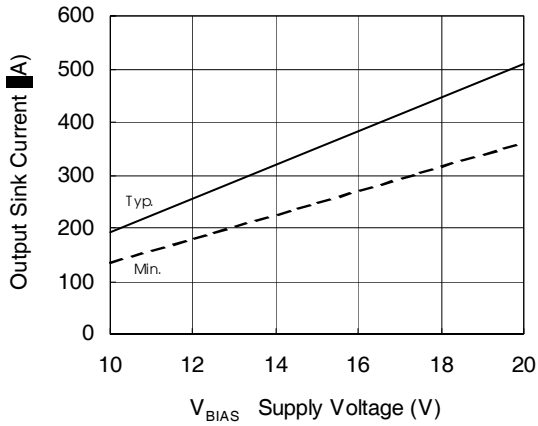


Figure 23B. Output Sink Current vs. Supply Voltage

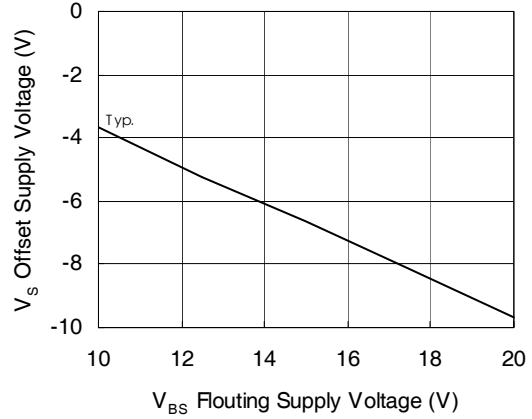
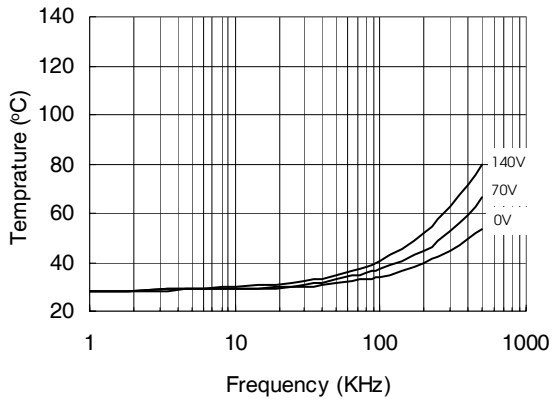
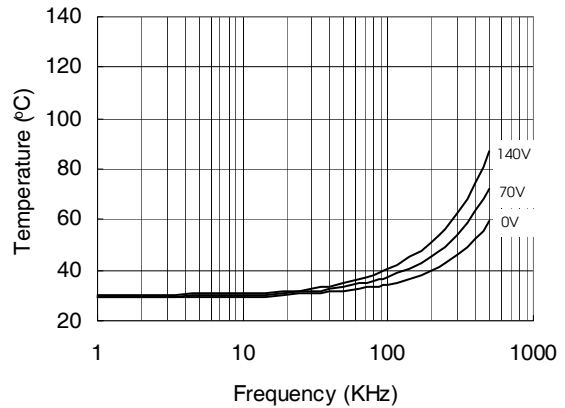


Figure 24. Maximum V_s Negative Offset vs. Supply Voltage

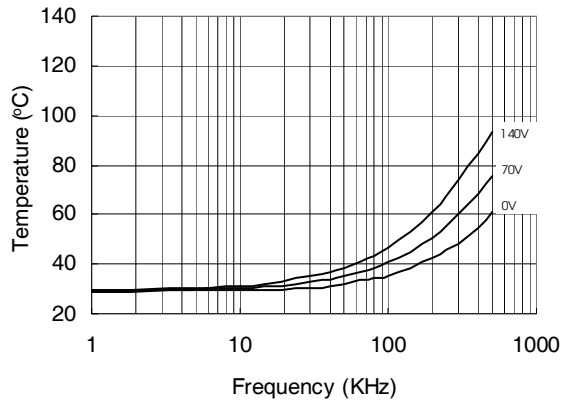


**Figure 25. IR2108 vs. Frequency (IRFBC20),
R_{gate}=33Ω, V_{CC}=15V**

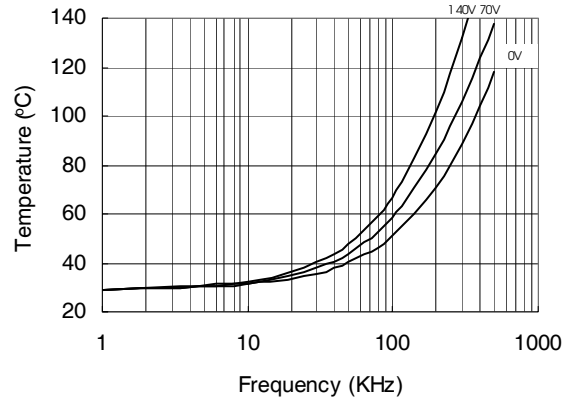


**Figure 26. IR2108 vs. Frequency (IRFBC30),
R_{gate}=22Ω, V_{CC}=15V**

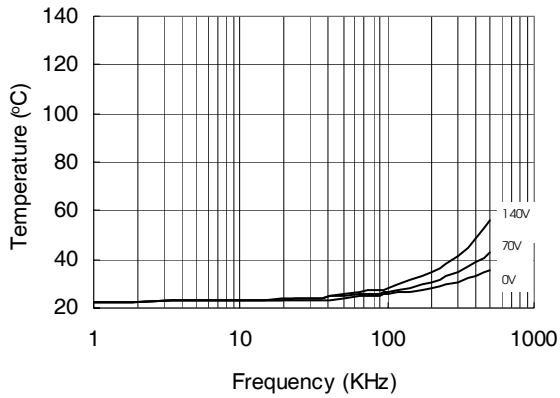
IR2108(4) (S) & (PbF)



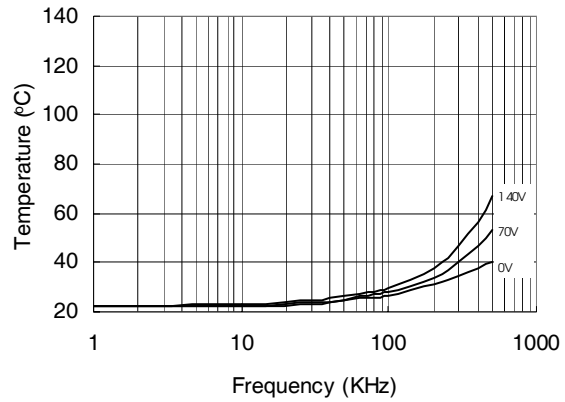
**Figure 27. IR2108 vs. Frequency (IRFBC40),
 $R_{gate}=15\Omega$, $V_{CC}=15V$**



**Figure 28. IR2108 vs. Frequency (IRFPE50),
 $R_{gate}=10\Omega$, $V_{CC}=15V$**



**Figure 29. IR21084 vs. Frequency (IRFBC20),
 $R_{gate}=33\Omega$, $V_{CC}=15V$**



**Figure 30. IR21084 vs. Frequency (IRFBC30),
 $R_{gate}=22\Omega$, $V_{CC}=15V$**

IR2108(4) (S) & (PbF)

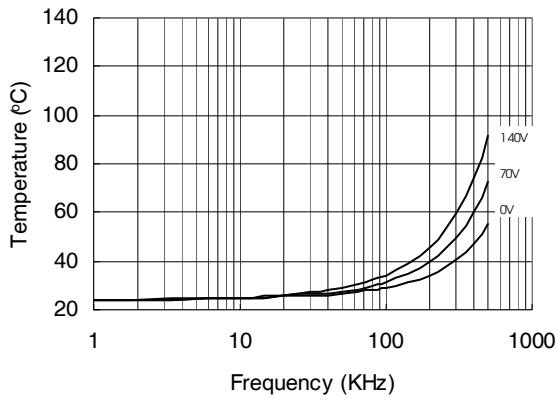


Figure 31. IR21084 vs. Frequency (IRFBC40),
 $R_{gate}=15\Omega$, $V_{CC}=15V$

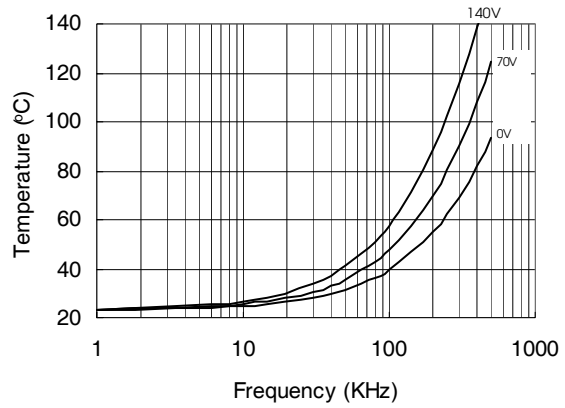


Figure 32. IR21084 vs. Frequency (IRFPE50),
 $R_{gate}=10\Omega$, $V_{CC}=15V$

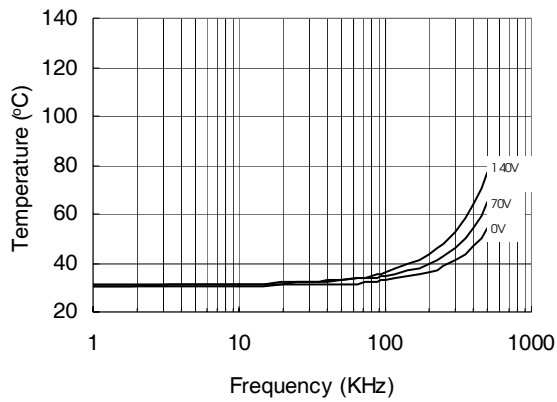


Figure 33. IR2108S vs. Frequency (IRFBC20),
 $R_{gate}=33\Omega$, $V_{CC}=15V$

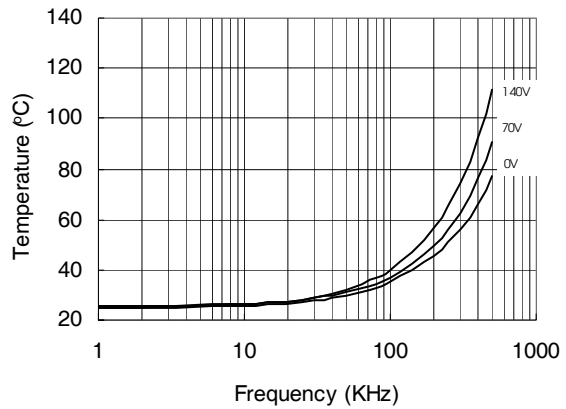
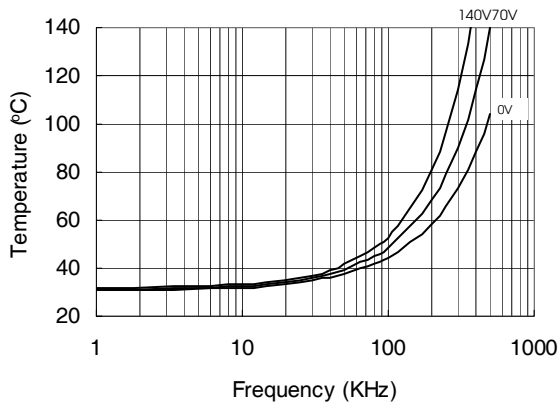
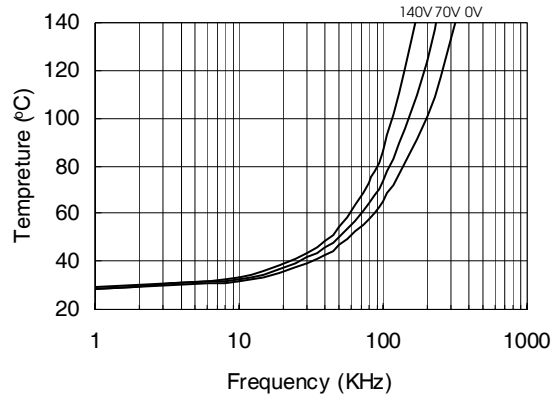


Figure 34. IR2108S vs. Frequency (IRFBC30),
 $R_{gate}=22\Omega$, $V_{CC}=15V$

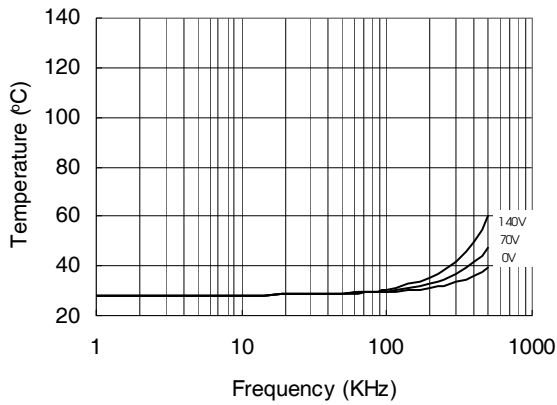
IR2108(4) (S) & (PbF)



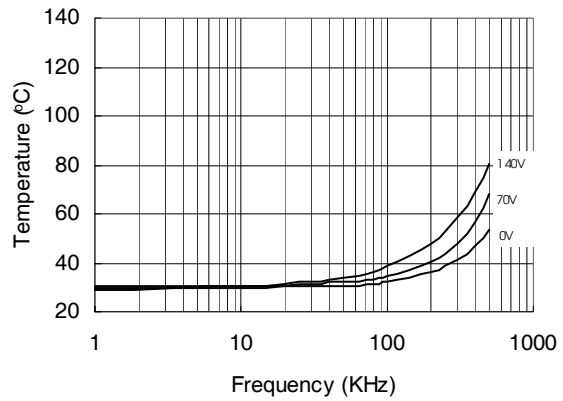
**Figure 35. IR2108S vs. Frequency (IRFBC40),
 $R_{gate}=15\Omega, V_{CC}=15V$**



**Figure 36. IR2108S vs. Frequency
(IRFPE50), $R_{gate}=10\Omega, V_{CC}=15V$**

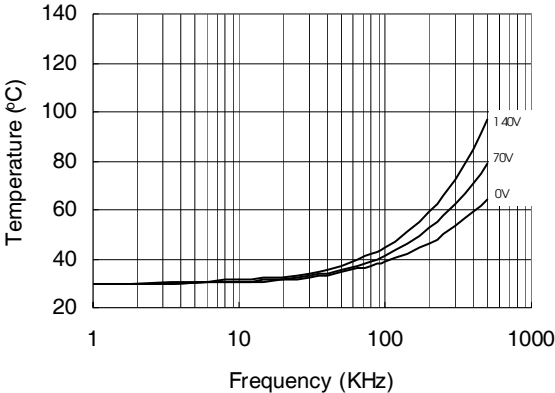


**Figure 37. IR21084S vs. Frequency (IRFBC20),
 $R_{gate}=33\Omega, V_{CC}=15V$**

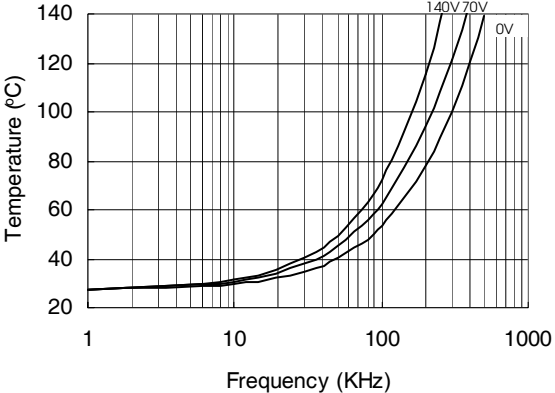


**Figure 38. IR21084S vs. Frequency (IRFBC30),
 $R_{gate}=22\Omega, V_{CC}=15V$**

IR2108(4) (S) & (PbF)

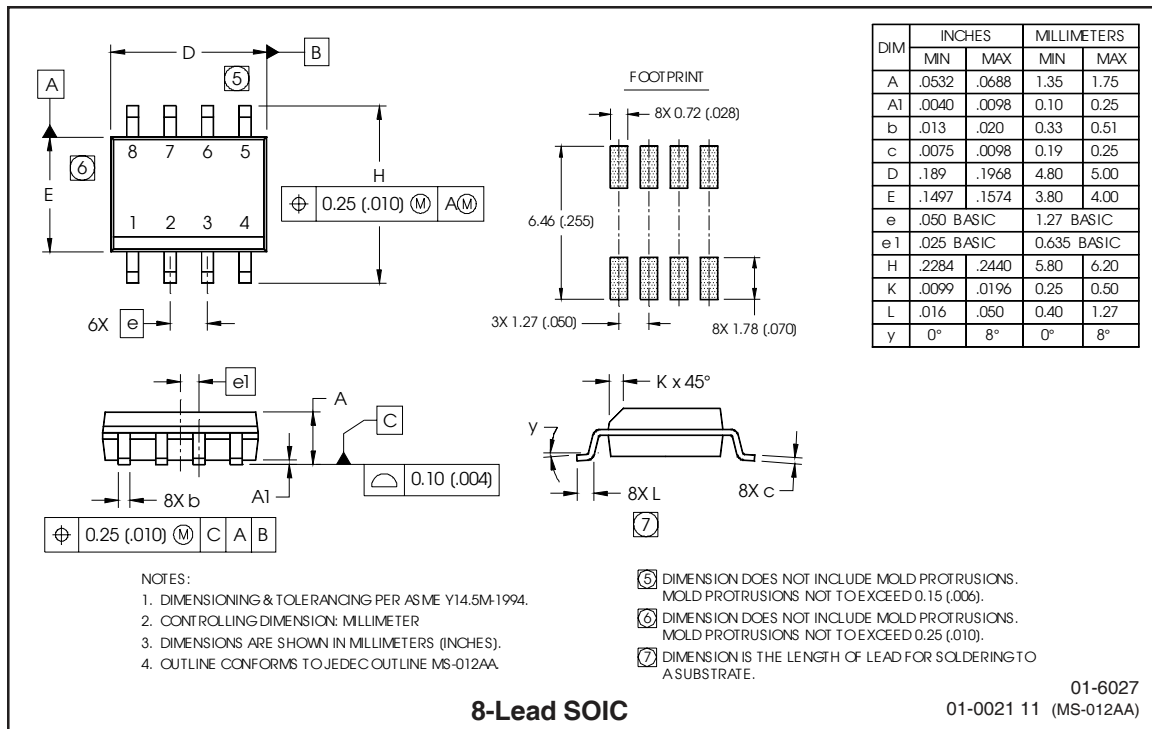
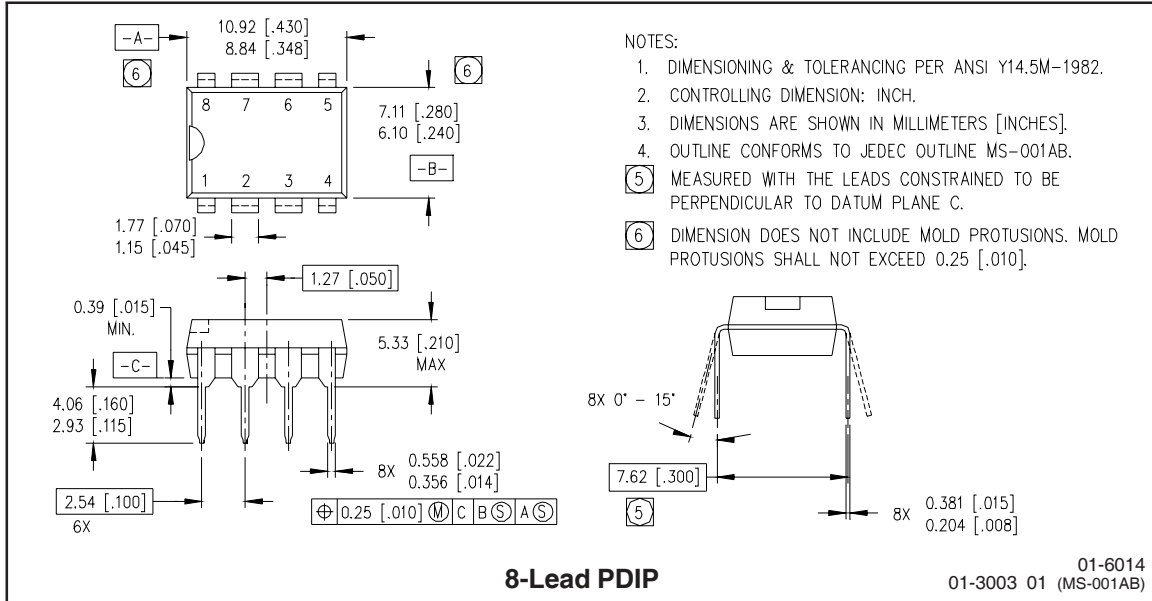


**Figure 39. IR21084S vs. Frequency (IRFBC40),
R_{gate}=15Ω, V_{cc}=15V**



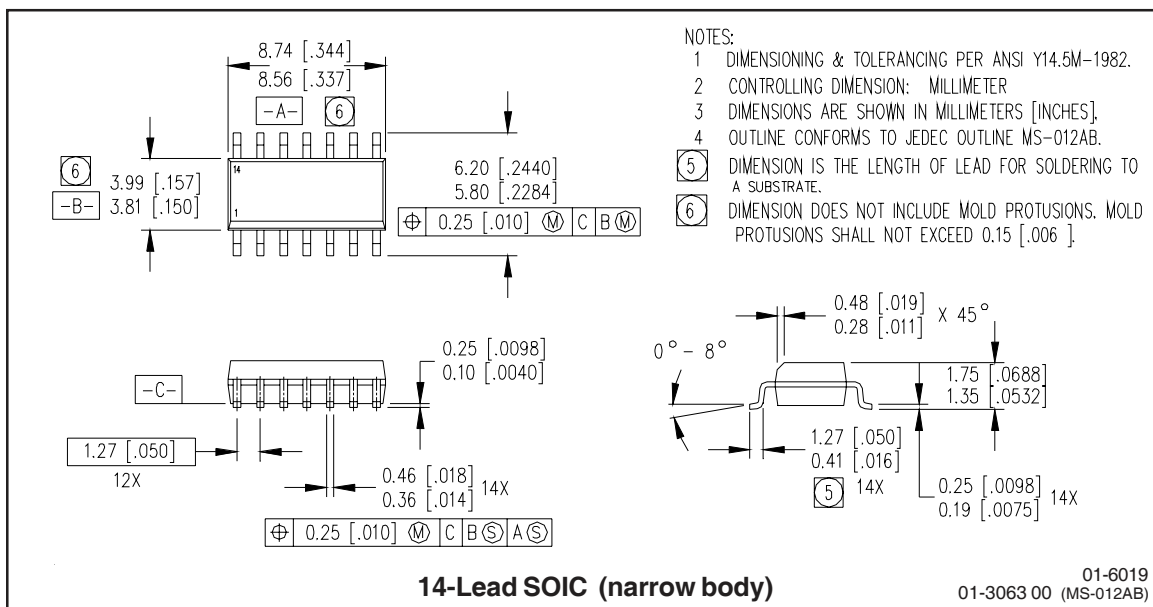
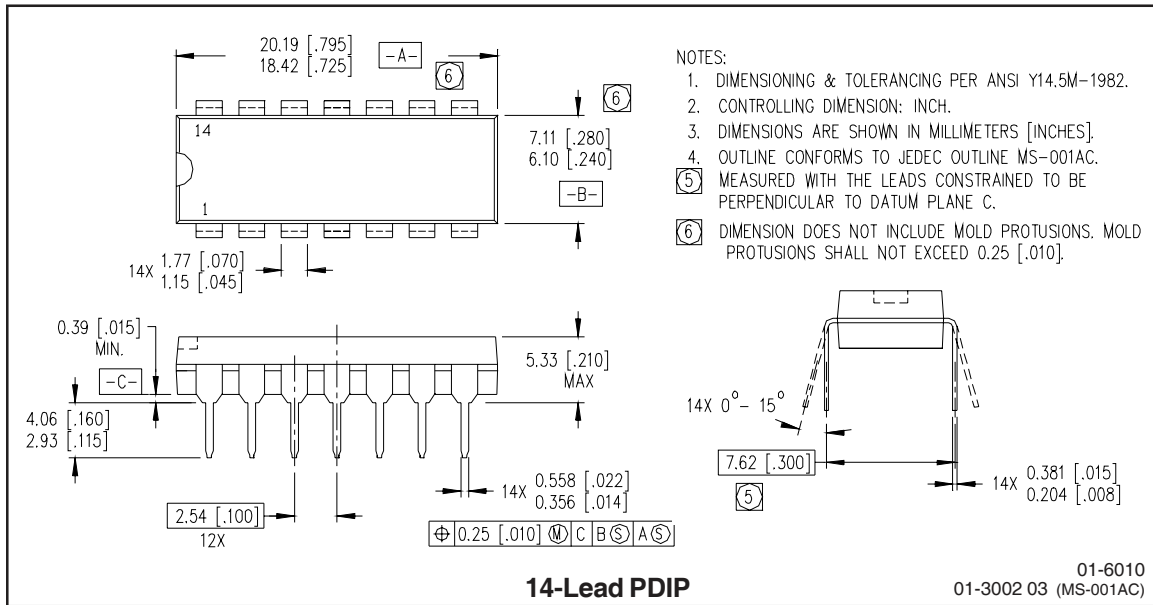
**Figure 40. IR21084S vs. Frequency (IRFPE50),
R_{gate}=10Ω, V_{cc}=15V**

Case outlines



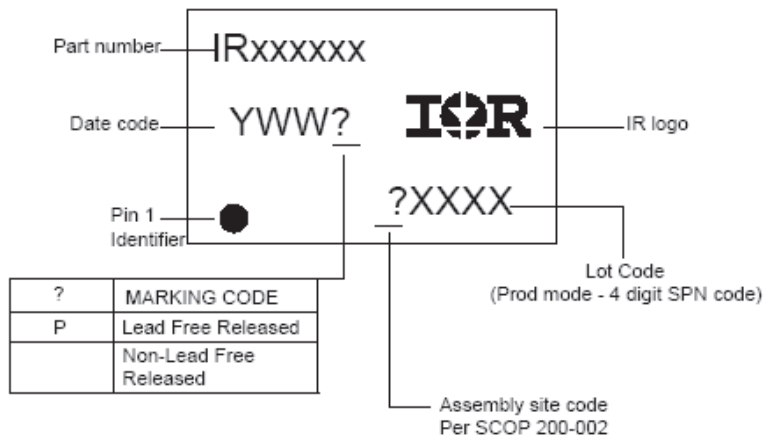
IR2108(4) (S) & (PbF)

International
IR Rectifier





LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)

8-Lead PDIP IR2108 order IR2108
 8-Lead SOIC IR2108S order IR2108S
 14-Lead PDIP IR21084 order IR21084
 14-Lead SOIC IR21084S order IR21084S

Lead-Free Part

8-Lead PDIP IR2108 order IR2108PbF
 8-Lead SOIC IR2108S order IR2108SPbF
 14-Lead PDIP IR21084 order IR21084PbF
 14-Lead SOIC IR21084S order IR21084SPbF