

16-bit Single Chip Microcontroller

- Low voltage operation from 1.2 V with a single alkaline or silver oxide button battery.
- Ultra low standby power consumption (0.3 μ A during HALT state in super economy mode)
- Embedded A/D converter to support various sensing applications

DESCRIPTIONS

The S1C17W18 is a 16-bit MCU that features low-voltage operation from 1.2 V even though Flash memory is included. The embedded high-efficiency DC-DC converter generates the constant-voltage to drive the IC with lower power consumption than 4-bit MCUs. This IC includes a real-time clock, a stopwatch, an LCD driver, a temperature sensor, an A/D converter, and a PWM timer capable of being used to generate drive waveforms for a motor driver as well as a high-performance 16-bit CPU. It is suitable for battery-driven applications that require an LCD display and a temperature measurement function.

FEATURES

Model	S1C17W18
CPU	
CPU core	Seiko Epson original 16-bit RISC CPU core S1C17
Other	On-chip debugger
Embedded Flash memory	
Capacity	128K bytes (for both instructions and data)
Erase/program count	1,000 times (min.) * Programming by the debugging tool ICDmini
Other	Security function to protect from reading/programming by ICDmini On-board programming function using ICDmini Flash programming voltage can be generated internally.
Embedded RAM	
Capacity	8K bytes
Embedded display RAM	
Capacity	96 bytes
Clock generator (CLG)	
System clock source	4 sources (IOSC/OSC1/OSC3/EXOSC)
System clock frequency (operating frequency)	1.1 MHz (max.) $V_{DD} = 1.2$ to 1.6 V 4.2 MHz (max.) $V_{DD} = 1.6$ to 3.6 V
IOSC oscillator circuit (boot clock source)	700 kHz (typ.) embedded oscillator 23 μ s (max.) starting time (time from cancelation of SLEEP state to vector table read by the CPU)
OSC1 oscillator circuit	32.768 kHz (typ.) crystal oscillator Oscillation stop detection circuit included
OSC3 oscillator circuit	4.2 MHz (max.) crystal/ceramic oscillator 250, 384, 500 kHz, 1, 2, and 4 MHz-switchable embedded oscillator 2.1 MHz (max.) CR oscillator (an external R is required)
EXOSC clock input	4.2 MHz (max.) square or sine wave input
Other	Configurable system clock division ratio Configurable system clock used at wake up from SLEEP state Operating clock frequency for the CPU and all peripheral circuits is selectable.
I/O port (PPORT)	
Number of general-purpose I/O ports	Input/output port: 67 bits (max., 128-pin package or chip) 56 bits (max., 80-pin package) 48 bits (max., 64-pin package) Output port: 1 bit (max.) Pins are shared with the peripheral I/O.
Number of input interrupt ports	63 bits (max., 128-pin package or chip) 52 bits (max., 80-pin package) 44 bits (max., 64-pin package)
Number of ports that support universal port multiplexer (UPMUX)	32 bits (max., 128-pin package or chip) 29 bits (max., 80-pin package) 24 bits (max., 64-pin package) A peripheral circuit I/O function selected via software can be assigned to each port.
Timers	
Watchdog timer (WDT)	Generates NMI or watchdog timer reset.
Real-time clock (RTCA)	128-1 Hz counter, second/minute/hour/day/day of the week/month/year counters Theoretical regulation function for 1-second correction Alarm and stopwatch functions
16-bit timer (T16)	4 channels Generates the SPIA master clocks and the ADC12A operating clock/trigger signal.

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Model	S1C17W18
Timers	
16-bit PWM timer (T16B)	3 channels Event counter/capture function PWM waveform generation function Number of PWM output or capture input ports: 2 ports/channel
Supply voltage detector (SVD)	
Detection level	30 levels (1.2 to 3.6 V)
Other	Intermittent operation mode Generates an interrupt or reset according to the detection level evaluation.
Serial interfaces	
UART (UART)	2 channels Baud-rate generator included, IrDA1.0 supported
Synchronous serial interface (SPIA)	2 channels 2 to 16-bit variable data length The 16-bit timer (T16) can be used for the baud-rate generator in master mode.
I ² C (I2C) *1	1 channel Baud-rate generator included
Sound generator (SNDA)	
Buzzer output function	512 Hz to 16 kHz output frequencies One-shot output function
Melody generation function	Pitch: 128 Hz to 16 kHz ≈ C3 to C6 Duration: 7 notes/rests (Half note/rest to thirty-second note/rest) Tempo: 16 tempos (30 to 480) Tie/slur may be specified.
IR remote controller (REMC2)	
Number of transmitter channels	1 channel
Other	EL lamp drive waveform can be generated for an application example.
LCD driver (LCD8B)	
LCD output	44 SEG × 5–8 COM (max.), 48 SEG × 1–4 COM (max.) (128-pin package or chip) 28 SEG × 5–8 COM (max.), 32 SEG × 1–4 COM (max.) (80-pin package) 20 SEG × 5–8 COM (max.), 24 SEG × 1–4 COM (max.) (64-pin package)
LCD contrast	32 levels
Other	1/4 or 1/3 bias power supply included, external voltage can be applied.
R/F converter (RFC)	
Conversion method	CR oscillation type with 24-bit counters
Number of conversion channels	2 channels (Up to two sensors can be connected to each channel.)
Supported sensors	DC-bias resistive sensors, AC-bias resistive sensors (Ch.0 only)
12-bit A/D converter (ADC12A)	
Conversion method	Successive approximation type
Resolution	12 bits
Number of conversion channels	1 channel
Number of analog signal inputs	8 ports/channel (The temperature sensor output is connected to a port.)
Temperature sensor/reference voltage generator (TSRVR)	
Temperature sensor circuit	Sensor output can be measured using ADC12A.
Reference voltage generator	Reference voltage for ADC12A is selectable from 2.0 V, 2.5 V, V _{DD} , and external input.
Multiplier/divider (COPRO2)	
Arithmetic functions	16-bit × 16-bit multiplier 16-bit × 16-bit + 32-bit multiply and accumulation unit 32-bit ÷ 32-bit divider
Reset	
#RESET pin	Reset when the reset pin is set to low.
Power-on reset	Reset at power on.
Key entry reset	Reset when the P00 to P01/P02/P03 keys are pressed simultaneously (can be enabled/disabled using a register).
Watchdog timer reset	Reset when the watchdog timer overflows (can be enabled/disabled using a register).
Supply voltage detector reset	Reset when the supply voltage detector detects the set voltage level (can be enabled/disabled using a register).
Interrupt	
Non-maskable interrupt	4 systems (Reset, address misaligned interrupt, debug, NMI)
Programmable interrupt	External interrupt: 1 system (8 levels) Internal interrupt: 22 systems (8 levels)
Power supply voltage	
V _{DD} operating voltage	1.2 to 3.6 V
V _{DD} operating voltage for Flash programming	2.4 to 3.6 V (V _{PP} = 7.5 V external power supply is required.) 2.4 to 3.6 V (When V _{PP} is generated internally)
V _{DD} operating voltage for super economy mode	2.5 to 3.6 V (128-pin package or chip)
Operating temperature	
Operating temperature range	-40 to 85 °C

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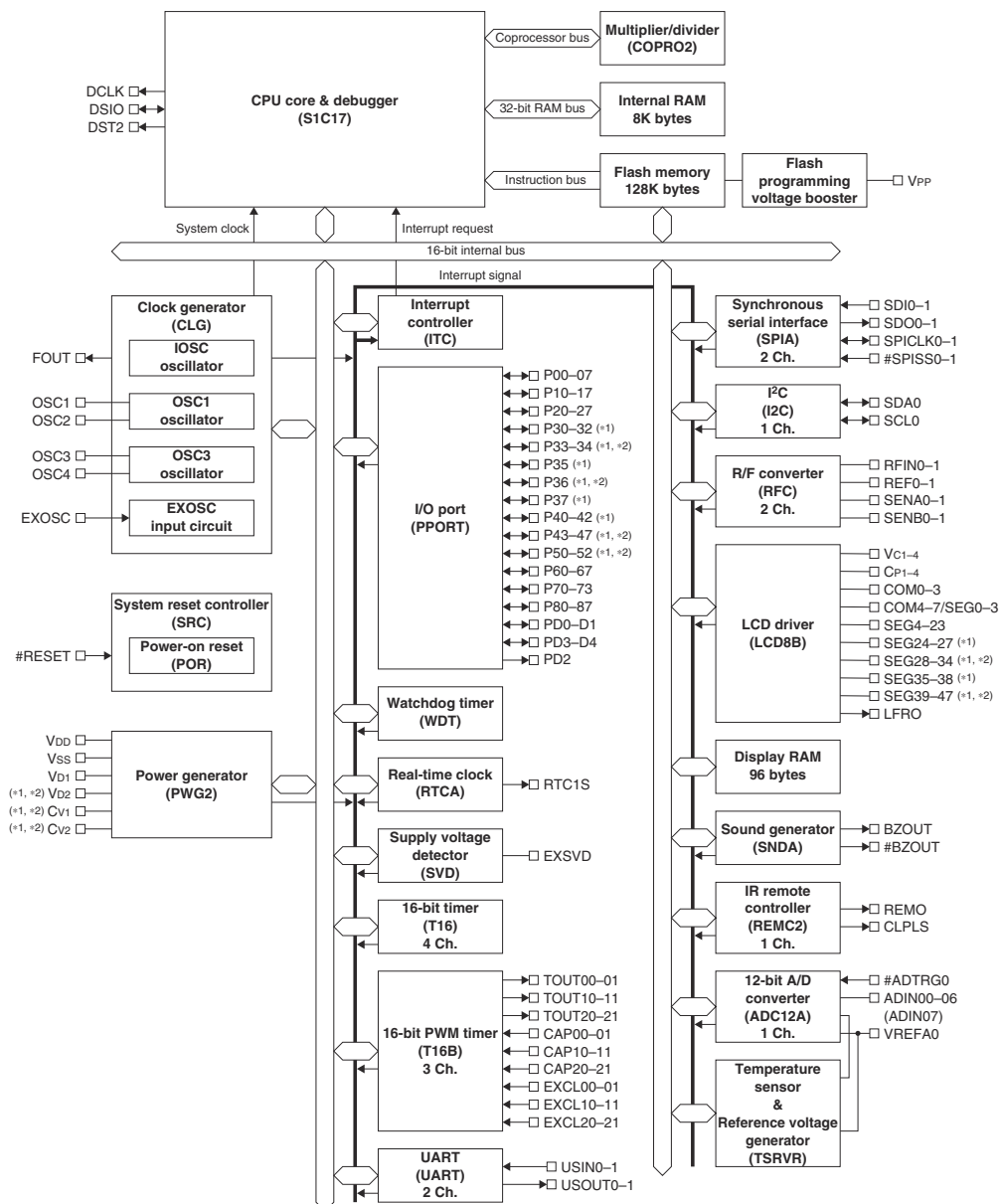
Model	S1C17W18
Current consumption (Typ. value)	
SLEEP mode *2	0.15 μ A IOSC = OFF, OSC1 = OFF, OSC3 = OFF
HALT mode	0.5 μ A OSC1 = 32 kHz, RTC = ON 0.3 μ A (128-pin package or chip) OSC1 = 32 kHz, RTC = ON, super economy mode
RUN mode	4 μ A OSC1 = 32 kHz, RTC = ON, CPU = OSC1 2 μ A (128-pin package or chip) OSC1 = 32 kHz, RTC = ON, CPU = OSC1, super economy mode 140 μ A OSC3 = 1 MHz (ceramic oscillator), OSC1 = 32 kHz, RTC = ON, CPU = OSC3
Shipping form	
1 *3	SQFN9-64PIN (P-VQFN064-0909-0.50, 9 x 9 mm, t = 1 mm, 0.5 mm pitch)
2 *3	TQFP14-80PIN (P-TQFP080-1212-0.50, 12 x 12 mm, t = 1.2 mm, 0.5 mm pitch)
3 *3	TQFP15-128PIN (P-TQFP128-1414-0.40, 14 x 14 mm, t = 1.2 mm, 0.4 mm pitch)
4	Die form (Pad pitch: 80 μ m (min.))

*1 The input filter in I2C (SDA and SCL inputs) does not comply with the standard for removing noise spikes less than 50 ns.

*2 The RAM retains data even in SLEEP mode.

*3 Shown in parentheses are JEITA package names.

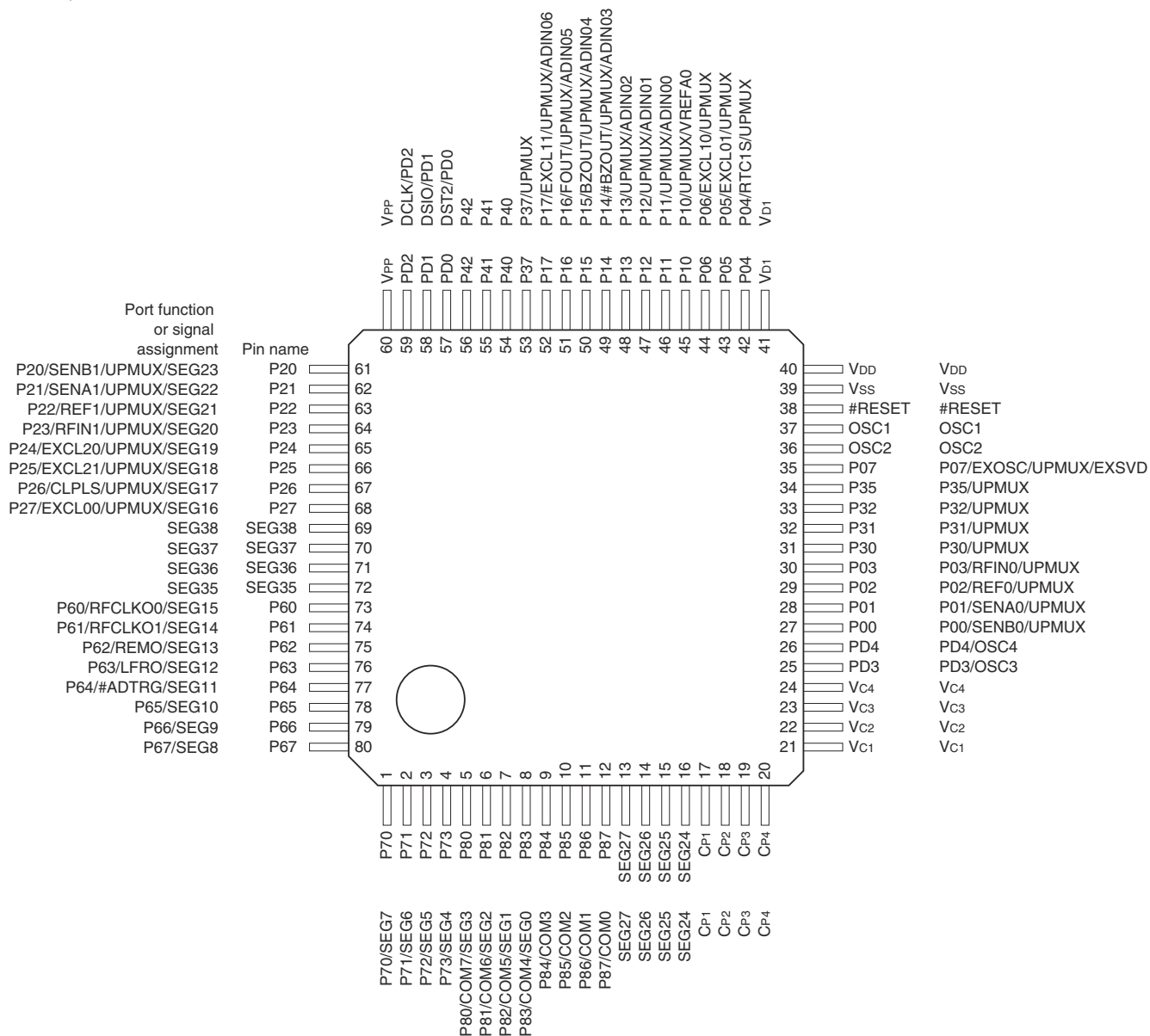
■ BLOCK DIAGRAM



*1 These pins do not exist in the 64-pin package.

*2 These pins do not exist in the 80-pin package.

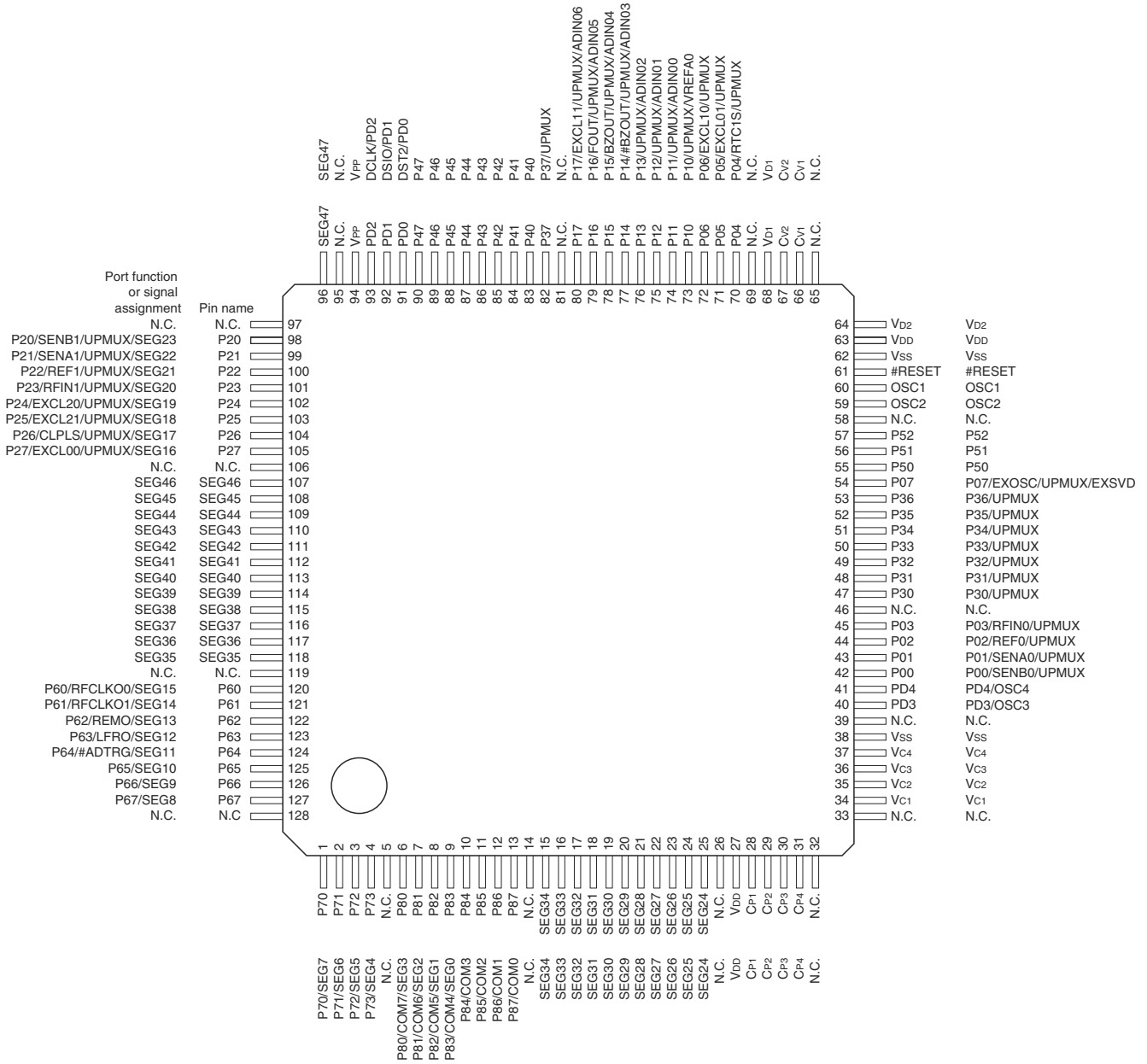
TQFP14-80PIN



Note: The model in this package cannot be placed into super economy mode, as it does not have the V_{D2}, C_{V1}, and C_{V2} pins.

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TQFP15-128PIN



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■ PIN DESCRIPTIONS

Symbol meanings

Assigned signal: The signal listed at the top of each pin is assigned in the initial state. The pin function must be switched via software to assign another signal (see the “I/O Ports” chapter).

I/O: I = Input
 O = Output
 I/O = Input/output
 P = Power supply
 A = Analog signal
 Hi-Z = High impedance state

Initial state: I (Pull-up) = Input with pulled up
 I (Pull-down) = Input with pulled down
 Hi-Z = High impedance state
 O (H) = High level output
 O (L) = Low level output

Tolerant fail-safe structure:

✓

= Over voltage tolerant fail-safe type I/O cell included (see the “I/O Ports” chapter)

The over voltage tolerant fail-safe type I/O cell allows interfacing without passing unnecessary current even if a voltage exceeding V_{DD} is applied to the port. Also unnecessary current is not consumed when the port is externally biased without supplying V_{DD} .

Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function	128pin/chip	80pin	64pin
V _{DD}	V _{DD}	P	–	–	Power supply (+)	✓	✓	✓
V _{SS}	V _{SS}	P	–	–	GND	✓	✓	✓
V _{PP}	V _{PP}	P	–	–	Power supply for Flash programming	✓	✓	✓
V _{D1}	V _{D1}	A	–	–	DC-DC converter output	✓	✓	✓
V _{D2}	V _{D2}	A	–	–	DC-DC converter stabilization capacitor connect pin	✓	–	–
C _{V1-2}	C _{V1-2}	A	–	–	DC-DC converter charge pump capacitor connect pins	✓	–	–
V _{C1-4}	V _{C1-4}	P	–	–	LCD panel driver power supply	✓	✓	✓
C _{P1-4}	C _{P1-4}	A	–	–	LCD power supply booster capacitor connect pins	✓	✓	✓
OSC1	OSC1	A	–	–	OSC1 oscillator circuit input	✓	✓	✓
OSC2	OSC2	A	–	–	OSC1 oscillator circuit output	✓	✓	✓
#RESET	#RESET	I	I (Pull-up)	–	Reset input	✓	✓	✓
P00	P00	I/O	Hi-Z	–	I/O port	✓	✓	✓
	SENB0	A			R/F converter Ch.0 sensor B oscillator pin	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
P01	P01	I/O	Hi-Z	–	I/O port	✓	✓	✓
	SENA0	A			R/F converter Ch.0 sensor A oscillator pin	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
P02	P02	I/O	Hi-Z	–	I/O port	✓	✓	✓
	REF0	A			R/F converter Ch.0 reference oscillator pin	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
P03	P03	I/O	Hi-Z	–	I/O port	✓	✓	✓
	RFIN0	A			R/F converter Ch.0 oscillation input	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
P04	P04	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	RTC1S	O			Real-time clock 1-second cycle pulse output	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
P05	P05	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	EXCL01	I			16-bit PWM timer Ch.0 event counter input 1	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
P06	P06	I/O	Hi-Z	–	I/O port	✓	✓	✓
	EXCL10	I			16-bit PWM timer Ch.1 event counter input 0	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
P07	P07	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	EXOSC	I			Clock generator external clock input	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
	EXSVD	A			External power supply voltage detection input	✓	✓	✓

Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function	128pin/chip	80pin	64pin
P10	P10	I/O	Hi-Z	-	I/O port	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
	VREFA0	A			12-bit A/D converter Ch.0 reference voltage input	✓	✓	✓
P11	P11	I/O	Hi-Z	-	I/O port	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
	ADIN00	A			12-bit A/D converter Ch.0 analog signal input 0	✓	✓	✓
P12	P12	I/O	Hi-Z	-	I/O port	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
	ADIN01	A			12-bit A/D converter Ch.0 analog signal input 1	✓	✓	✓
P13	P13	I/O	Hi-Z	-	I/O port	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
	ADIN02	A			12-bit A/D converter Ch.0 analog signal input 2	✓	✓	✓
P14	P14	I/O	Hi-Z	-	I/O port	✓	✓	✓
	#BZOUT	O			Sound generator inverted output	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
	ADIN03	A			12-bit A/D converter Ch.0 analog signal input 3	✓	✓	✓
P15	P15	I/O	Hi-Z	-	I/O port	✓	✓	✓
	BZOUT	O			Sound generator output	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
	ADIN04	A			12-bit A/D converter Ch.0 analog signal input 4	✓	✓	✓
P16	P16	I/O	Hi-Z	-	I/O port	✓	✓	✓
	FOUT	O			Clock external output	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
	ADIN05	A			12-bit A/D converter Ch.0 analog signal input 5	✓	✓	✓
P17	P17	I/O	Hi-Z	-	I/O port	✓	✓	✓
	EXCL11	I			16-bit PWM timer Ch.1 event counter input 1	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
	ADIN06	A			12-bit A/D converter Ch.0 analog signal input 6	✓	✓	✓
P20	P20	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	SENB1	A			R/F converter Ch.1 sensor B oscillator pin	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
	SEG23	A			LCD segment output	✓	✓	✓
P21	P21	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	SENA1	A			R/F converter Ch.1 sensor A oscillator pin	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
	SEG22	A			LCD segment output	✓	✓	✓
P22	P22	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	REF1	A			R/F converter Ch.1 reference oscillator pin	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
	SEG21	A			LCD segment output	✓	✓	✓
P23	P23	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	RFIN1	A			R/F converter Ch.1 oscillation input	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
	SEG20	A			LCD segment output	✓	✓	✓
P24	P24	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	EXCL20	I			16-bit PWM timer Ch.2 event counter input 0	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
	SEG19	A			LCD segment output	✓	✓	✓
P25	P25	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	EXCL21	I			16-bit PWM timer Ch.2 event counter input 1	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
	SEG18	A			LCD segment output	✓	✓	✓
P26	P26	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	CLPLS	O			IR remote controller clear pulse output	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
	SEG17	A			LCD segment output	✓	✓	✓
P27	P27	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	EXCL00	I			16-bit PWM timer Ch.0 event counter input 0	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	✓
	SEG16	A			LCD segment output	✓	✓	✓
P30	P30	I/O	Hi-Z	✓	I/O port	✓	✓	-
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	-

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Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function	128pin/chip	80pin	64pin
P31	P31	I/O	Hi-Z	✓	I/O port	✓	✓	–
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	–
P32	P32	I/O	Hi-Z	✓	I/O port	✓	✓	–
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	–
P33	P33	I/O	Hi-Z	✓	I/O port	✓	–	–
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	–	–
P34	P34	I/O	Hi-Z	✓	I/O port	✓	–	–
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	–	–
P35	P35	I/O	Hi-Z	✓	I/O port	✓	✓	–
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	–
P36	P36	I/O	Hi-Z	✓	I/O port	✓	–	–
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	–	–
P37	P37	I/O	Hi-Z	✓	I/O port	✓	✓	–
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓	–
P40	P40	I/O	Hi-Z	✓	I/O port	✓	✓	–
P41	P41	I/O	Hi-Z	✓	I/O port	✓	✓	–
P42	P42	I/O	Hi-Z	✓	I/O port	✓	✓	–
P43	P43	I/O	Hi-Z	✓	I/O port	✓	–	–
P44	P44	I/O	Hi-Z	✓	I/O port	✓	–	–
P45	P45	I/O	Hi-Z	✓	I/O port	✓	–	–
P46	P46	I/O	Hi-Z	✓	I/O port	✓	–	–
P47	P47	I/O	Hi-Z	✓	I/O port	✓	–	–
P50	P50	I/O	Hi-Z	✓	I/O port	✓	–	–
P51	P51	I/O	Hi-Z	✓	I/O port	✓	–	–
P52	P52	I/O	Hi-Z	✓	I/O port	✓	–	–
P60	P60	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	RFCLKO0	O			R/F converter Ch.0 clock monitor output	✓	✓	✓
	SEG15	A			LCD segment output	✓	✓	✓
P61	P61	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	RFCLKO1	O			R/F converter Ch.1 clock monitor output	✓	✓	✓
	SEG14	A			LCD segment output	✓	✓	✓
P62	P62	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	REMO	O			IR remote controller transmit data output	✓	✓	✓
	SEG13	A			LCD segment output	✓	✓	✓
P63	P63	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	LFRO	O			LCD frame signal monitor output	✓	✓	✓
	SEG12	A			LCD segment output	✓	✓	✓
P64	P64	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	#ADTRG0	I			12-bit A/D converter Ch.0 trigger input	✓	✓	✓
	SEG11	A			LCD segment output	✓	✓	✓
P65	P65	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	SEG10	A			LCD segment output	✓	✓	✓
P66	P66	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	SEG9	A			LCD segment output	✓	✓	✓
P67	P67	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	SEG8	A			LCD segment output	✓	✓	✓
P70	P70	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	SEG7	A			LCD segment output	✓	✓	✓
P71	P71	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	SEG6	A			LCD segment output	✓	✓	✓
P72	P72	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	SEG5	A			LCD segment output	✓	✓	✓
P73	P73	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	SEG4	A			LCD segment output	✓	✓	✓
P80	P80	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	COM7	A			LCD common output	✓	✓	✓
	SEG3	A			LCD segment output	✓	✓	✓
P81	P81	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	COM6	A			LCD common output	✓	✓	✓
	SEG2	A			LCD segment output	✓	✓	✓

Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function	128pin/chip	80pin	64pin
P82	P82	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	COM5	A			LCD common output	✓	✓	✓
	SEG1	A			LCD segment output	✓	✓	✓
P83	P83	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	COM4	A			LCD common output	✓	✓	✓
	SEG0	A			LCD segment output	✓	✓	✓
P84	P84	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	COM3	A			LCD common output	✓	✓	✓
P85	P85	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	COM2	A			LCD common output	✓	✓	✓
P86	P86	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	COM1	A			LCD common output	✓	✓	✓
P87	P87	I/O	Hi-Z	✓	I/O port	✓	✓	✓
	COM0	A			LCD common output	✓	✓	✓
PD0	DST2	O	O (L)	✓	On-chip debugger status output	✓	✓	✓
	PD0	I/O			I/O port	✓	✓	✓
PD1	DSIO	I/O	I (Pull-up)	✓	On-chip debugger data input/output	✓	✓	✓
	PD1	I/O			I/O port	✓	✓	✓
PD2	DCLK	O	O (H)	-	On-chip debugger clock output	✓	✓	✓
	PD2	O			Output port	✓	✓	✓
PD3	PD3	I/O	Hi-Z	-	I/O port	✓	✓	✓
	OSC3	A			OSC3 oscillator circuit input	✓	✓	✓
PD4	PD4	I/O	Hi-Z	-	I/O port	✓	✓	✓
	OSC4	A			OSC4 oscillator circuit output	✓	✓	✓
SEG24–27	SEG24–27	A	Hi-Z	-	LCD segment output	✓	✓	-
SEG28–34	SEG28–34	A	Hi-Z	-	LCD segment output	✓	-	-
SEG35–38	SEG35–38	A	Hi-Z	-	LCD segment output	✓	✓	-
SEG39–47	SEG39–47	A	Hi-Z	-	LCD segment output	✓	-	-

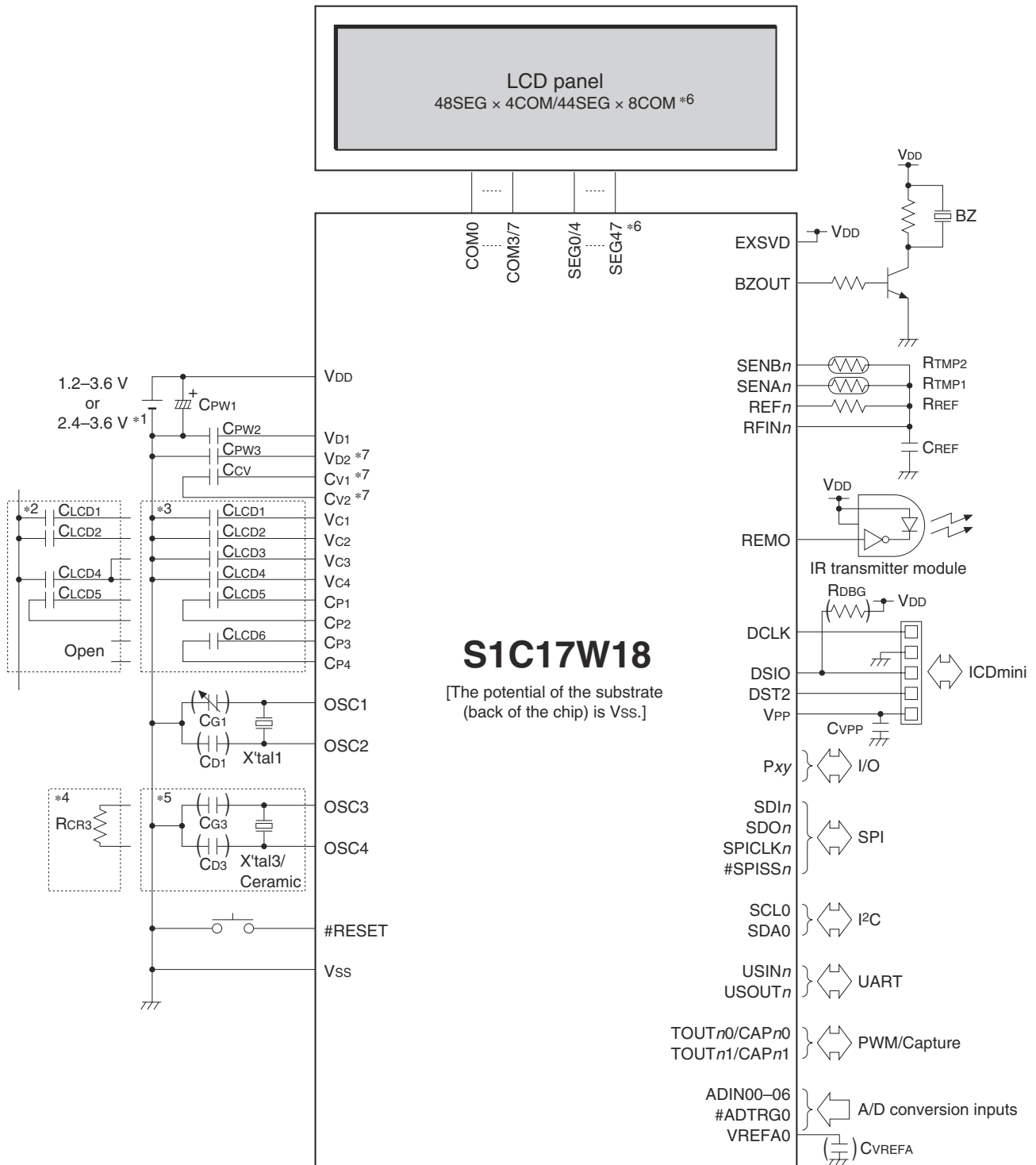
Universal port multiplexer (UPMUX)

The universal port multiplexer (UPMUX) allows software to select the peripheral circuit input/output function to be assigned to each pin from those listed below. Note, however, that a function cannot be assigned to two or more pins simultaneously.

Peripheral circuit	Signal to be assigned	I/O	Channel number <i>n</i>	Function
Synchronous serial interface (SPIA)	SDIn	I	<i>n</i> = 0, 1	SPIA Ch. <i>n</i> data input
	SDOn	O		SPIA Ch. <i>n</i> data output
	SPICLK _n	I/O		SPIA Ch. <i>n</i> clock input/output
	#SPISS _n	I		SPIA Ch. <i>n</i> slave-select input
I ² C (I2C)	SCL _n	I/O	<i>n</i> = 0	I2C Ch. <i>n</i> clock input/output
	SDA _n	I/O		I2C Ch. <i>n</i> data input/output
UART (UART)	USIN _n	I	<i>n</i> = 0, 1	UART Ch. <i>n</i> data input
	USOUT _n	O		UART Ch. <i>n</i> data output
16-bit PWM timer (T16B)	TOUT _{n0} /CAP _{n0}	I/O	<i>n</i> = 0, 1, 2	T16B Ch. <i>n</i> PWM output/capture input 0
	TOUT _{n1} /CAP _{n1}	I/O		T16B Ch. <i>n</i> PWM output/capture input 1

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■ BASIC EXTERNAL CONNECTION DIAGRAM



- *1: For Flash programming
- *2: When 1/3 bias is selected
- *3: When 1/4 bias is selected
- *4: When OSC3 CR oscillator is selected
- *5: When OSC3 crystal/ceramic oscillator is selected
- *6: The SEG24–SEG47 pins do not exist in the 64-pin package. (24SEG × 4COM/20SEG × 8COM)
The SEG28–SEG34 and SEG39–SEG47 pins do not exist in the 80-pin package. (32SEG × 4COM/28SEG × 8COM)
- *7: The V_{D2}, CV₁, and CV₂ pins do not exist in the 64-pin and 80-pin packages.
- (): Do not mount components if unnecessary.

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