3A Single Cell Li-on Battery Slave Switching Charger

General Description

The RT9465 is a switch-mode single cell li-Ion/Li-Polymer battery charger for portable applications. It integrates a synchronous PWM controller and high accuracy voltage regulation. Besides, the charging current is regulated through the integrated sensing MOSFET.

The RT9465 optimizes the charging task by using a control algorithm to vary the charge rate via different modes, including fast charge mode and constant voltage mode. The key charge parameters are programmable via the I^2C interface. The junction temperature is monitored by ADC.

Other features include under-voltage protection, over-voltage protection (including V_{BAT} and V_{IN} side), thermal regulation and MIVR.

The RT9465 is available in a WQFN-16L 3x3 package.

Ordering Information

RT9465 □□

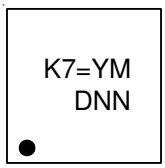
- Package Type
  QW : WQFN-16L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



K7= : Product Code

YMDNN : Date Code

Features

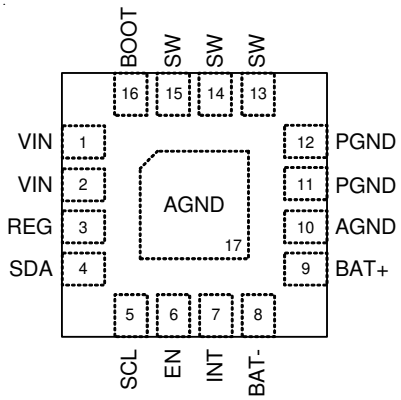
- **Input Voltage Range : 3.9V to 14V**
- **Synchronous 1.5MHz/0.75MHz Switching Frequency 95% Max. Duty**
- **Up to 92%/94% Peak Efficiency at V_{IN} = 9V/5V**
- **V_{IN} Over-Voltage Protection : 14.5V**
- **V_{IN} Under-Voltage Protection : 3.8V**
- **V_{IN} Under-Voltage-Lock-Out : 3.3V**
- **Fault Detection (V_{IN} and V_{BAT} Monitoring)**
- **Programmable Minimum Input Voltage Range : 3.9V to 13.4V (0.1V/Step)**
- **Programmable Battery Voltage Regulation Range : 3.8V to 5.06V (0.02V/Step)**
- **Programmable End of Charge Range : 0.6A to 1.6A (0.1A/Step)**
- **Programmable Average Output Current Regulation Range : 0.6A to 3A (0.1A/Step)**
- **Junction Temperature Monitor : 60°C to 116°C (4°C/Step)**
- **V_{IN} Minimum Input Voltage Regulation (MIVR) : ±3%**
- **Battery CV (Constant Voltage) Regulation : ±1%**
- **Output CC (Constant Current) Regulation, Output Current < 1A : ±100mA (V_{IN} = 9V/12V)**
- **Output CC (Constant Current) Regulation, Output Current > 1A : ±10% (V_{IN} = 9V/12V)**
- **Junction Temperature Monitor Accuracy : ±3°C**
- **Thermal Shutdown : 160°C**

Applications

- Cellular Telephones
- Personal Information Appliances
- Tablet PC, Power Bank
- Portable Instruments

Pin Configuration

(TOP VIEW)

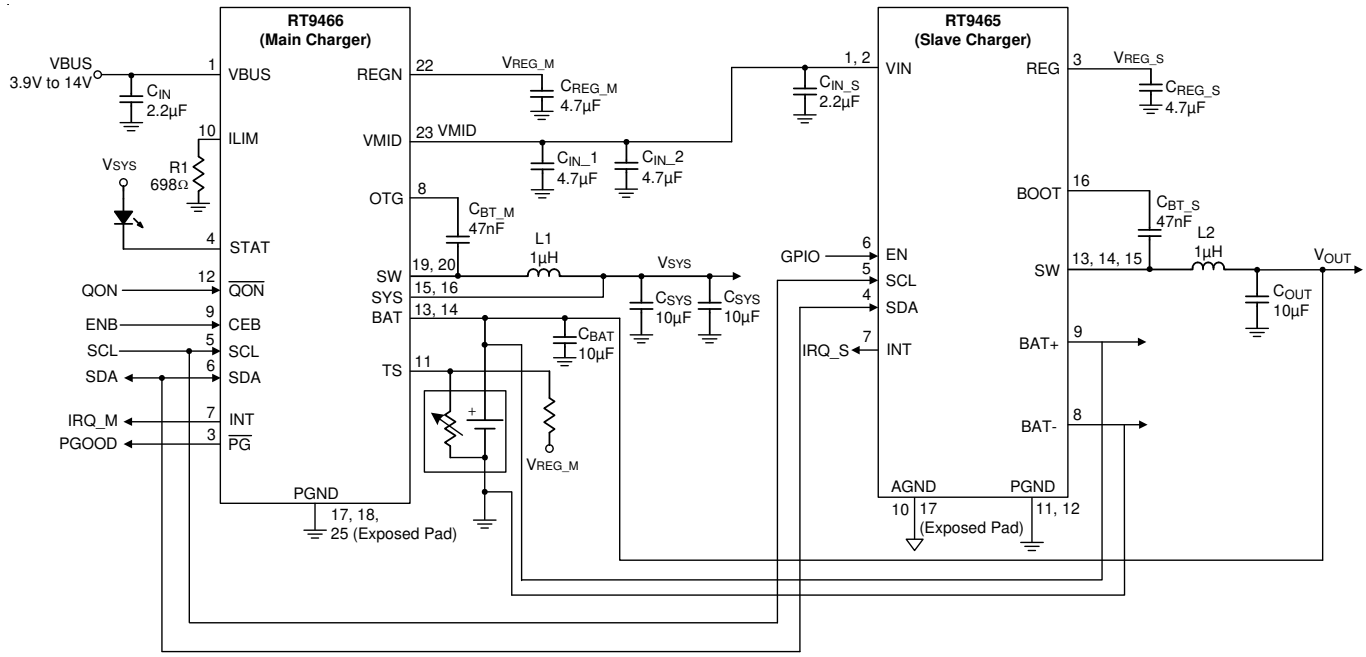


WQFN-16L 3x3

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 2	VIN	Power input. Bypass VIN to GND with a 2.2μF/25V ceramic capacitor.
3	REG	PWM low-side driver and bootstrap power supply. Bypass REGN to GND with a 4.7μF/6.3V ceramic capacitor.
4	SDA	I^2C interface serial clock input. Open-drain. An external pull-up resistor 10kΩ is required.
5	SCL	I^2C interface serial data input/output. Open-drain. An external pull-up resistor 10kΩ is required.
6	EN	Device enable control pin. Pull low to disable device.
7	INT	Open-drain. Interrupt signal to Host.
8	BAT-	Negative battery voltage sense.
9	BAT+	Positive battery voltage sense.
10, 17 (Exposed Pad)	AGND	Analog ground. The exposed pad must be soldered to a large PCB and connected to AGND for maximum thermal dissipation.
11, 12	PGND	Power ground.
13, 14, 15	SW	Switch node. Connect to an external inductor.
16	BOOT	Bootstrap supply for high-side MOSFET. Connect 47nF/16V ceramic capacitor across BOOT and SW.

Typical Application Circuit



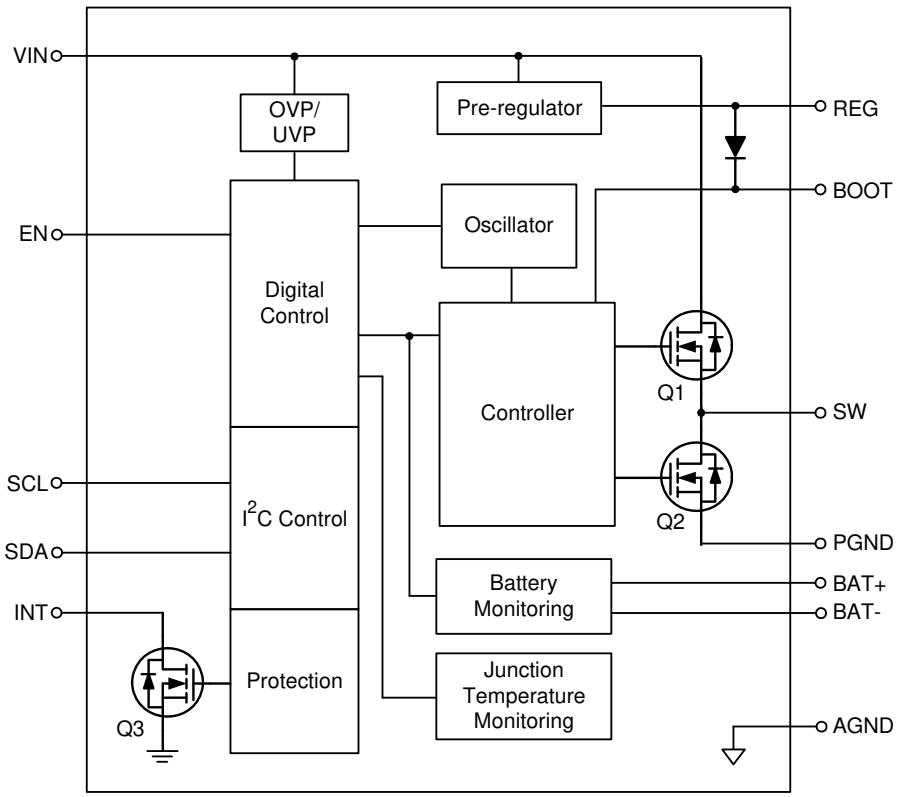
Note : The total C_{IN} of slave charger between PMID pin of main charger is 10μF at least.

Table 1. Component List of Evaluation Board

Reference	Qty	Part Number	Description	Package	Manufacturer
C_{IN_S}	1	GRM155R61E225KE11	2.2μF/25V/X5R	0402	muRata
C_{REG_S}	1	GRM155R60J475ME47	4.7μF/6.3V/X5R	0402	muRata
C_{BT_S}	1	GRM033R61C473KE84	47nF/16V/X5R	0201	muRata
C_{OUT}	1	GRM188R61A106KE69	10μF/10V/X5R	0603	muRata
L2	1	DFE252012F-1R0M	1μH	2.5x2.0x1.2	muRata
U1	1	RT9465GQW	Chip	WQFN-16L 3x3	RICHTEK

Note 1. The total C_{IN} of slave charger between PMID pin of main charger is 10μF at least.

Functional Block Diagram



Absolute Maximum Ratings (Note 2)

- Supply Input Voltage, VIN ---------- –0.3V to 22V
- BOOT ---------- –0.3V to 22V
- SW ---------- –0.3V to 20V
- REG, SCL, SDA, EN, INT, BAT+, BAT- ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-16L 3x3 ---------- 3.33W
- Package Thermal Resistance (Note 3)
  WQFN-16L 3x3, θ_{JA} ---------- 30°C/W
  WQFN-16L 3x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 5)

- Supply Input Voltage, VIN ---------- 3.9V to 14V
- Charge Current, IBAT ---------- 0.6A to 3A
- Battery Voltage, VBAT ---------- 3.8V to 5.06V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, V_{BAT} = 4.2V, L = 1µH, C_{IN_S} = 2.2µF, C_{OUT} = 10µF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current						
V_{IN} Supply Current	$I_{(VIN)\_SW}$	PWM is switching, V_{IN} = 5V, V_{BAT+} = 3.8V	--	8	--	mA
	$I_{(VIN)\_SW}$	PWM is switching, V_{IN} = 9V, V_{BAT+} = 3.8V	--	28	--	
	$I_{(VIN)\_no\_SW}$	PWM is non-switching, V_{IN} = 5V, V_{BAT+} = 4.4V	--	--	2	
Leakage Current from Battery	I_{BAT_leak}	Charger disable, V_{BAT} = 3.8V	--	--	1	µA
V_{IN}/V_{BAT} Power up						
V_{IN} Under-Voltage Protection	V_{UVP}		3.67	3.8	3.93	V
V_{IN} Under-Voltage Protection Hysteresis	V_{UVP_HYS}		120	200	280	mV
Input Power Regulation						
Input Voltage Regulation Range	V_{MIVR}	I^2C programmable per 0.1V	3.9	--	13.4	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{MIVR} Accuracy	V_{MIVR_ACC}	MIVR = 4.4V, 9V	–3	--	3	%
Protection						
V_{IN}						
IC Active Threshold Voltage	V_{UVLO}	V_{IN} rising	3.05	3.3	3.55	V
IC Active Hysteresis	V_{UVLO_HYS}	V_{IN} falling from UVLO	--	150	--	mV
V_{IN} OVP Threshold Voltage	V_{INOVP}	V_{IN} rising	13.5	14.5	15.5	V
V_{IN} OVP Hysteresis	V_{INOVP_HYS}		--	350	--	mV
V_{BAT}						
Battery OVP	V_{BATOVP}	$(V_{BATOVP\_Rising} - V_{CV})/V_{CV}$	102	104	106	%
Battery UVP	V_{BATUVP}	V_{BAT} falling	2.3	2.4	2.5	V
Thermal Protection						
Over-Temperature Protection	OTP	Thermal shutdown	--	160	--	°C
OTP Hysteresis	OTP_HYS		--	10	--	°C
Thermal Regulation Threshold	TR	Charge current begins to reduce	--	120	--	°C
Battery Charging Interval						
End of Charge						
Battery Voltage Regulation	V_{OREG}	I^2C programmable per 20mV	3.8	--	5.06	V
Battery Voltage Accuracy	V_{OREG_ACC}	Temperature = 0 to 85°C	–1	--	1	%
Fast Charge						
Charging Current	I_{CHG}	I^2C programmable per 0.1A	0.6	--	3	A
I_{CHG} Accuracy	I_{CHG_ACC}	V_{IN} = 5V, charge current > 1A	–15	--	15	%
		V_{IN} = 9V, 12V, charge current > 1A	–10	--	10	
		V_{IN} = 5V, charge current < 1A	–150	--	150	mA
		V_{IN} = 9V, 12V, charge current < 1A	–100	--	100	
End of Charging Current	I_{EOC}	I^2C programmable per 0.1A	0.6	--	1.6	A
I_{EOC} Accuracy	I_{EOC_ACC}	V_{IN} = 5V, 9V, 12V, I_{EOC} setting > 1A	–15	--	15	%
		V_{IN} = 5V, 9V, 12V, I_{EOC} setting < 1A	–150	--	150	mA
Battery Charger						
High-Side On-Resistance	$R_{ON(Q1)}$	From VIN to SW	17	21.5	26	mΩ
Low-Side On-Resistance	$R_{ON(Q2)}$	From SW to PGND	17	21.5	26	mΩ
Charging Efficiency		V_{IN} = 9V, V_{BAT} = 3.8V, and I_{CHG} = 2.5A	--	89.5	--	%
Switching Frequency (1.5MHz)	f_{OSC1}	I^2C programmable 1.5 MHz	1.35	1.5	1.65	MHz
Switching Frequency (750kHz)	f_{OSC2}	I^2C programmable 0.75MHz	0.675	0.75	0.825	MHz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Frequency Accuracy			10	--	10	%
Maximum Duty Cycle		At minimum voltage input	--	95	--	%
Minimum Duty Cycle			0	--	--	%
V_{REG} Regulation	V_{REG}	V_{IN} = 5V	4.74	4.9	5.06	V
EN Pull Low	R_{EN}		180	500	820	kΩ
I^2C Characteristics						
Output Low Voltage	V_{OL}	I_{DS} = 10mA	--	--	0.4	V
SCL, SDA Input Logic High Threshold Voltage	V_{IH}		1.3	--	--	V
SCL, SDA Input Logic Low Threshold Voltage	V_{IL}		--	--	0.4	V
SCL Clock			--	--	400	kHz
Load Capacitance	C_{LOAD}	V_{PULL_UP} = 1.8V	--	--	1	pF
Junction Temperature Monitor Accuracy			-3	--	3	°C
Control I/O Pin						
EN Input Threshold Voltage	V_{IH}	Logic high threshold	1.2	--	--	V
EN Input Threshold Voltage	V_{IL}	Logic low threshold	--	--	0.4	V
Device Turn-On Delay Time After EN Pull-High			--	--	500	μS

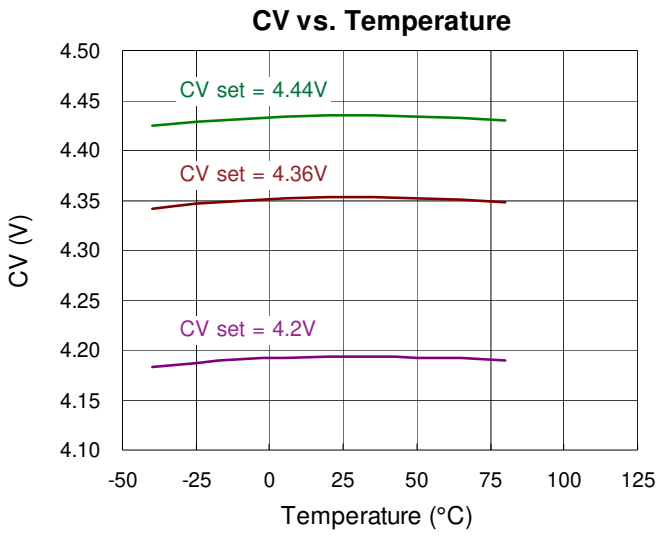
Note 2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

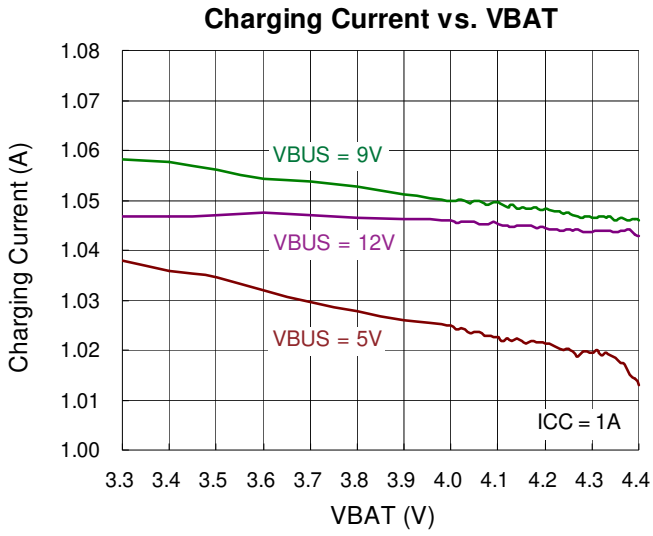
Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

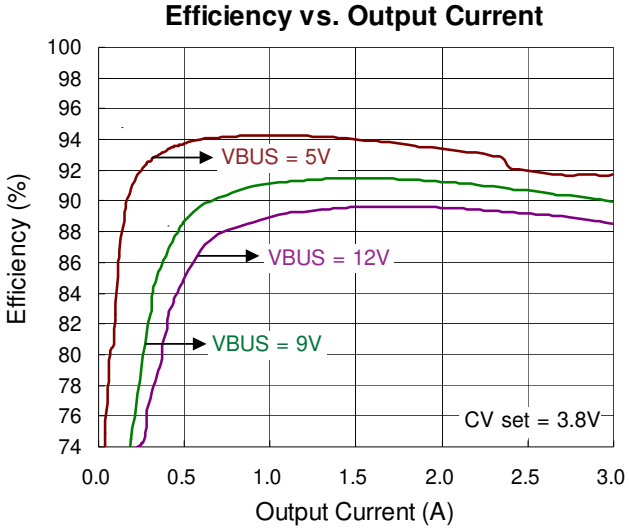
Note 4. Devices are ESD sensitive. Handling precaution is recommended.

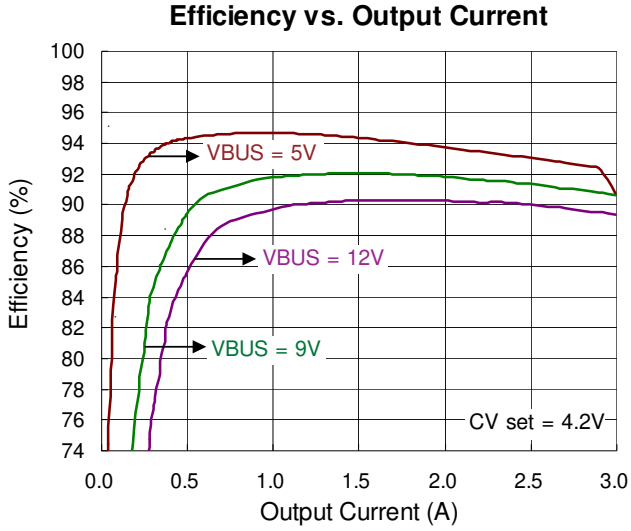
Note 5. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics









I²C Register Information

I²C Slave Address : 1001011 (4BH)

R : Read only

R/W : Read and write

R/C : Read automatically clear

Register Address : 0x00, Register Name : CHG_CTRL0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	RST_REG	0	Y	Y	R/W	All registers reset bit. 0 : No action. (default) 1 : Reset all registers. (Notice : This bit will be reset to "0" after reset procedure finish)
6:0	Reserved	0000000	Y	Y	R/W	Reserved

Register Address : 0x01, Register Name : CHG_CTRL1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	CHG_EN	0	Y	Y	R/W	Charging enable 0 : CHG is disabled (default) 1 : CHG is enabled
6:4	Reserved	100	Y	Y	R/W	Reserved
3	IRQ_pulse	0	Y	Y	R/W	IRQ remind function 0 : IRQ reminding is disabled (default) 1 : IRQ reminding is enabled. If IRQ is triggered and no check action, IRQ pin will be released with every 2s interval and be triggered again.
2:0	Reserved	000	Y	Y	R/W	Reserved

Register Address : 0x02, Register Name : CHG_CTRL2

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	Sel_SWFreq	0	Y	Y	R/W	The switching frequency selection bit 0 : The switching frequency is 1.5MHz. (default) 1 : The switching frequency is 0.75MHz.
6	FixFreq	0	Y	Y	R/W	Charger switching frequency 0 : Charger switching frequency is varied (default) 1 : Charger switching frequency is fixed
5	OSCSS_EN	0	Y	Y	R/W	Charger spread spectrum enable 0 : Disabled (default) 1 : Enabled
4:0	Reserved	00000	Y	Y	R/W	Reserved

Register Address : 0x03, Register Name : CHG_CTRL3

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:2	VOREG<5:0>	010100	Y	Y	R/W	Battery regulation voltage. The delta-V of the battery regulation voltage is 20mV. 000000 : 3.8V 000001 : 3.82V 000010 : 3.84V … 010100 : 4.2V (default) 010101 : 4.22V … 101001 : 4.62V 101010 : 4.64V 101011 : 4.66V ... 111111 : 5.06V
1:0	Reserved	00	Y	Y	R/W	Reserved

Register Address : 0x04, Register Name : CHG_CTRL4

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	THREG <1:0>	11	Y	Y	R/W	Charger thermal regulation threshold 00 : 60°C 11 : 80°C 10 : 100°C 11 : 120°C (default)
5:0	Reserved	000000	Y	Y	R/W	Reserved

Register Address : 0x05, Register Name : CHG_CTRL5

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:1	VMIVR[6:0]	0000101	Y	Y	R/W	Input MIVR threshold setting 0000000 : 3.9V 0000001 : 4V 0000010 : 4.1V 0000011 : 4.2V 0000100 : 4.3V 0000101 : 4.4V (default) 0000110 : 4.5V … 0011110 : 6.9V 0011111 : 7V … 0110010 : 8.9V 0110011 : 9V … 1010000 : 11.9V 1010001 : 12V … 1011111 : 13.4V 1100000 to 1111111 : 13.4V
0	MIVR_EN	1	Y	Y	R/W	MIVR loop enable 0 : MIVR loop disable 1 : MIVR loop enable (default)

Register Address : 0x06, Register Name : CHG_CTRL6

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:3	ICHG[4:0]	10100	Y	Y	R/W	Charging regulation current 00000 to 00110 : 0.6A ... 01001 : 0.9A 01010 : 1A 01011 : 1.1A ... 10011 : 1.9A 10100 : 2A (default) ... 11001 : 2.5A 11010 : 2.6A … 11101 : 2.9A 11110 to 11111 : 3A
2:0	Reserved	000	Y	Y	R/W	Reserved

Register Address : 0x07, Register Name : CHG_CTRL7

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:4	IEOC[3:0]	0101	Y	Y	R/W	EOC current setting 0000 to 0100 : 600mA 0101 : 600mA (default) 0110 : 700mA 0111 : 800mA 1000 : 900mA 1001 : 1000mA 1010 : 1100mA 1011 : 1200mA 1100 : 1300mA 1101 : 1400mA 1110 : 1500mA 1111 : 1600mA
3	EOC_EN	1	Y	Y	R/W	IEOC enable/disable 0 : Disable 1 : Enable (default)
2:0	CHG_TDEG_EOC[2:0]	100	Y	Y	R/W	EOC deglitch time 000 : 120μs 001 : 180μs 010 : 240μs 011 : 360μs 100 : 2ms (default) 101 : 4ms 110 : 8ms 111 : 16ms

Register Address : 0x08, Register Name : CHG_CTRL8

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	TE	1	Y	Y	R/W	Termination enable 0 : Disable charge current termination 1 : Enable charge current termination (default)
6:5	EOC_TIMER[1:0]	00	Y	Y	R/W	EOC back-charging time 00 : 0mins (default) 01 : 30mins 10 : 45mins 11 : 60mins
4:0	Reserved	00000	Y	Y	R/W	Reserved

Register Address : 0x09, Register Name : CHG_CTRL9

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:5	WT_FC[2:0]	000	Y	Y	R/W	Fast charge timer 000 : 4hrs (default) 001 : 6hrs 010 : 8hrs 011 : 10hrs 100 : 12hrs 101 : 14hrs 110 : 16hrs 111 : 20hrs
4	TMR2X_EN	0	Y	Y	R/W	Double charger timer during MIVR, and thermal regulation 0 : Disable 2x extended charger timer (default) 1 : Enable 2x extended charger timer
3	TMR_EN	0	Y	Y	R/W	Charger timer enable/disable 0 : Disable (default) 1 : Enable
2	TMR_PAUSE	0	Y	Y	R/W	Timer control bit 0 : Timer is active (default) 1 : Timer is pause
1:0	Reserved	00	Y	Y	R/W	Reserved

Register Address : 0x0A, Register Name : CHG_CTRL10

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	WDT_EN	0	Y	Y	R/W	Watchdog timer enable/disable 0 : Disable (default) 1 : Enable
6	WDT_TRST	1	Y	Y	R/W	Waiting timer to reset I^2C setup after watchdog is asserted 0 : 200ms 1 : 500ms (default)
5:4	WDT[1:0]	01	Y	Y	R/W	Watchdog timer, from WDTEN is enabled to watchdog IRQ, clear timer by I^2C access 00 : 8s 01 : 40s (default) 10 : 80s 11 : 160s
3:0	Reserved	0000	Y	Y	R/W	Reserved

Register Address : 0x0C, Register Name : CHG_CTRL12

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:4	ADC_RPT[3:0]	0000	Y	Y	R	Report the TEMP_ADC result, sampling every 64T (22μs) and average times (352μs if TEMP_AVG = 0) 0000 : <60 degree (default) 0001 : >60 degree 0010 : >64 degree 0011 : >68 degree 0100 : >72 degree 0101 : >76 degree 0110 : >80 degree 0111 : >84 degree 1000 : >88 degree 1001 : >92 degree 1010 : >96 degree 1011 : >100 degree 1100 : >104 degree 1101 : >108 degree 1110 : >112 degree 1111 : >116 degree
3	TEMP_EN	1	Y	Y	R/W	Temperature ADC measurement function enable/disable 0 : Disable 1 : Enable (default)
2	TEMP_AVG	0	Y	Y	R/W	Choose the average times for TEMP_ADC code calculate 0 : 16times (default) 1 : 32times
1:0	Reserved	00	Y	Y	R/W	Reserved

Register Address : 0x0D, Register Name : CHG_CTRL13

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:4	ADC_HIGH [3:0]	0011	Y	Y	R/W	Temperature sensor threshold set. The IRQ "TEMP_H" will be trigger when the ADC code is larger than ADC_HIGH. 0000 : <60 degree 0001 : >60 degree 0010 : >64 degree 0011 : >68 degree (default) 0100 : >72 degree 0101 : >76 degree 0110 : >80 degree 0111 : >84 degree 1000 : >88 degree 1001 : >92 degree 1010 : >96 degree 1011 : >100 degree 1100 : >104 degree 1101 : >108 degree 1110 : >112 degree 1111 : >116 degree
3:0	ADC_OFFSET [3:0]	0000	Y	Y	R/W	Temperature sensor threshold set. The IRQ "TEMP_L" will be trigger when ADC code is smaller than (ADC_HIGH - ADC_OFFSET) after "TEMP_H" trigged. 0000 : 4 degree (default) 0001 : 4 degree 0010 : 8 degree 0011 : 12 degree 0100 : 16 degree 0101 : 20 degree 0110 : 24 degree 0111 : 28 degree 1000 : 32 degree 1001 : 36 degree 1010 : 40 degree 1011 : 44 degree 1100 : 48 degree 1101 : 52 degree 1110 : 56 degree 1111 : 60 degree

Register Address : 0x20, Register Name : SYSTEM1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	CHG_STAT	00	Y	Y	R	Charger status bit 00 : Ready (default) 01 : Charge in progress 10 : Charge done 11 : Fault
5:4	Reserved	00	Y	Y	R/W	Reserved
3:1	VERSION[2:0]	000	N	N	R	Version code
0	TRIMDONE	0	N	N	R	Trim done

Register Address : 0x30, Register Name : CHG_STATC

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	PWR_RDY	0	Y	Y	R	Power ready status bit 0 : Input power is bad, $V_{IN} < V_{UVP}$ (default) 1 : Input power is good, $V_{IN} > V_{UVP}$
6	CHG_MIVR	0	Y	Y	R	Charger warning. Input voltage MIVR loop active. 0 : MIVR loop is not active (default) 1 : MIVR loop is active
5	CHG_TREG	0	Y	Y	R	Charger warning. Thermal regulation loop active. 0 : Thermal regulation loop is not active (default) 1 : Thermal regulation loop is active
4:0	Reserved	00000	Y	Y	R/W	Reserved

Register Address : 0x31, Register Name : CHG_FAULT

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	CHG_ VBUSOV	0	Y	Y	R	VBUS over-voltage protection. Set when VBUS > VIN_OVP is detected. 0 : VBUS is not over-voltage (default) 1 : VBUS is over-voltage
6	CHG_ VBATSUV	0	Y	Y	R	Charger fault. Battery UVP. 0 : Battery is not UVP (default) 1 : Battery is UVP
5	CHG_ VBATOV	0	Y	Y	R	Charger fault. Battery OVP. 0 : Battery is not OVP (default) 1 : Battery is OVP
4:0	Reserved	00000	Y	Y	R/W	Reserved

Register Address : 0x32, Register Name : CHG_IRQ1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	OTPI	0	Y	Y	R/C	Thermal shutdown fault 0 : No event occurs (default) 1 : Event occurs
6	CHG_ ADPBADI	0	Y	Y	R/C	Charger bad adaptor fault 0 : No event occurs (default) 1 : Event occurs
5	CHG_TMRI	0	Y	Y	R/C	Charger timer time-out fault 0 : No event occurs (default) 1 : Event occurs
4	TEMP_H	0	Y	Y	R/C	Temperature too high fault 0 : No event occurs (default) 1 : Event occurs
3	TEMP_L	0	Y	Y	R/C	Temperature too low fault 0 : No event occurs (default) 1 : Event occurs
2	Reserved	0	Y	Y	R/W	Reserved
1	CHG_STATCI	0	Y	Y	R/C	Status of each CHG_STATC register (Reg0x30) is changed 0 : No event occurs (default) 1 : Event occurs
0	CHG_FAULTI	0	Y	Y	R/C	Status of each CHG_FAULT register (Reg0x31) is changed 0 : No event occurs (default) 1 : Event occurs

Register Address : 0x33, Register Name : CHG_IRQ2

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	CHG_IEOCI	0	Y	Y	R/C	Charging current is lower than EOC current ever occurs 0 : No event occurs (default) 1 : Event occurs
6	CHG_TERMI	0	Y	Y	R/C	Charge terminated event 0 : No event occurs (default) 1 : Event occurs
5	SSFINISHI	0	Y	Y	R/C	Charger soft-start finishes event 0 : No event occurs (default) 1 : Event occurs
4	WDTMRI	0	Y	Y	R/C	Watch dog timer timeout fault 0 : No event occurs (default) 1 : Event occurs
3:0	Reserved	0000	Y	Y	R/W	Reserved

Register Address : 0x40, Register Name : CHG_STATC_Mask

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	PWR_RDYM	0	Y	Y	R/W	Power ready interrupt mask 0 : Interrupt is not masked (default) 1 : Interrupt is masked
6	CHG_MIVRM	0	Y	Y	R/W	Input voltage MIVR loop active interrupt mask 0 : Interrupt is not masked (default) 1 : Interrupt is masked
5	CHG_TREGM	0	Y	Y	R/W	Thermal regulation loop active interrupt mask 0 : Interrupt is not masked (default) 1 : Interrupt is masked
4:0	Reserved	00000	Y	Y	R/W	Reserved

Register Address : 0x41, Register Name : CHG_FAULT_Mask

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	CHG_ VBUSOVM	1	Y	Y	R/W	VBUS over-voltage protection interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
6	CHG_ VBATSUVM	1	Y	Y	R/W	Battery UVP interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
5	CHG_ VBATOVM	1	Y	Y	R/W	Battery OVP interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
4:0	Reserved	00000	Y	Y	R/W	Reserved

Register Address : 0x42, Register Name : CHG_IRQ1_Mask

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	OTPM	1	Y	Y	R/W	Thermal shutdown fault interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
6	CHG_ ADPBADM	1	Y	Y	R/W	Charger bad adaptor fault interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
5	CHG_TMRM	1	Y	Y	R/W	Charger timer time-out fault interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
4	TEMP_HM	1	Y	Y	R/W	Temperature too high fault interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
3	TEMP_LM	1	Y	Y	R/W	Temperature too low fault interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
2	Reserved	1	Y	Y	R/W	Reserved
1	CHG_ STATCM	1	Y	Y	R/W	Status of each CHG_STATC register (Reg0x30) changed interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
0	CHG_FAULTM	1	Y	Y	R/W	Status of each CHG_FAULT register (Reg0x31) changed interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)

Register Address : 0x43, Register Name : CHG_IRQ2_Mask

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	CHG_IEOCM	1	Y	Y	R/C	Charging current is lower than EOC current interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
6	CHG_TERMM	1	Y	Y	R/C	Charge terminated event interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
5	SSFINISHM	1	Y	Y	R/C	Charger soft-start finishes event interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
4	WDTMRM	1	Y	Y	R/C	Watch dog timer timeout fault interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
3:0	Reserved	1111	Y	Y	R/W	Reserved

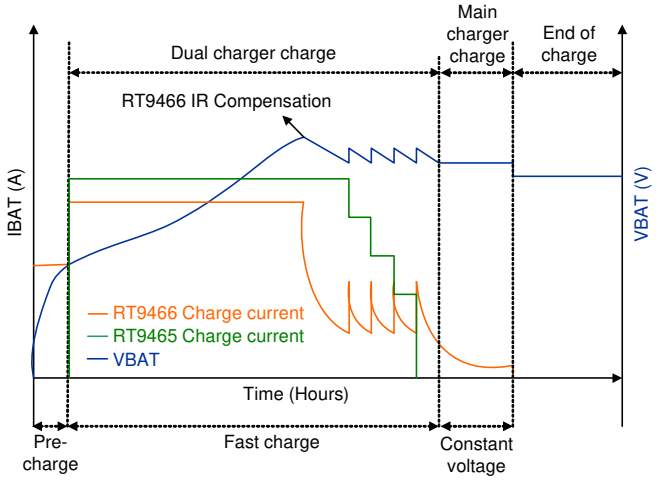
Application Information

Device Power On

The internal bias circuit is powered from V_{IN}. The device will be powered on when the V_{IN} is higher than V_{UVLO} threshold and EN pin is higher than 1.2V. In $V_{IN} > V_{UVLO}$ and EN pin from low logic to high logic condition, the device requires maximum 500μs turn on delay time.

Dual Charger Program Flow

A main charger (RT9466) is required in the system to manage pre-charge, fast-charge and constant voltage state. Below charge profile and program flow show the dual charge interactions. Once battery voltage higher than pre-charge voltage, system needs to enable slave charger (RT9465) to increase charge current and reduce fast charge period. The CV setting of slave charger needs to higher than main charger (include main charger's IR compensation). If main charger triggers IEOC event, the system needs to reduce the slave charger's charge current to next step. When the main charger triggers the IEOC event and slave charger's ICHG is at 600mA, the system needs to turn off slave charger and main charger takes over the constant voltage state period.



Battery charging state	Main charger	Slave charger
Pre-charge state (Main charger duty)	Pre-charge parameter setting	
Constant current charge state (Dual charger work)	1. Set CV point of main charger 2. Set charge current of main charger 3. Set IEOC	1. Set battery regulation voltage (0x03). The setting value needs higher than CV+IR compensation of main charger. 2. Set initial charge regulation current (0x06) If main charger charge current <IEOC (IRQ), and then go to next step down setting. . . . Set charging current = 600mA. If main charger charge current < IEOC (IRQ), and then turn off slave charger.
Constant voltage state (Main charger duty)	Constant voltage state parameter setting	
EOC state (Main charger duty)	EOC parameter setting	

Charge Current (I_{CHG})

The RT9465 senses and averages the inductor current to the regulation loop for constant current charge. Users can set the charge current from 0.6A to 3A by I²C interface.

Protection Features

When below events are triggered, the device turns off buck converter and pulls low INT pin to inform host. The device sets CHG_EN bit to 0 when buck converter turns off.

- V_{IN} Over-Voltage Protection (V_{INOVP})
- V_{IN} Under-Voltage Protection (V_{INUVP})
- Battery Over-Voltage Protection (V_{BATOVP})
- Battery Under-Voltage Protection (V_{BATUVP})
- Over-Temperature Protection (OTP)

Interrupt

The RT9465 reports status to host (CPU, MCU, EC, or...etc.) by the INT (interrupt to host) pin, which is an open-drain output. The INT pin goes low when any fault occurs. It will be automatically reset when all the fault flags are cleared. The IRQ_Pulse (0x01, bit3) provides a reminder function. If the system interrupts by the interrupt signal but does not take any action to check the registers, the INT pin will be released with every 2 seconds and be triggered again.

I²C Interface Timing Diagram

The RT9465 acts as an I²C -bus slave. The I²C -bus master configures the settings for charge mode command bytes to the RT9465 via the 2-wire I²C -bus. After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The second byte selects the register to which the data will be written. The third byte contains data to the selected register.

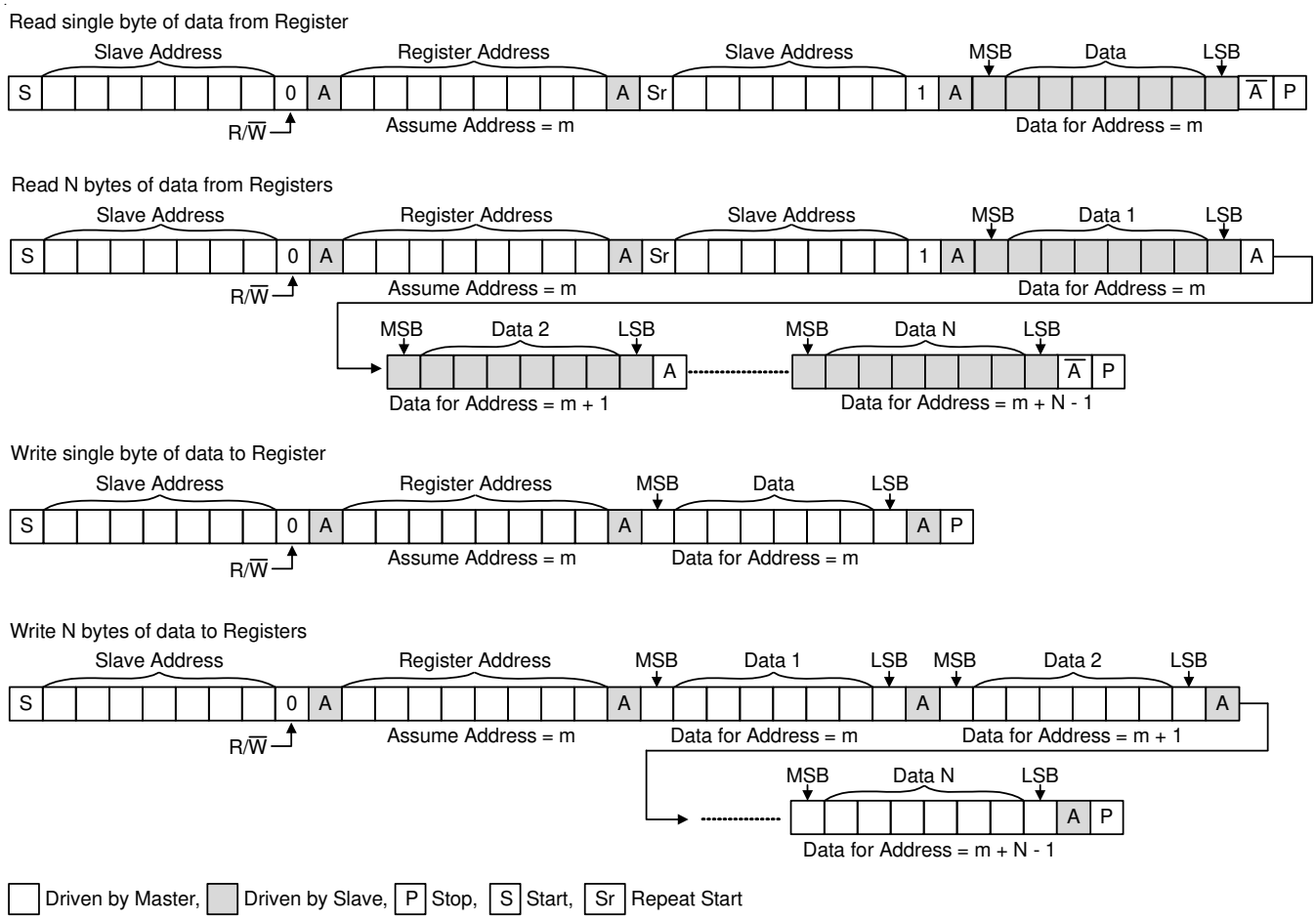


Figure 1. Read and Write Function

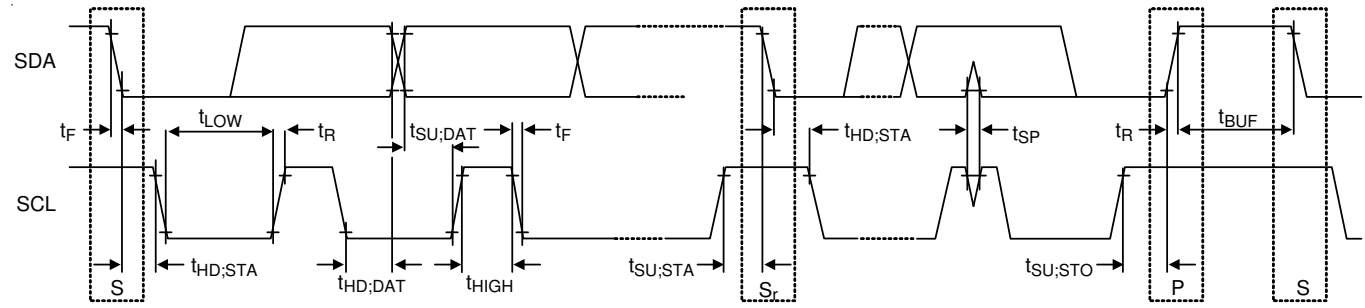


Figure 2. I²C Waveform Information

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-16L 3x3 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / (30°C/W) = 3.33W for a WQFN-16L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

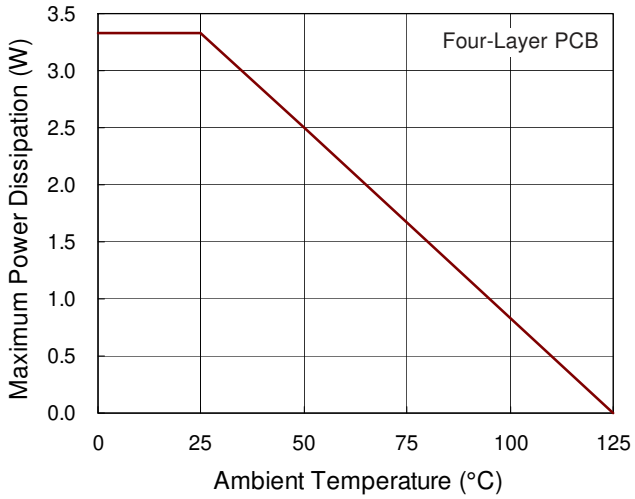


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Considerations

- Place the input and output capacitors as close to the input and output pins as possible.
- Keep the main power traces as wide and short as possible.
- The output inductor and bootstrap capacitor should be placed close to the chip and SW pins.

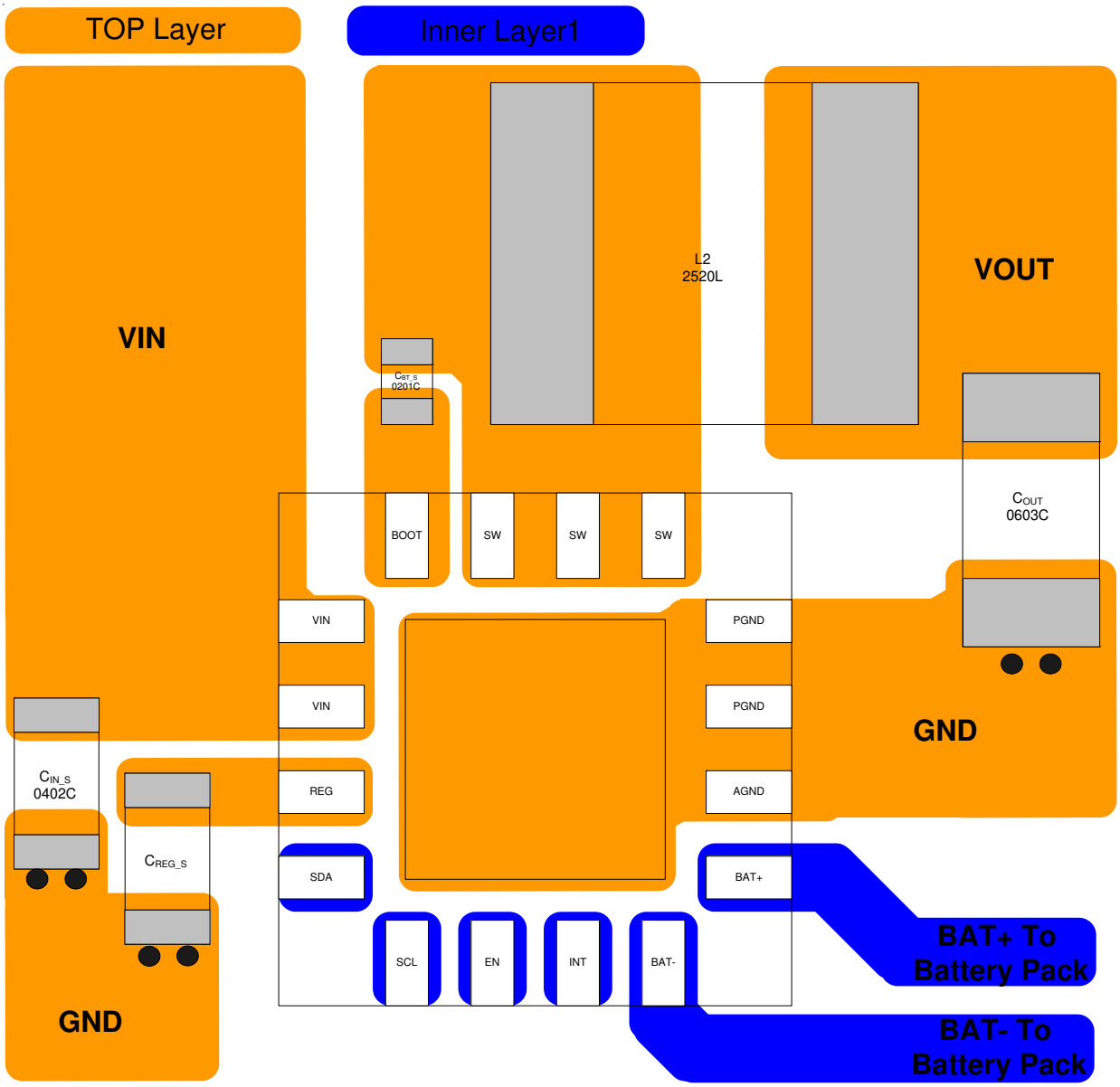
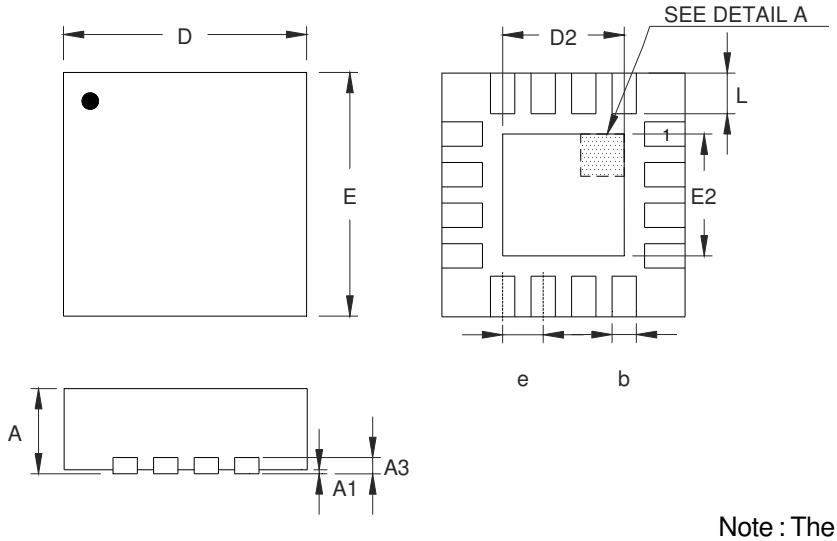
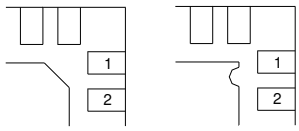


Figure 4. PCB Layout Guide

Outline Dimension





DETAIL A

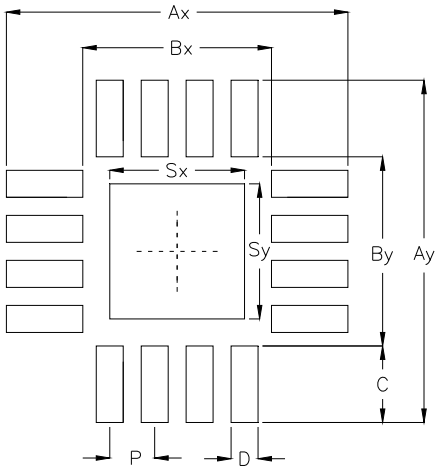
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN3*3-16	16	0.50	3.50	3.50	2.10	2.10	0.70	0.30	1.50	1.50	±0.05

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789