**MICREL** ®

# 8-BIT SHIFT REGISTER

**SY100S341**

## FEATURES

■ **Max. shift frequency of 600MHz**

■ **Max. Clock to Q delay of 1200ps**

■ **$I_{EE}$ min. of −150mA**

■ **Industry standard 100K ECL levels**

■ **Extended supply voltage option:**
  **$V_{EE}$ = −4.2V to −5.5V**

■ **Voltage and temperature compensation for improved noise immunity**

■ **Internal 75kΩ input pull-down resistors**

■ **70% faster than Fairchild 300K at lower power**

■ **Function and pinout compatible with Fairchild F100K**

■ **Available in 28-pin PLCC package**
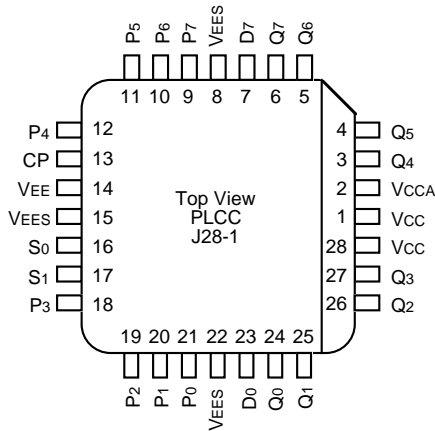
## DESCRIPTION

The SY100S341 offer eight D-type, edge-triggered flip-flops with both individual inputs for parallel operation as well as serial inputs for bidirectional shifting, and are designed for use in high-performance ECL systems. Data is clocked into the flip-flops on the rising edge of the clock.

The mode of operation is selected by two Select inputs ($S_0$, $S_1$) which determine if the device performs a shift, hold or parallel entry function, as described in the Truth Table. The inputs on these devices have 75kΩ pull-down resistors.

## PIN NAMES

| Label | Function |
|---|---|
| CP | Clock Pulse Input |
| $S_0 — S_1$ | Select Inputs |
| $D_0 — D_7$ | Serial Inputs |
| $P_0 — P_7$ | Parallel Inputs |
| $Q_0 — Q_7$ | Data Outputs |
| $V_{EES}$ | $V_{EE}$ Substrate |
| $V_{CCA}$ | $V_{CCO}$ for ECL Outputs |

**28-Pin PLCC (J28-1)**

## Ordering Information

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|---|---|---|---|---|
| SY100S341JC | J28-1 | Commercial | SY100S341JC | Sn-Pb |
| SY100S341JCTR[1] | J28-1 | Commercial | SY100S341JC | Sn-Pb |
| SY100S341JZ[2] | J28-1 | Commercial | SY100S341JZ with Pb-Free bar-line indicator | Matte-Sn |
| SY100S341JZTR[1, 2] | J28-1 | Commercial | SY100S341JZ with Pb-Free bar-line indicator | Matte-Sn |

**Notes:**

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

## BLOCK DIAGRAM
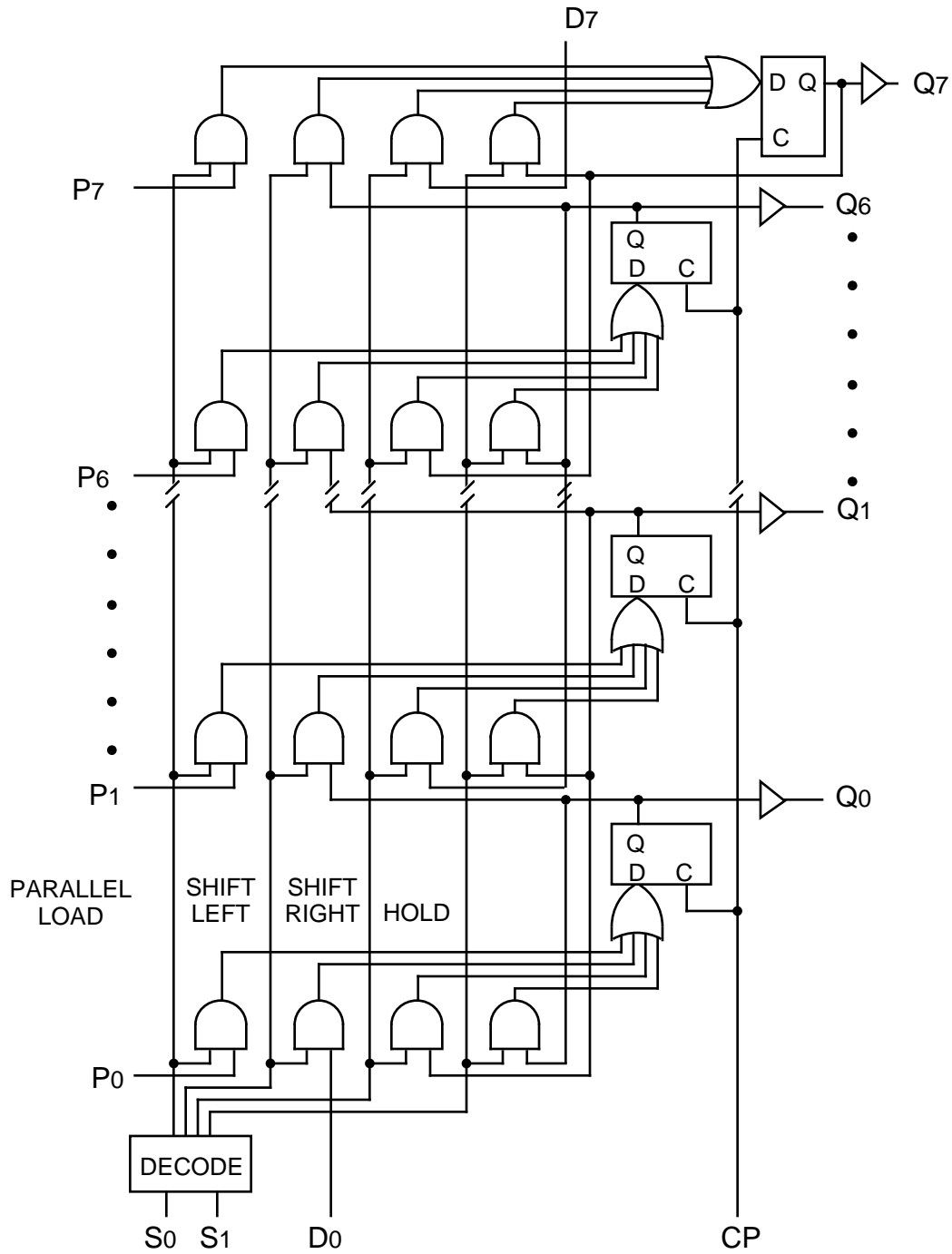
## TRUTH TABLE

| Function | Inputs | | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $D_7$ | $D_0$ | $S_1$ | $S_0$ | CP | $Q_7$ | $Q_6$ | $Q_5$ | $Q_4$ | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
| Load Register | X | X | L | L | u | $P_7$ | $P_6$ | $P_5$ | $P_4$ | $P_3$ | $P_2$ | $P_1$ | $P_0$ |
| Shift Left | X | L | L | H | u | $Q_6$ | $Q_5$ | $Q_4$ | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ | L |
| Shift Left | X | H | L | H | u | $Q_6$ | $Q_5$ | $Q_4$ | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ | H |
| Shift Right | L | X | H | L | u | L | $Q_7$ | $Q_6$ | $Q_5$ | $Q_4$ | $Q_3$ | $Q_2$ | $Q_1$ |
| Shift Right | H | X | H | L | u | H | $Q_7$ | $Q_6$ | $Q_5$ | $Q_4$ | $Q_3$ | $Q_2$ | $Q_1$ |
| Hold | X | X | H | H | X | No Change | | | | | | | |
| Hold | X | X | X | X | H | | | | | | | | |
| Hold | X | X | X | X | L | | | | | | | | |

**NOTE:**

1. H = HIGH Voltage Level

   L = LOW Voltage Level

   X = Don't Care

   u = LOW-to-HIGH Transition

## DC ELECTRICAL CHARACTERISTICS

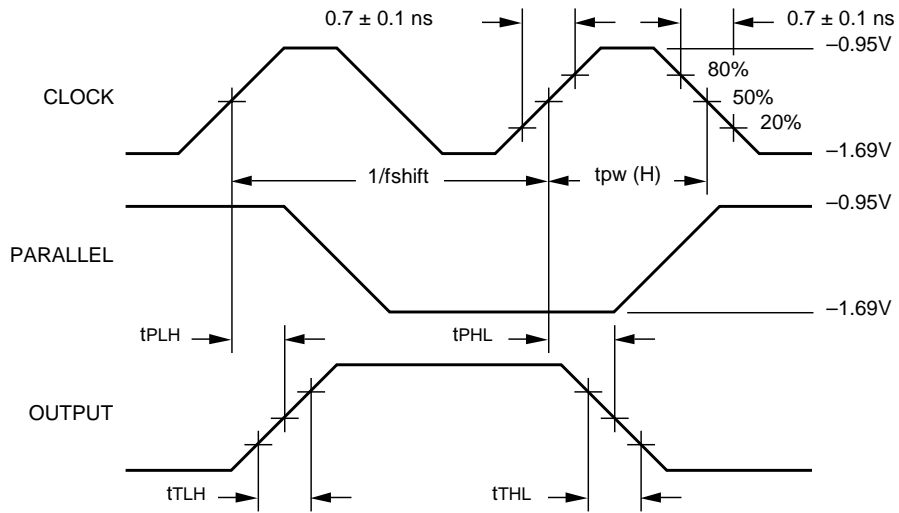$V_{EE}$ = −4.2V to −5.5V unless otherwise specified; $V_{CC}$ = $V_{CCA}$ = GND

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input HIGH Current, All Inputs | — | — | 200 | µA | $V_{IN}$ = $V_{IH}$ (Max.) |
| $I_{EE}$ | Power Supply Current | −150 | −102 | −71 | mA | Inputs Open |

## AC ELECTRICAL CHARACTERISTICS

$V_{EE}$ = −4.2V to −5.5V unless otherwise specified; $V_{CC}$ = $V_{CCA}$ = GND

| Symbol | Parameter | $T_A$ = 0°C | | $T_A$ = +25°C | | $T_A$ = +85°C | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| $f_{shift}$ | Shift Frequency | 600 | — | 600 | — | 600 | — | MHz | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay CP to Output | 450 | 1200 | 450 | 1200 | 450 | 1200 | ps | |
| $t_{TLH}$ $t_{THL}$ | Transition Time 20% to 80%, 80% to 20% | 300 | 900 | 300 | 900 | 300 | 900 | ps | |
| $t_S$ | Set-up Time $D_n$, $P_n$ $S_n$ | 300 600 | — — | 300 600 | — — | 300 600 | — — | ps | |
| $t_H$ | Hold Time $D_n$, $P_n$ $S_n$ | 300 0 | — — | 300 0 | — — | 300 0 | — — | ps | |
| $t_{pw}$ (H) | Pulse Width HIGH, CP | — | 600 | — | 600 | — | 600 | ps | |

## TIMING DIAGRAMS

```
                                    0.7 ± 0.1 ns                              0.7 ± 0.1 ns
                                                                                        −0.95V
                                                                          80%
         CLOCK                                                             50%
                                                                          20%
                                                                                        −1.69V
                                    1/fshift              tpw (H)
                                                                                        −0.95V
         PARALLEL
                                                                                        −1.69V
         tPLH                          tPHL
                                                                          −0.95V
         OUTPUT
                                                                          −1.69V
         tTLH                          tTHL
```

**Propagation Delay and Transition Times**

```
                                                                                        −0.95V
         Pn, Sn, Dn                                     50%
                                                                                        −1.69V
                                              tH
                        tS
                                                                                        −0.95V
         CLOCK                            50%
                                                                                        −1.69V
```
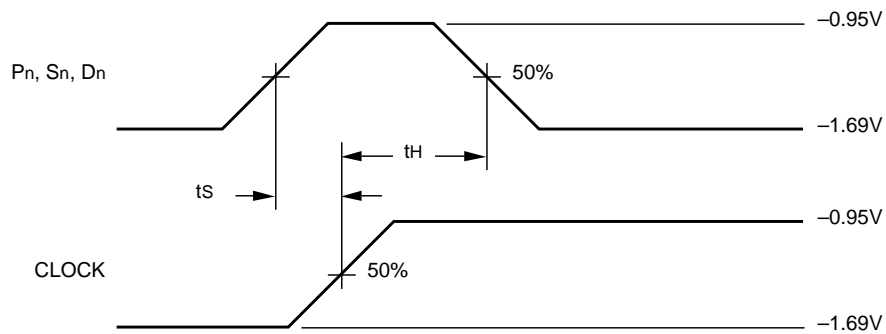
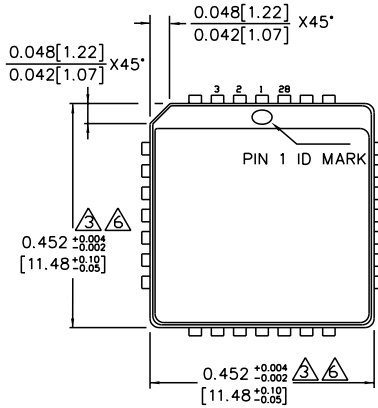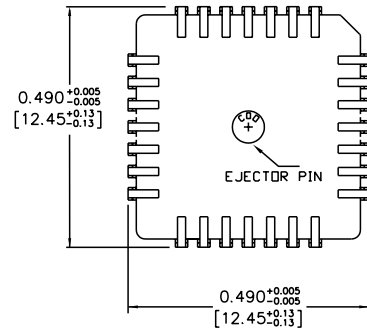**Set-up and Hold Times**

**Notes:**

1. $V_{EE}$ = –4.2V to –5.5V unless otherwise specified; $V_{CC}$ = $V_{CCA}$ = GND.

2. $t_S$ is the minimum time before the transition of the clock that information must be present at the data input.

3. $t_H$ is the minimum time after the transition of the clock that information must remain unchanged at the data input.
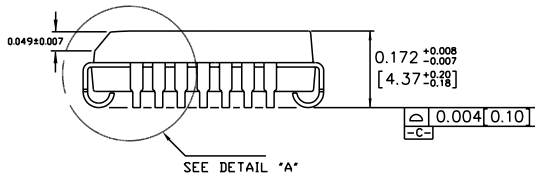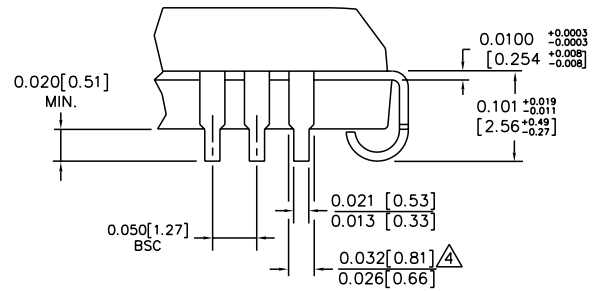
## 28-PIN PLCC (J28-1)



TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL "A"

Rev. A

NOTES:
1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

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