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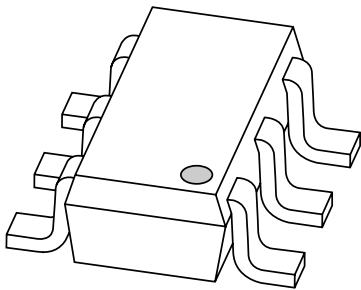
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Kind regards,

Team Nexperia

DATA SHEET



PBSS4140DPN
40 V low V_{CEsat} NPN/PNP
transistor

40 V low V_{CEsat} NPN/PNP transistor

PBSS4140DPN

FEATURES

- 600 mW total power dissipation
- Low collector-emitter saturation voltage
- High current capability
- Improved device reliability due to reduced heat generation
- Replaces two SOT23 packaged low V_{CEsat} transistors on same PCB area
- Reduces required PCB area
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and muting
- LCD backlighting
- Supply line switching circuits
- Battery driven equipment (mobile phones, video cameras and hand-held devices).

DESCRIPTION

NPN/PNP low V_{CEsat} transistor pair in an SC-74 (SOT457) plastic package.

MARKING

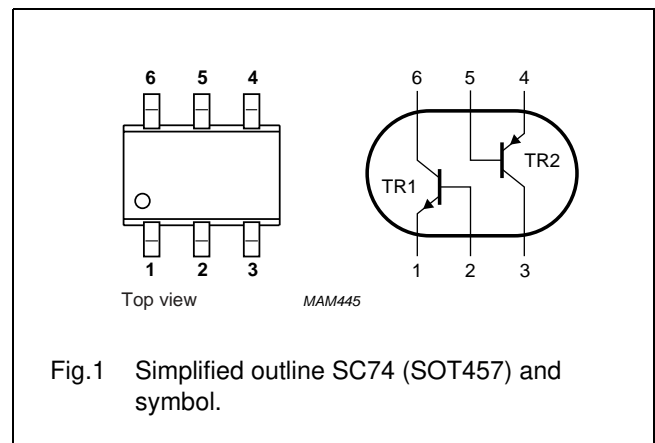
| TYPE NUMBER | MARKING CODE |
|-------------|--------------|
| PBSS4140DPN | M2 |

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | UNIT |
|-------------|---------------------------|------|------------|
| V_{CEO} | collector-emitter voltage | 40 | V |
| I_C | peak collector current | 1 | A |
| I_{CM} | peak collector current | 2 | A |
| TR1 | NPN | – | – |
| TR2 | PNP | – | – |
| R_{CEsat} | equivalent on-resistance | <500 | m Ω |

PINNING

| PIN | DESCRIPTION |
|------|--------------------|
| 1, 4 | emitter TR1; TR2 |
| 2, 5 | base TR1; TR2 |
| 6, 3 | collector TR1; TR2 |



40 V low V_{CEsat} NPN/PNP transistor

PBSS4140DPN

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|--|-------------------------------|--------------------------------------|------|------|------|
| Per transistor; for the PNP transistor with negative polarity | | | | | |
| V_{CBO} | collector-base voltage | open emitter | – | 40 | V |
| V_{CEO} | collector-emitter voltage | open base | – | 40 | V |
| V_{EBO} | emitter-base voltage | open collector | – | 5 | V |
| I_C | collector current (DC) | | – | 1 | A |
| I_{CM} | peak collector current | | – | 2 | A |
| I_{BM} | peak base current | | – | 1 | A |
| P_{tot} | total power dissipation | $T_{amb} \leq 25\text{ °C}$; note 1 | – | 370 | mW |
| T_{stg} | storage temperature | | –65 | +150 | °C |
| T_j | junction temperature | | – | 150 | °C |
| T_{amb} | operating ambient temperature | | –65 | +150 | °C |
| Per device | | | | | |
| P_{tot} | total power dissipation | $T_{amb} \leq 25\text{ °C}$; note 1 | – | 600 | mW |

Note

1. Device mounted on a printed-circuit board, single side copper, tinplated, mounting pad for collector 1 cm².

THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|---------------|---|---------------------|-------|------|
| $R_{th\ j-a}$ | thermal resistance from junction to ambient | in free air; note 1 | 208 | K/W |

Note

1. Device mounted on a printed-circuit board, single side copper, tinplated, mounting pad for collector 1 cm².

40 V low V_{CEsat} NPN/PNP transistor

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CHARACTERISTICS

$T_{amb} = 25\text{ °C}$ unless otherwise specified.

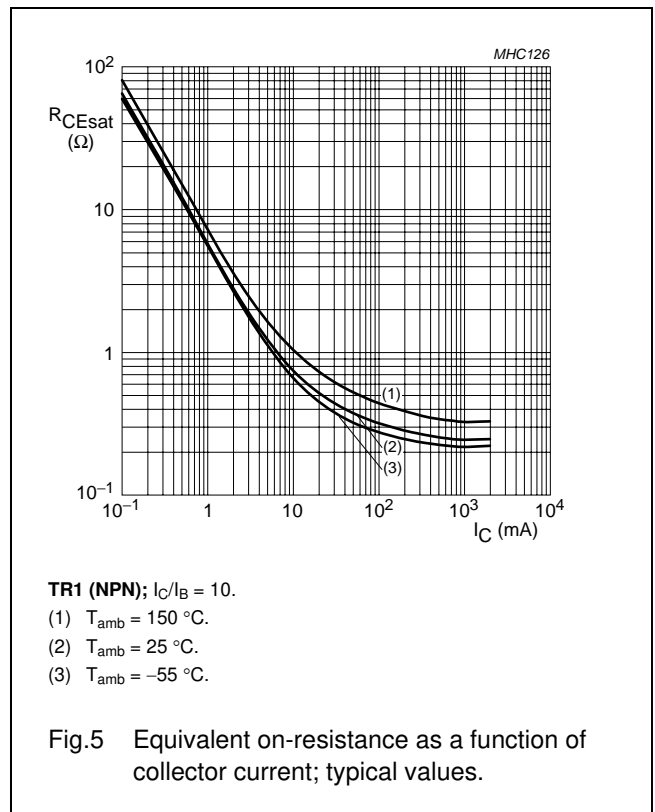
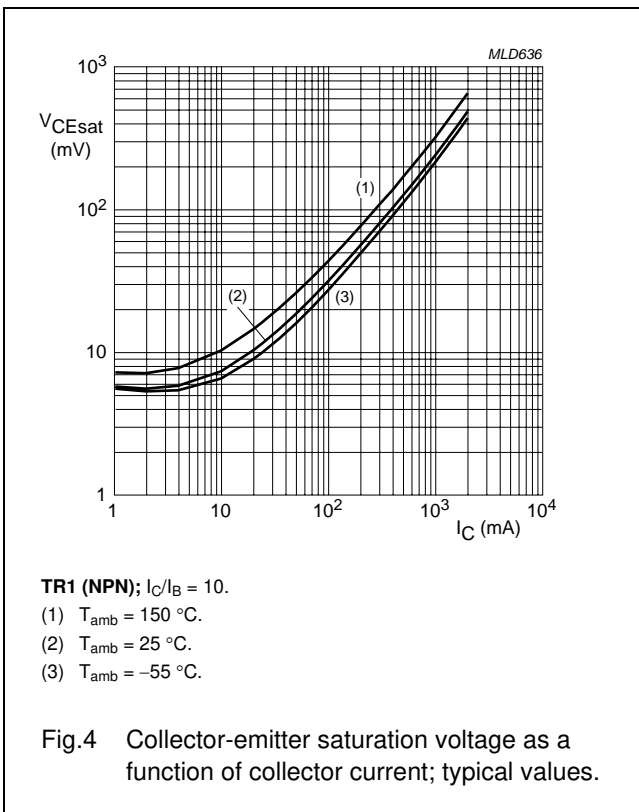
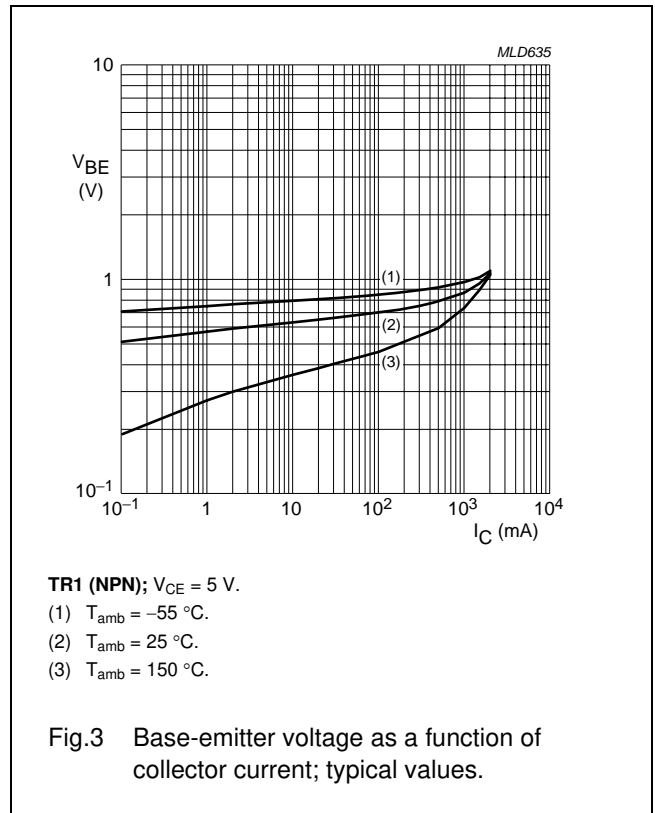
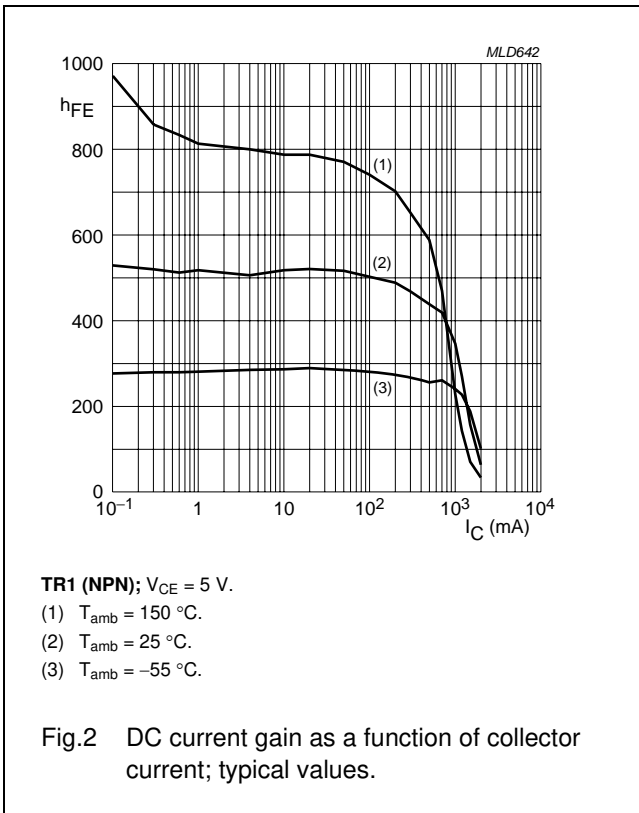
| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|--------------------------------------|--|------|------|------|------------------|
| Per transistor unless otherwise specified; for the PNP transistor with negative polarity | | | | | | |
| I_{CBO} | collector-base cut-off current | $V_{CB} = 40\text{ V}; I_E = 0$ | – | – | 100 | nA |
| | | $V_{CB} = 40\text{ V}; I_E = 0; T_j = 150\text{ °C}$ | – | – | 50 | μA |
| I_{CEO} | collector-emitter cut-off current | $V_{CE} = 30\text{ V}; I_B = 0$ | – | – | 100 | nA |
| I_{EBO} | emitter-base cut-off current | $V_{EB} = 5\text{ V}; I_C = 0$ | – | – | 100 | nA |
| h_{FE} | DC current gain | $V_{CE} = 5\text{ V}; I_C = 1\text{ mA}$ | 300 | – | – | |
| V_{CEsat} | collector-emitter saturation voltage | $I_C = 100\text{ mA}; I_B = 1\text{ mA}$ | – | – | 200 | mV |
| | | $I_C = 500\text{ mA}; I_B = 50\text{ mA}$ | – | – | 250 | mV |
| | | $I_C = 1\text{ A}; I_B = 100\text{ mA}$ | – | – | 500 | mV |
| NPN transistor | | | | | | |
| h_{FE} | DC current gain | $V_{CE} = 5\text{ V}; I_C = 500\text{ mA}$ | 300 | – | 900 | |
| | | $V_{CE} = 5\text{ V}; I_C = 1\text{ A}$ | 200 | – | – | |
| V_{BEsat} | base-emitter saturation voltage | $I_C = 1\text{ A}; I_B = 100\text{ mA}$ | – | – | 1.2 | V |
| V_{BEon} | base-emitter turn-on voltage | $V_{CE} = 5\text{ V}; I_C = 1\text{ A}$ | – | – | 1.1 | V |
| R_{CEsat} | equivalent on-resistance | $I_C = 500\text{ mA}; I_B = 50\text{ mA}; \text{note 1}$ | – | 260 | <500 | $\text{m}\Omega$ |
| f_T | transition frequency | $V_{CE} = 10\text{ V}; I_C = 50\text{ mA}; f = 100\text{ MHz}$ | 150 | – | – | MHz |
| C_c | collector capacitance | $V_{CB} = 10\text{ V}; I_E = I_e = 0; f = 1\text{ MHz}$ | – | – | 10 | pF |
| PNP transistor | | | | | | |
| h_{FE} | DC current gain | $V_{CE} = -5\text{ V}; I_C = -100\text{ mA}$ | 300 | – | 800 | |
| | | $V_{CE} = -5\text{ V}; I_C = -500\text{ mA}$ | 250 | – | – | |
| | | $V_{CE} = -5\text{ V}; I_C = -1\text{ A}$ | 160 | – | – | |
| V_{BEsat} | base-emitter saturation voltage | $I_C = -1\text{ A}; I_B = -50\text{ mA}$ | – | – | -1.1 | V |
| V_{BEon} | base-emitter turn-on voltage | $V_{CE} = -5\text{ V}; I_C = -1\text{ A}$ | – | – | -1.0 | V |
| R_{CEsat} | equivalent on-resistance | $I_C = -500\text{ mA}; I_B = -50\text{ mA}; \text{note 1}$ | – | 300 | <500 | $\text{m}\Omega$ |
| f_T | transition frequency | $V_{CE} = -10\text{ V}; I_C = -50\text{ mA}; f = 100\text{ MHz}$ | 150 | – | – | MHz |
| C_c | collector capacitance | $V_{CB} = -10\text{ V}; I_E = I_e = 0; f = 1\text{ MHz}$ | – | – | 12 | pF |

Note

1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.

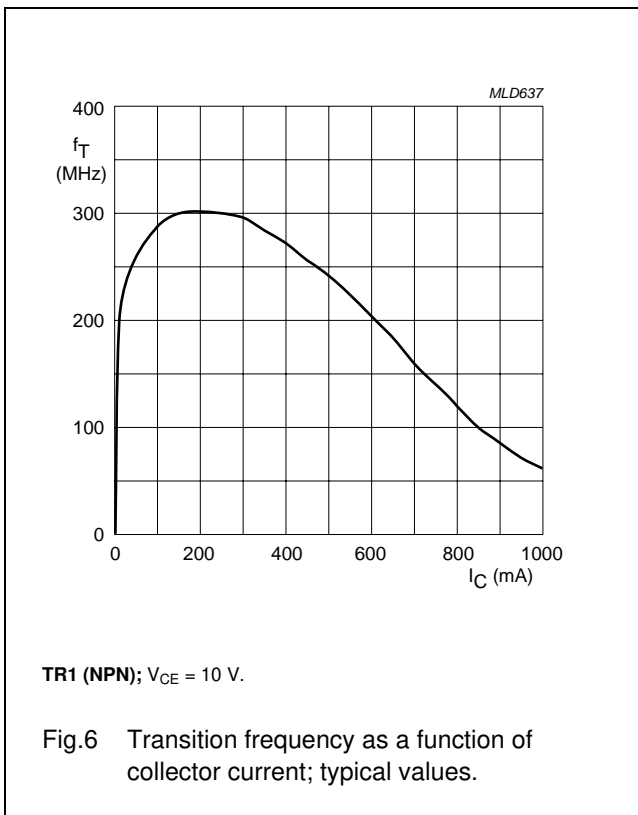
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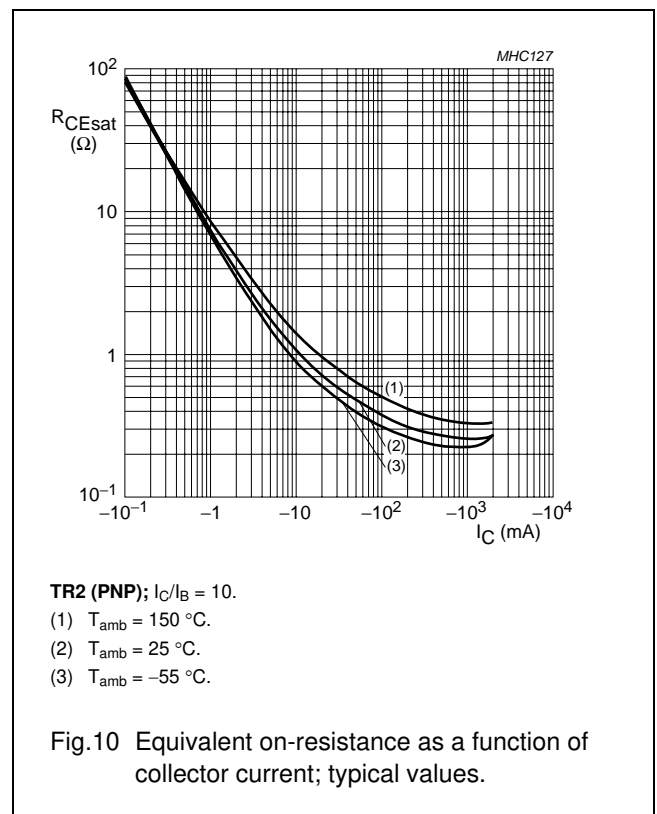
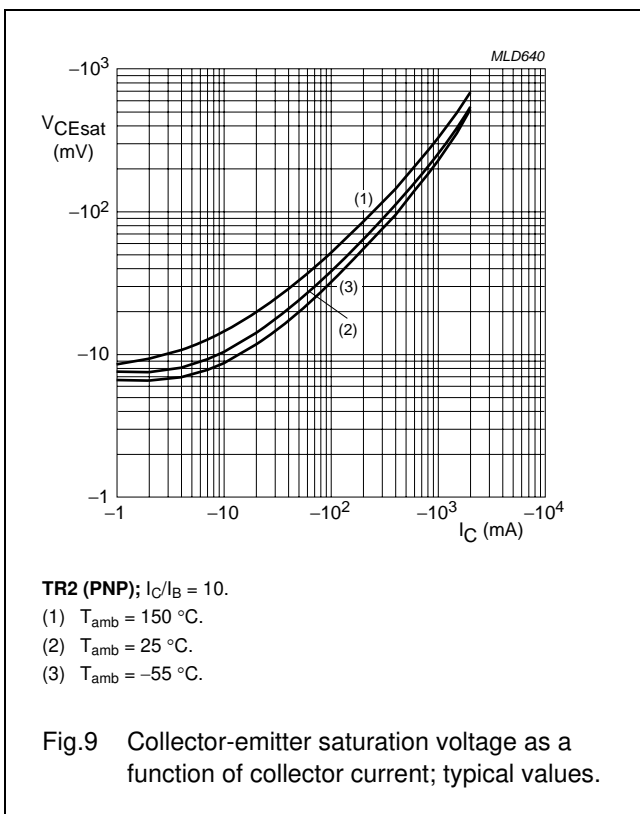
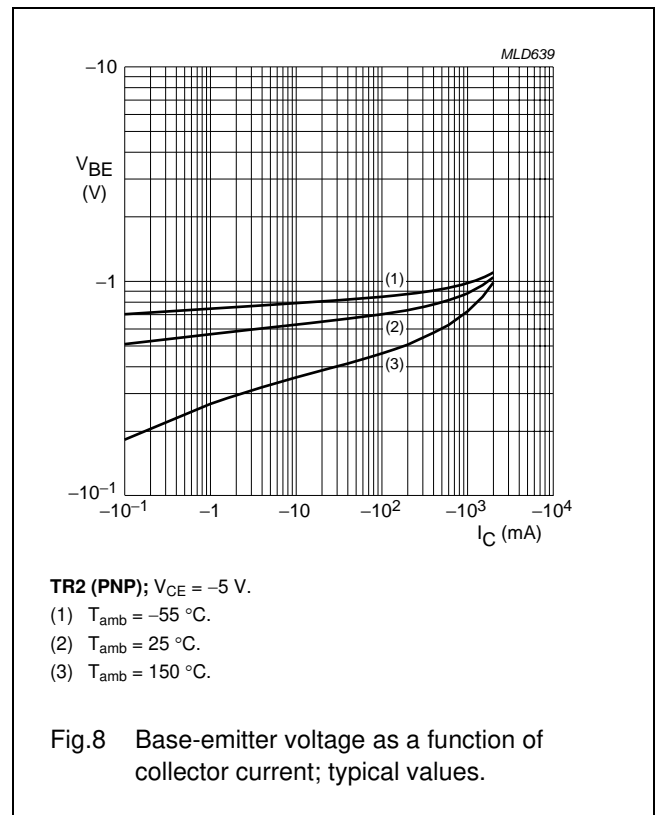
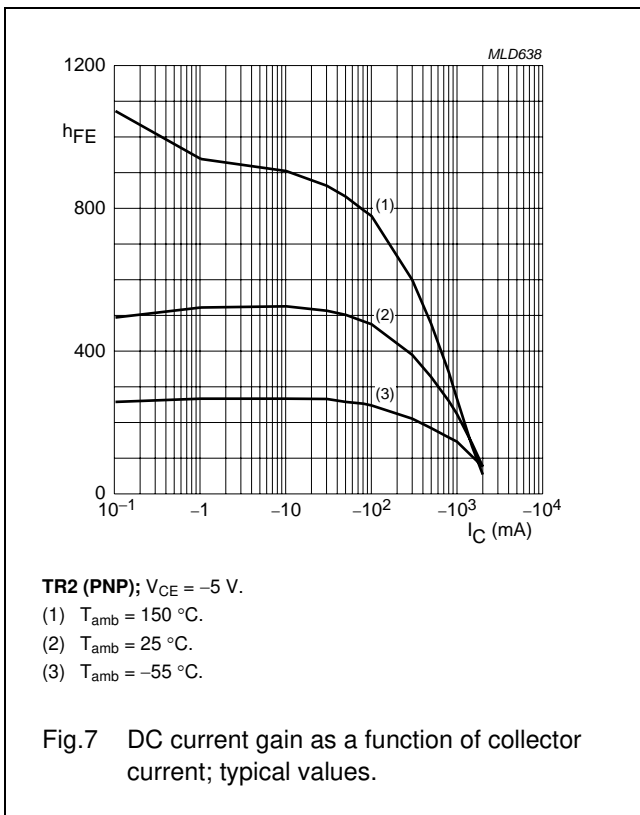
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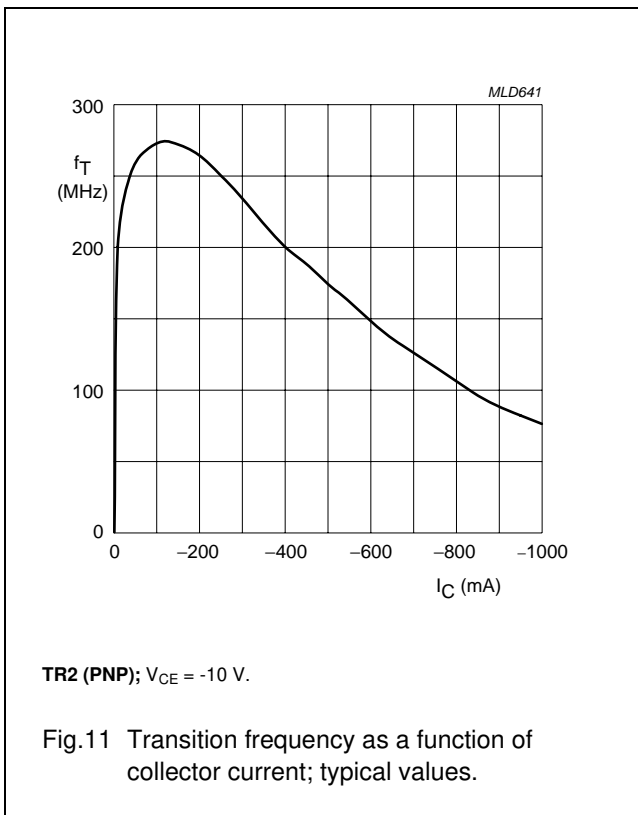
40 V low V_{CEsat} NPN/PNP transistor

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40 V low V_{CEsat} NPN/PNP transistor

PBSS4140DPN



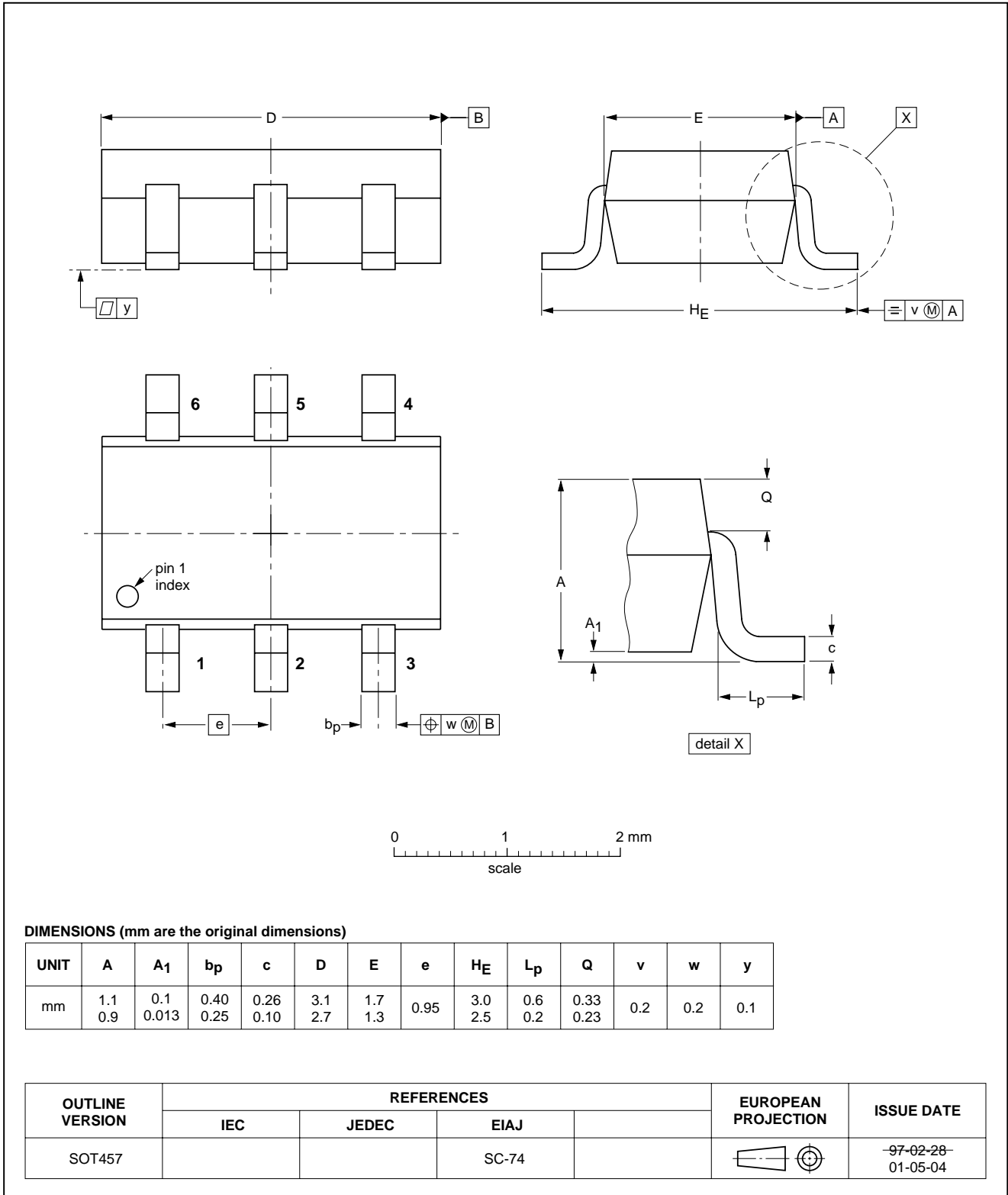
40 V low V_{CEsat} NPN/PNP transistor

PBSS4140DPN

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT457



40 V low V_{CEsat} NPN/PNP transistor

PBSS4140DPN

DATA SHEET STATUS

| DOCUMENT STATUS ⁽¹⁾ | PRODUCT STATUS ⁽²⁾ | DEFINITION |
|--------------------------------|-------------------------------|---|
| Objective data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary data sheet | Qualification | This document contains data from the preliminary specification. |
| Product data sheet | Production | This document contains the product specification. |

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2. The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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NXP Semiconductors

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