Integer Mode

The HMC700LP4(E) synthesizer is capable of operating in integer mode. In integer mode the synthesizer step size is fixed to that of the PFD frequency, f_{PFD}. Integer mode typically has the lower phase noise for a given PFD operating frequency, than fractional mode. The advantage is usually of the order of 4 to 6 dB. Integer mode, however, often requires a lower PFD frequency to meet step size requirements. The fractional mode advantage is that higher PFD frequencies can be used, hence lower phase noise can often be realized in fractional mode.

Integer Frequency Tuning

In integer mode the digital ΔΣ modulator is shut off and the division ratio of the prescaler is set at a fixed value. To run in integer mode clear *frac_rstb* and *buffrstb* Table 13. Then program the integer portion of the frequency as explained by (EQ 4), ignoring the fractional part.

VCO Divider Register Buffering

The VCO divider registers inside the HMC700LP4E are not double buffered. As soon as either the integer (Reg 3) or fractional (Reg 4) VCO divider register is programmed the new value takes effect. Under certain conditions, this can present a momentary mis-load of the internal VCO divider which can take several milliseconds to clear. In time sensitive frequency settling applications a specific programming sequence is required to avoid this delay. This delay arises only when the upper 11 bits of the 16 bit VCO divider (Reg 3) are all changing state such that none of the bits remain as a 1.

In time sensitive applications the following programming sequence should be used.

For Fractional Mode:

Write Register 5 = 0h (zero the Seed);
Write Register 4 = 0h (zero the Fractional divide value);
Write Register 3 to the 'intermediate' integer divide value;
Write Register 3 to the final integer divide value;
Write Register 5 = 50894Ch (or any other non-zero value);
Write Register 4 to the final fractional divide value;

For Integer Mode:

Write Register 3 to the 'intermediate' integer divide value;
Write Register 3 to the final integer divide value;

The 'intermediate' VCO Divider register value (Register 3) must have a '1' in the upper 11 bits (lower 5 bits do not matter) that does not change when going from the starting value to the intermediate value and then from the intermediate value to the final value.

A simple algorithm to calculate a suitable interim value is to 'OR' the Register 3 Start value with the Register 3 Final value. For example, if you are going from 74h to 80h the 'OR'ed value would be F4h. This behaviour is not present on other Hittite Microwave PLL devices.

Soft Reset and Power on Reset

The HMC700LP4(E) features a hardware Power on Reset (POR). All chip registers will be reset to default states approximately 250us after power up. The SPI registers may also be soft reset by an SPI write to strobe register *rst_swrst* (Table 7)

Power Down Mode

Chip Power Down is done by deasserting Chip Enable, CE, pin 23 (Low = Disabled). This will result in all analog functions and internal clocks disabled. Current consumption will typically drop below 10µA in Power Down state. During Power Down, the serial register writes will still operate, however, serial data output is disabled so Read operations will not work.

It is possible to control Power Down Mode from the serial port register *rst_chipen_from_spi* by clearing *rst_chipen_pin_select* (Table 8).

It is also possible to leave various blocks on when in Power Down (see Table 8), including:

a. Digital Clocks
b. Internal bias reference sources
c. PFD block
d. Charge Pump Block
e. Reference Path buffer
f. VCO Path buffer
g. Digital I/O Test pads

Chip Identification

The version of the synthesizer is described in *Table 6*. Version information may be read from the synthesizer by reading the content of *chip_ID* in Reg 00h.

SERIAL PORT

Typical serial port operation can be run with SCK at speeds up to 50MHz.

Serial Port WRITE Operation

Table 4. Timing Characteristics

Parameter	Conditions	Min	Typ	Max	Units
t_1	SEN to SCK Setup Time	8			nsec
t_2	SDI to SCK Setup Time	5			nsec
t_3	SDI to SCK Setup Time	5			nsec
tsck	SCK period	20			nsec
t_4	SCK High Duration	8			nsec
t_5	SCK Low Duration	8			nsec
t_6	SEN High Duration	640			nsec
t_7	SEN Low Duration	20			nsec

A typical WRITE cycle is shown in Figure 15.

a. The Master (host) both asserts SEN (Serial Port Enable) and clears SDI to indicate a WRITE cycle, followed by a rising edge of SCK.
b. The slave (synthesizer) reads SDI on the 1st rising edge of SCK after SEN. SDI low initiates the Write cycle (/WR).
c. Host places the six address bits on the next six falling edges of SCK, MSB first.
d. Slave registers the address bits in the next six rising edges of SCK (2-7).
e. Host places the 24 data bits on the next 24 falling edges of SCK, MSB first .
f. Slave registers the data bits on the next 24 rising edges of SCK (8-31).
g. SEN is de-asserted on the 32nd falling edge of SCK.
h. The 32nd falling edge of SCK completes the cycle.

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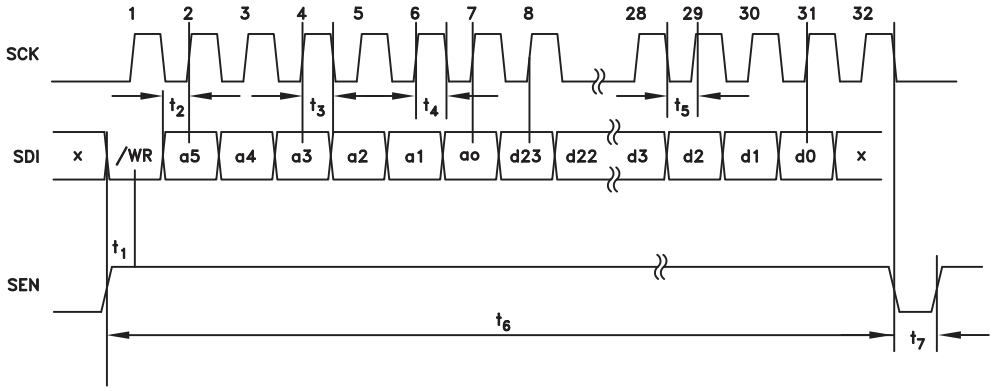

Figure 15. Serial Port Timing Diagram - Write Serial Port WRITE Operation

Serial Port READ Operation

A typical READ cycle is shown in Figure 16.

a. The Master (host) asserts both SEN (Serial Port Enable) and SDI to indicate a READ cycle, followed by a rising edge SCK. Note: The Lock Detect function is multiplexed onto the LD_SDO pin. It is suggested that lock detect (LD) only be considered valid when SEN is low. In fact LD will not toggle until the first active data bit toggles on LD_SDO, and will be restored immediately after the trailing edge of the LSB of serial data out as shown in Figure 15.

b. The slave (synthesizer) reads SDI on the 1st rising edge of SCK after SEN. SDI high initiates the READ cycle (RD).

c. Host places the six address bits on the next six falling edges of SCK, MSB first.

d. Slave registers the address bits on the next six rising edges of SCK (2-7).

e. Slave switches from Lock Detect and places the requested 24 data bits on SD_LDO on the next 24 rising edges of SCK (8-31), MSB first .

f. Host registers the data bits on the next 24 falling edges of SCK (8-31).

g. Slave restores Lock Detect on the 32nd rising edge of SCK.

h. SEN is de-asserted on the 32nd falling edge of SCK.

i. The 32nd falling edge of SCK completes the READ cycle.

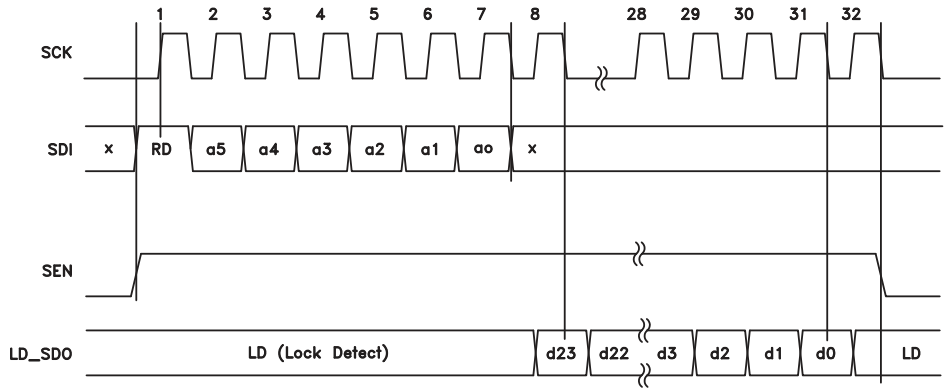

Figure 16. Serial Port Timing Diagram - READ Serial Port Operation

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General Purpose Output (GPO) Pins

The HMC700LP4(E) also supports a simple two pin GPO bus implemented on pins D1 and D0. GPO operation requires that GPO output pads be enabled via *gpio_pads_en* (Table 15). Two bit arbitrary data may be written to the GPO outputs via register *gpo_test*, when *gpo_select* is first set to 10d (Table 20). Other test waveforms, described in Table 20, may be output to the GPO pins according to the value written to *gpo_select*. If the GPO outputs are not used, and it is desirable that they are as quiet as possible then the GPO pads should be disabled via *gpio_pads_en* (Table 15) and *gpo_select* set to a value that has a static source, such as 10d.

Register Map

Note: For Read Operations from register 00h, it is Read Only containing the chip ID. Current Hittite synthesizer chip IDs are shown in Table 6.

Table 6. Reg00h ID (Read Only) Register

Bit	Name	Width	Default	Description
[23:0]	chip_ID	24	478708h or 485901	Part Number, Description HMC700LP4, 16-Bit 5.5V

For write operations to register 00h, it is a Write Only strobe register as defined in Table 7.

Table 7. Reg00h RST Strobe Register

Bit	Name	Width	Default	Description
[0]	rst_swrst	1	n/a	Strobe (WRITE ONLY) generates soft reset. Resets all digital and registers to default states.

Table 8. Reg 01h RST Register

Bit	Name	Width	Default	Description
[0]	rst_chipen_pin_select	1	1	1 = Chip enable via CE pin, CE (Pin 23) enables chip. CE low puts chip in power down. 0 = Chip enable via SPI (rst_chipen_from_spi), CE Pin is ignored
[1]	rst_chipen_from_spi	1	0	1= Chip Enable when rst_chipen_pin_select = 0 0= Power Down when rst_chipen_pin_select = 0 see Power Down Mode description and csp_enable Reg07 <20> If rst_chipen_pin_select =1 this register is ignored
[2]	rst_chipen_digclks_keep_on	1	0	keeps digital clocks on when chip is Power Down from any source
[3]	rst_chipen_bias_keep_on	1	0	keeps chip internal bias generators on when chip is Power Down from any source
[4]	rst_chipen_pfd_keep_on	1	0	keeps internal PFD block on when chip is Power Down from any source
[5]	rst_chipen_chp_keep_on	1	0	keeps internal Charge Pump block on when chip is Power Down from any source
[6]	rst_chipen_refbuf_keep_on	1	0	keeps reference path buffer on when chip is Power Down from any source
[7]	rst_chipen_vcobuf_keep_on	1	0	keeps VCO path RF buffer on when chip is Power Down from any source
[8]	rst_chipen_dig_io_keep_on	1	0	keeps digital IO pins on when chip is Power Down from any source
[9]	rst_chipen_rdiv_fe_sync	1	0	Tri-states the PFD on the next falling edge of the ref clock and also puts the chip to sleep

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Table 9. Reg 02h REFDIV Register

Bit	Name	Width	Default	Description
[13:0]	rdiv	14	1	Reference Divider 'R' Value (EQ 4) 00h - illegal 01h - divide-by-1 (bypass) 10h - divide-by-2 11h - divide-by-3 etc ... 3FFFh - divide-by-16, 383 The reference divider is controlled by several bits in register 8. See register 8 description for details.

Table 10. Reg 03h Frequency Register - Integer Part

Bit	Name	Width	Default	Description	
[15:0]	intg	16	C8h	VCO Divider Integer part, used in all modes, see (EQ 4)	
				Fractional Mode min 36d max 2^16 -1 = 65,535d	**Integer Mode** min 32d max 2^16+31 = 65,567d

Table 11. Reg 04h Frequency - Fractional Part Register

Bit	Name	Width	Default	Description	
[23:0]	frac	24	0	VCO Divider Fractional part (24 bit unsigned) see section Fractional Frequency Tuning	
				Used in Fractional Mode only **min 0d** **max 2^24-1**	

Table 12. Reg 05h SD Seed Register

Bit	Name	Width	Default	Description
[23:0]	seed	24	0	**Fractional Mode**: Seeds fractional modulator **FSK Mode**: Sets f1 in FSK mode when fsk_enable=1 (see section FSK Modulation)

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Table 13. Reg 06h SD CFG Register

Bit	Name	Width	Default	Description
[7:0]	reserved		87h	
[9:8]	order	2	2h	Select the Modulator Type 0 - not used 1 - not used 2 - Type B 3 - Type A
[10]	frac_rstb	1	1	0 holds the frac core in reset reset is used for integer mode or integer mode with CSP
[11]	buff_rstb	1	1	0 holds the frac core buffers in reset reset is used with frac_rstb=0 for integer mode, no CSP
[12]	bypass_mode	1	0	1 fractional modulator output is ignored, but fractional modulator continues to be clocked, used to test the isolation of the digital fractional modulator from the VCO output in integer mode
[13]	autoseed_mode	1	1	loads the seed whenever the frac register is written
[14]	reserved	1	0	Must be kept at 0
[15]	fsk_enable	1	0	enables the FSK mode of operation and FSK input on SDI pin, (see section FSK Modulation)
[16]	reserved	1	0	
[17]	clkrq_refdiv_sel	1	0	selects the SD clock source 1 = reference divider clock 0 = VCO divider clock (recommended)
[18]	clkrq_invert_clk	1	1	inverts the selected sd clock
[19]	sd_spare_out	1	0	spare
[23:20]	csp_corr_magn	4	8h	CSP magnitude correction (see section Cycle Slip Prevention (CSP)) 0000 low magnitude 1111 high magnitude sign of the correction is determined automatically by the CSP state machine

Note: To Enable Frac Mode:

Set Reg 6 [12:10]= 011

Also, Reg 9[9:7] or Reg 9[4:2] must be adjusted to mitigate spurs in frac mode (Dn or Up Leakage)

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Table 14. Reg 07h LKD/CSP Register

Bit	Name	Width	Default	Description
[9:0]	wincnt_max	10	250	lock detect window sets the number of consecutive counts of divided VCO that must land inside the Lock Detect Window to declare LOCK
[10]	lkd_enable	1	1	enables internal lock detect function, Note output to Lock Detect Flag on *LD_SDO* as per Figure 13 controlled by *pfd_LD_opEn*, *Reg 0Bh PFD* Register
[11]	lkd_winasym_enable	1	0	asymmetrical window enables lock detect window to only lag or only lead the divided reference signal at the PFD, see Figure 9
[12]	lkd_win_asym_up_sel	1	0	1 selects lead window when lkd_winasym_enable=1 0 selects lag window when lkd_winasym_enable=1
[13]	ringosc_oneshot_sel	1	0	1 ring osc based one shot for lock detection mode 0 nominal 20nsec analog one shot for lock detection mode
[16:14]	oneshot_duration	3	0	duration of the ringosc based oneshot pulse in lock detection mode
[18:17]	ringosc_cfg	2	0	Lock Detect ringosc frequency trim “00” fastest “11” slowest
[19]	ringosc_mode	1	0	force ringosc ON
[20]	csp_enable	1	1	cycle slip prevention (CSP) enable

See section PFD Lock Detect for more information about this register.

Table 15. Reg 08h Analog EN Register

Bit	Name	Width	Default	Description
[0]	bias_en	1	1	enables main chip bias reference
[1]	cp_en	1	1	charge pump enable
[2]	pfd_en	1	1	pfd enable
[3]	refbuf_en		1	reference path buffer enable. Set to 1 for normal operation.
[4]	vcobuf_en	1	1	vco path RF buffer enable
[5]	gpio_pads_en	1	1	gpio pads enable, Pins D0 and D1 required for use of GPO port or VCO Serial Port
[6]	sdo_pad_en	1	1	LD_SDO pad driver enable (Pin 5) required for use of Lock Detect, Serial Port Read Operation or VCO Serial Port operation
[7]	vcodiv_digclk_en	1	1	vco divider output clk to digital enable
[8]	vcodiv_en	1	1	enable vco divider
[9]	reserved	1	0	
[10]	vcodiv_dutycyc_mode	1	0	vcodiv duty cycle mode stretches the VCO divider output when N>32
[11]	reserved	1	0	Set to 0 for normal operation
[12]	rdiv_ref_to_dig_en	1	1	reference input applied to digital when set to 1, non-divided reference signal is fed to digital (required for normal operation)
[13]	rdiv_refdiv_to_dig_en	1	1	reference divider applied to digital, when set to 1, divided reference signal is fed to digital (required for normal operation)

Charge Pump control register. see Figure 14

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Table 16. Reg 09h CP Register

Bit	Name	Width	Default	Description
[1:0]	Reserved set them to 0	2	0	
[4:2]	cp_UPoffset_sel	3	0	Charge Pump UP Offset Control 55uA/step 000 = 0uA 001 = 55uA 010 = 110uA ... 111 = 385uA
[6:5]	Reserved Set them to 0	2	0	
[9:7]	cp_DNoffset_sel	3	0	Charge Pump DN Offset Control 55uA/step 000 = 0uA 001 = 55uA 010 = 110uA ... 111 = 385uA
[13:10]	cfg cp_UPtrim_sel	4	0	Charge Pump UP Current Trim 7uA/step 0000 = 0uA 0001 = 7uA 0010 = 14uA 0100 = 28uA 1000 = 56uA 1111 = 105uA
[17:14]	cp_DNtrim_sel	4	0	Charge Pump DN Current Trim 7uA/step 0000 = 0uA 0001 = 7uA 0010 = 14uA 0100 = 28uA 1000 = 56uA 1111 = 105uA
[20:18]	cp_UPcurrent_sel	3	0	Charge Pump UP MAIN Current Control 500uA step 000 tristate if PFD also disabled 001 500uA 010 1000uA 011 1500uA 100 2000uA 101 2000uA 110 2000uA 111 2000uA
[23:21]	cp_DNcurrent_sel	3	0	Charge Pump UP MAIN Current Control 500uA step 000 tristate if PFD also disabled 001 500uA 010 1000uA 011 1500uA 100 2000uA 101 2000uA 110 2000uA 111 2000uA

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Table 17. Reg 0Ah CP Op Amp Register

Bit	Name	Width	Default	Description
[1:0]	cp_opamp_bias_sel	2	0	Charge Pump Internal Op-Amp bias select 00 - 540 µA 01 - 689 µA 10 - 943 µA 11 - 1503 µA Enabled with Chg Pump enable Note: this circuit affects internal charge pump operation and linearity. Default setting is recommended. Enabled with Reg08h[1] cp_en

Table 18. Reg 0Bh PFD Register

Bit	Name	Width	Default	Description
[2:0]	pfd_del_sel	3	0	sets PFD reset path delay. Recommended value 010 When in Integer mode, Reg B Bits [2:0] should not be 000 because it doesn't ensure sufficient 'on' time for the CP at 50MHz. This isn't an issue in Fractional Mode;
[3]	pfd_phase_sel	1	0	Swaps the PFD inputs 1 negative VCO tuning slope 0 positive VCO tuning slope
[4]	pfd_up_en	1	1	enables the PFD UP output according to state of pfd_mute_when_locked_enable, see *Reg0B<9>*
[5]	pfd_dn_en	1	1	enables the PFD DN output according to state of pfd_mute_when_locked_enable, see *Reg0B<9>*
[6]	pfd_LD_opEn	1	1	pfd Lock Detect Output Enable, enables Lock Detect flag output to LD_SDO pin
[7]	pfd_pullup_ctrl	1	0	Forces PFD UP output on
[8]	pfd_puldn_ctrl	1	0	Forces PFD DN output on
[9]	pfd_mute_when_locked_ enable	1	0	1: if set: when locked disables UP if pfd_up_en=0 when locked disables DN if pfd_dn_en=0 when NOT locked, allows both UP and DN to be active and ignores pdf_up_en and pfd_dn_en 0: if clear, pfd_dn_en and pfd_up_en enable UP and DN outputs at all times
[10]	spare0	1	0	reserved
[11]	spare1	1	1	reserved

Table 19. Reg 0Ch VCO SPI Register

Bit	Name	Width	Default	Description
[9:0]	vcospi_vco_data	10	0	data register contents, when written automatically outputs this data via VCO SPI when to_gpo_sdo=1 *Reg09<7>*

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Table 20. Reg 0Dh GPO_SPI_RDIV Register

Bit	Name	Width	Default	Description
[3:0]	gpo_select	4	10d	Test signals selected here are output to gpo pins when *gpo_pads_en=1* (Table 15) D1 & D0 0: clk_vcodiv & clk_refdiv 1: pfd_up & pfd_dn 2: refOut & refDivOut 3: seed_stb_sypulse_test & frac_stb_sypulse_test 4: intg_inbuff_enable_test & clk_sd 5: oneshot_trigg_test & oneshot_pulse_test 6: '0' & ringosc_test 7: csp_corr_add & csp_corr_sub 8: pfd_sat_refdiv & pfd_sat_vcodiv 9: (csp_corr_add or csp_corr_sub) & pfd_sat_rstb 10: gpo_test , see Reg0D<5:4> 11: not used 12: not used 13: not used 14: not used 15: not used
[5:4]	gpo_test	2	0	data written to this register is output to D0 and D1 pins when gpo_select = 10d
[6]	refclkdiv4	1	0	1: sel ref divby4 for clocking the vco_spi 0: sel ref divby1 for clocking the vco_spi
[7]	to_gpo_sdo	1	0	enable the automatic output of vcospi_vco_data to LD_SDO Output VCO_SPI clock to D1 (see *Reg0D<6>*) Output VCO_SPI EN to D0

Table 21. Reg 0Fh LD State Register (Read Only)

Bit	Name	Width	Default	Description
[0]	locked	1	0	Read only Lock Detect flag, 1 when locked

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HMC700LP4 / 700LP4E

v11.0411

8 GHz 16-Bit Fractional-N PLL

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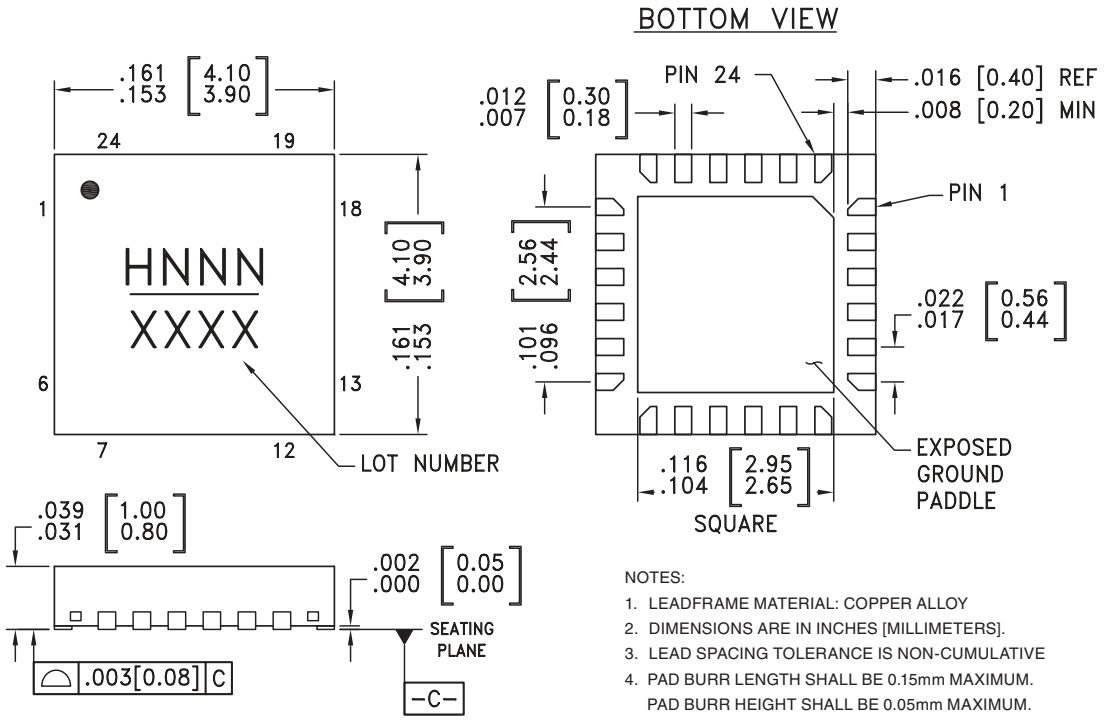
Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC700LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H700 XXXX
HMC700LP4(E)	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H700 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

Evaluation PCB

Please reference HMC700LP4 Product Note for information on Evaluation PCB kit and List of Materials.

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