

OPA241
OPA2241
OPA4241
OPA251
OPA2251
OPA4251

Single-Supply, *MicroPOWER* OPERATIONAL AMPLIFIERS

OPA241 Family optimized for +5V supply.

OPA251 Family optimized for $\pm 15V$ supply.

FEATURES

- **MicroPOWER:** $I_Q = 25\mu A$
- **SINGLE-SUPPLY OPERATION**
- **RAIL-TO-RAIL OUTPUT (within 50mV)**
- **WIDE SUPPLY RANGE**
 Single Supply: +2.7V to +36V
 Dual Supply: $\pm 1.35V$ to $\pm 18V$
- **LOW OFFSET VOLTAGE:** $\pm 250\mu V$ max
- **HIGH COMMON-MODE REJECTION:** 124dB
- **HIGH OPEN-LOOP GAIN:** 128dB
- **SINGLE, DUAL, AND QUAD**

APPLICATIONS

- **BATTERY OPERATED INSTRUMENTS**
- **PORTABLE DEVICES**
- **MEDICAL INSTRUMENTS**
- **TEST EQUIPMENT**

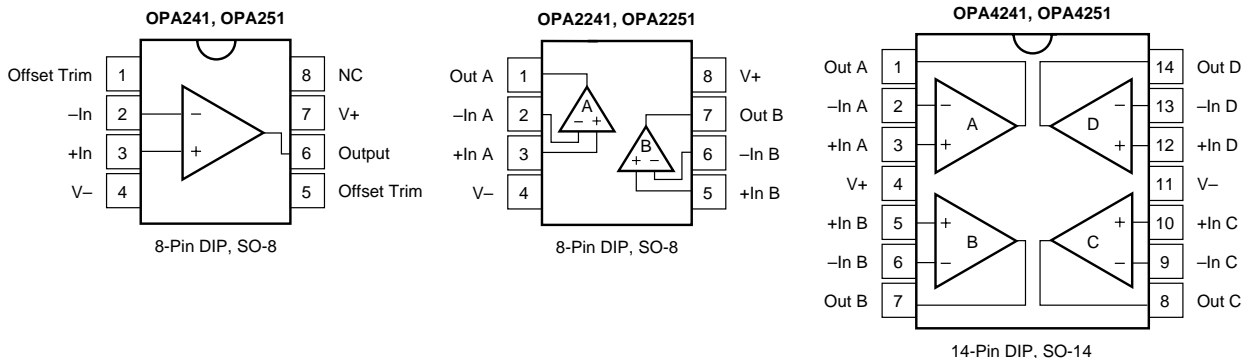
DESCRIPTION

The OPA241 series and OPA251 series are specifically designed for battery powered, portable applications. In addition to very low power consumption ($25\mu A$), these amplifiers feature low offset voltage, rail-to-rail output swing, high common-mode rejection, and high open-loop gain.

The OPA241 series is optimized for operation at low power supply voltage while the OPA251 series is optimized for high power supplies. Both can operate from either single (+2.7V to +36V) or dual supplies ($\pm 1.35V$ to $\pm 18V$). The input common-mode voltage range extends 200mV below the negative supply—ideal for single-supply applications.

They are unity-gain stable and can drive large capacitive loads. Special design considerations assure that these products are easy to use. High performance is maintained as the amplifiers swing to their specified limits. Because the initial offset voltage ($\pm 250\mu V$ max) is so low, user adjustment is usually not required. However, external trim pins are provided for special applications (single versions only).

The OPA241 and OPA251 (single versions) are available in standard 8-pin DIP and SO-8 surface-mount packages. The OPA2241 and OPA2251 (dual versions) come in 8-pin DIP and SO-8 surface-mount packages. The OPA4241 and OPA4251 (quad versions) are available in 14-pin DIP and SO-14 surface-mount packages. All are fully specified from $-40^\circ C$ to $+85^\circ C$ and operate from $-55^\circ C$ to $+125^\circ C$.



SPECIFICATIONS: $V_S = 2.7V$ to $5V$

At $T_A = +25^\circ C$, $R_L = 100k\Omega$ connected to $V_S/2$, unless otherwise noted.

Boldface limits apply over the specified temperature range, $T_A = -40^\circ C$ to $+85^\circ C$.

PARAMETER	CONDITION	OPA241UA, PA OPA2241UA, PA OPA4241UA, PA			OPA251UA, PA OPA2251UA, PA OPA4251UA, PA			UNITS
		MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
OFFSET VOLTAGE Input Offset Voltage V_{OS} $T_A = -40^\circ C$ to $+85^\circ C$ vs Temperature dV_{OS}/dT vs Power Supply PSRR $T_A = -40^\circ C$ to $+85^\circ C$ Channel Separation (dual, quad)	$T_A = -40^\circ C$ to $+85^\circ C$ $V_S = 2.7V$ to $36V$ $V_S = 2.7V$ to $36V$		± 50 ± 100 ± 0.4 3 0.3	± 250 ± 400 30 30		± 100 ± 130 ± 0.6 * *	* *	μV μV $\mu V/^\circ C$ $\mu V/V$ $\mu V/V$
INPUT BIAS CURRENT Input Bias Current ⁽²⁾ I_B $T_A = -40^\circ C$ to $+85^\circ C$ Input Offset Current I_{OS} $T_A = -40^\circ C$ to $+85^\circ C$			-4 ± 0.1	-20 -25 ± 2 ± 2		* *		nA nA nA nA
NOISE Input Voltage Noise, $f = 0.1Hz$ to $10Hz$ Input Voltage Noise Density, $f = 1kHz$ e_n Current Noise Density, $f = 1kHz$ i_n			1 45 40			* * *		$\mu Vp-p$ nV/\sqrt{Hz} fA/\sqrt{Hz}
INPUT VOLTAGE RANGE Common-Mode Voltage Range V_{CM} Common-Mode Rejection Ratio CMRR $T_A = -40^\circ C$ to $+85^\circ C$	$V_{CM} = -0.2V$ to $(V+) - 0.8V$ $V_{CM} = 0V$ to $(V+) - 0.8V$	-0.2 80 80	106	$(V+) - 0.8$		*		V dB dB
INPUT IMPEDANCE Differential Common-Mode			$10^7 \parallel 2$ $10^9 \parallel 4$			* *		$\Omega \parallel pF$ $\Omega \parallel pF$
OPEN-LOOP GAIN Open-Loop Voltage Gain A_{OL} $T_A = -40^\circ C$ to $+85^\circ C$	$R_L = 100k\Omega$, $V_O = (V-) + 100mV$ to $(V+) - 100mV$ $R_L = 100k\Omega$, $V_O = (V-) + 100mV$ to $(V+) - 100mV$ $R_L = 10k\Omega$, $V_O = (V-) + 200mV$ to $(V+) - 200mV$ $R_L = 10k\Omega$, $V_O = (V-) + 200mV$ to $(V+) - 200mV$	100 100 100 100	120 120			* *		dB dB dB dB
FREQUENCY RESPONSE Gain-Bandwidth Product GBW Slew Rate SR Overload Recovery Time	$V_S = 5V$, $G = 1$ $V_{IN} \cdot G = V_S$		35 0.01 60			* * *		kHz V/ μs μs
OUTPUT Voltage Output Swing from Rail ⁽³⁾ V_O $T_A = -40^\circ C$ to $+85^\circ C$ $T_A = -40^\circ C$ to $+85^\circ C$ Short-Circuit Current I_{SC} Single Versions Dual, Quad Versions Capacitive Load Drive C_{LOAD}	$R_L = 100k\Omega$ to $V_S/2$, $A_{OL} \geq 70dB$ $R_L = 100k\Omega$ to $V_S/2$, $A_{OL} \geq 100dB$ $R_L = 100k\Omega$ to $V_S/2$, $A_{OL} \geq 100dB$ $R_L = 10k\Omega$ to $V_S/2$, $A_{OL} \geq 100dB$ $R_L = 10k\Omega$ to $V_S/2$, $A_{OL} \geq 100dB$		50 75 100	100 100 200 200		* * *		mV mV mV mV
POWER SUPPLY Specified Voltage Range V_S Operating Voltage Range Quiescent Current (per amplifier) I_Q $T_A = -40^\circ C$ to $+85^\circ C$	$T_A = -40^\circ C$ to $+85^\circ C$ $I_O = 0$ $I_O = 0$	+2.7	+2.7 to +5 ± 25	+36 ± 30 ± 36	*	* *	*	V V μA μA
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance θ_{JA} 8-Pin DIP SO-8 Surface Mount 14-Pin DIP SO-14 Surface Mount		-40 -55 -55		+85 +125 +125	* * *		* * *	$^\circ C$ $^\circ C$ $^\circ C$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$

* Specifications the same as OPA241UA, PA.

NOTES: (1) $V_S = +5V$. (2) The negative sign indicates input bias current flows out of the input terminals. (3) Output voltage swings are measured between the output and power supply rails.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

SPECIFICATIONS: $V_S = \pm 15V$

At $T_A = +25^\circ C$, $R_L = 100k\Omega$ connected to ground, unless otherwise noted.

Boldface limits apply over the specified temperature range, $T_A = -40^\circ C$ to $+85^\circ C$.

PARAMETER	CONDITION	OPA241UA, PA OPA2241UA, PA OPA4241UA, PA			OPA251UA, PA OPA2251UA, PA OPA4251UA, PA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage V_{OS} $T_A = -40^\circ C$ to $+85^\circ C$ vs Temperature dV_{OS}/dT vs Power Supply PSRR $T_A = -40^\circ C$ to $+85^\circ C$ Channel Separation (dual, quad)	$T_A = -40^\circ C$ to $+85^\circ C$ $V_S = \pm 1.35V$ to $\pm 18V$ $V_S = \pm 1.35V$ to $\pm 18V$		± 100 ± 150 ± 0.6 * *			± 50 ± 100 ± 0.5 3 0.3	± 250 ± 300 30 30	μV μV $\mu V/^\circ C$ $\mu V/V$ $\mu V/V$
INPUT BIAS CURRENT Input Bias Current ⁽¹⁾ I_B $T_A = -40^\circ C$ to $+85^\circ C$ Input Offset Current I_{OS} $T_A = -40^\circ C$ to $+85^\circ C$			*			-4 ± 0.1	-20 ± 2	nA nA nA
NOISE Input Voltage Noise, $f = 0.1Hz$ to $10Hz$ Input Voltage Noise Density, $f = 1kHz$ e_n Current Noise Density, $f = 1kHz$ i_n			*			1 45 40		$\mu Vp-p$ nV/\sqrt{Hz} fA/\sqrt{Hz}
INPUT VOLTAGE RANGE Common-Mode Voltage Range V_{CM} Common-Mode Rejection Ratio CMRR $T_A = -40^\circ C$ to $+85^\circ C$	$V_{CM} = -15.2V$ to $14.2V$ $V_{CM} = -15V$ to $14.2V$		*		(V-) -0.2 100 100	124	(V+) -0.8	V dB dB
INPUT IMPEDANCE Differential Common-Mode			*			$10^7 \parallel 2$ $10^9 \parallel 4$		$\Omega \parallel pF$ $\Omega \parallel pF$
OPEN-LOOP GAIN Open-Loop Voltage Gain A_{OL} $T_A = -40^\circ C$ to $+85^\circ C$ $T_A = -40^\circ C$ to $+85^\circ C$	$R_L = 100k\Omega$, $V_O = -14.75V$ to $+14.75V$ $R_L = 100k\Omega$, $V_O = -14.75V$ to $+14.75V$ $R_L = 20k\Omega$, $V_O = -14.7V$ to $+14.7V$ $R_L = 20k\Omega$, $V_O = -14.7V$ to $+14.7V$		*		100 100 100 100	128 128		dB dB dB dB
FREQUENCY RESPONSE Gain-Bandwidth Product GBW Slew Rate SR Overload Recovery Time	$G = 1$ $V_{IN} \cdot G = V_S$		*			35 0.01 60		kHz V/ μs μs
OUTPUT Voltage Output Swing from Rail ⁽²⁾ V_O $T_A = -40^\circ C$ to $+85^\circ C$ $T_A = -40^\circ C$ to $+85^\circ C$ Short-Circuit Current I_{SC} Single Versions Dual Versions Capacitive Load Drive C_{LOAD}	$R_L = 100k\Omega$, $A_{OL} \geq 70dB$ $R_L = 100k\Omega$, $A_{OL} \geq 100dB$ $R_L = 100k\Omega$, $A_{OL} \geq 100dB$ $R_L = 20k\Omega$, $A_{OL} \geq 100dB$ $R_L = 20k\Omega$, $A_{OL} \geq 100dB$		*			50 75 100	250 250 300 300	mV mV mV mV mA mA
POWER SUPPLY Specified Voltage Range V_S Operating Voltage Range Quiescent Current (per amplifier) I_Q $T_A = -40^\circ C$ to $+85^\circ C$	$T_A = -40^\circ C$ to $+85^\circ C$ $I_Q = 0$ $I_Q = 0$		*	*	± 1.35	± 15 ± 27	± 18 ± 38 ± 45	V V μA μA
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance θ_{JA} 8-Pin DIP SO-8 Surface Mount 14-Pin DIP SO-14 Surface Mount			*	*	-40 -55 -55		+85 +125 +125	$^\circ C$ $^\circ C$ $^\circ C$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$

* Specifications the same as OPA251UA, PA.

NOTES: (1) The negative sign indicates input bias current flows out of the input terminals. (2) Output voltage swings are measured between the output and power supply rails.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage, V+ to V-	36V
Input Voltage ⁽²⁾	(V-) -0.5V to (V+) +0.5V
Output Short Circuit to Ground ⁽³⁾	Continuous
Operating Temperature	-55°C to +125°C
Storage Temperature	-55°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTES: (1) Stresses above these ratings may cause permanent damage.
 (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 5mA or less. (3) One amplifier per package.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

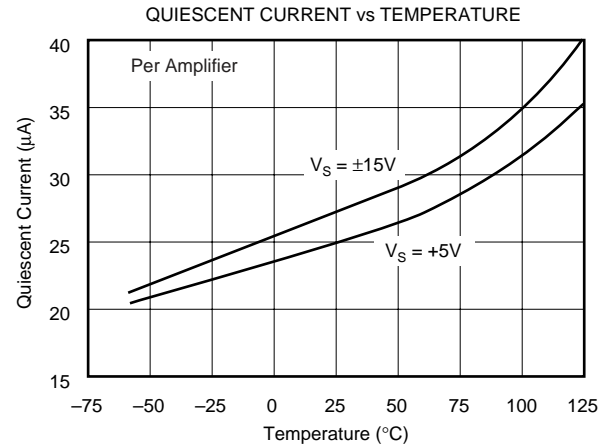
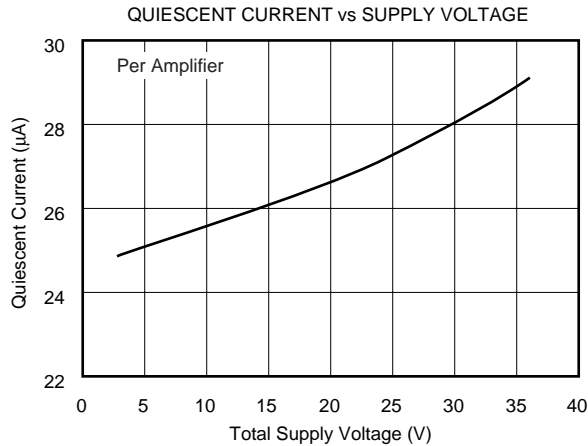
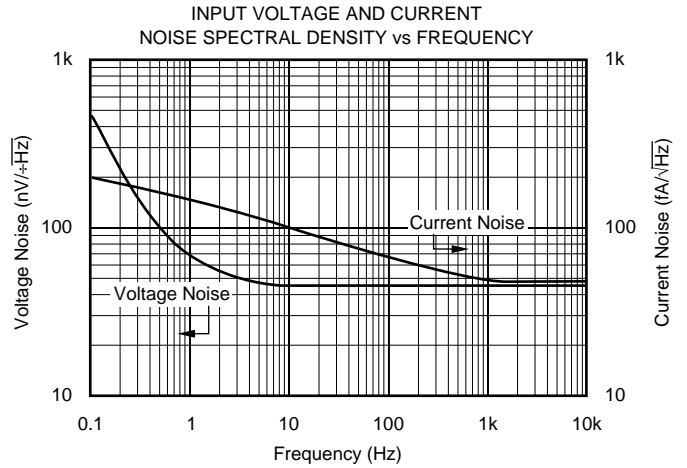
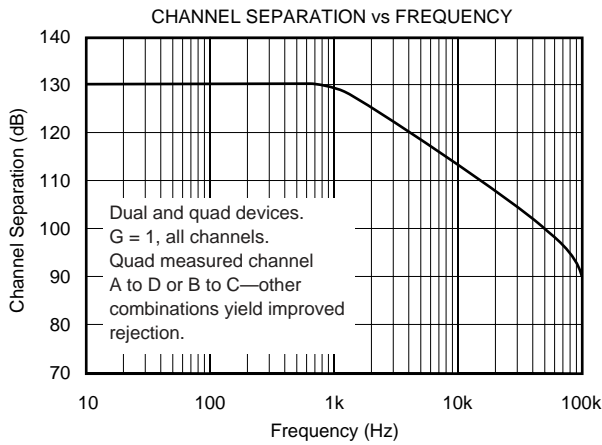
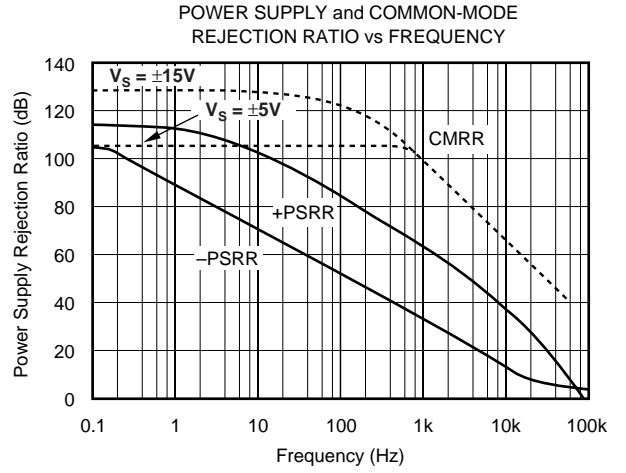
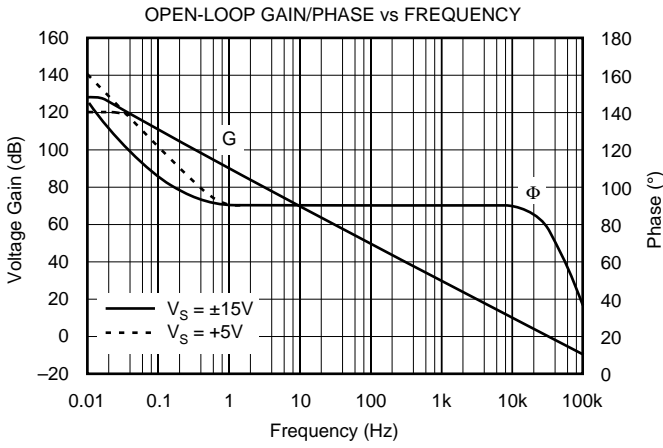
PRODUCT	SPECIFIED VOLTAGE	OPERATING VOLTAGE RANGE	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	SPECIFICATION TEMPERATURE RANGE
OPA241 SERIES					
Single					
OPA241PA	2.7V to 5V	2.7V to 36V	8-Pin DIP	006	-40°C to +85°C
OPA241UA	2.7V to 5V	2.7V to 36V	SO-8 Surface Mount	182	-40°C to +85°C
Dual					
OPA2241PA	2.7V to 5V	2.7V to 36V	8-Pin DIP	006	-40°C to +85°C
OPA2241UA	2.7V to 5V	2.7V to 36V	SO-8 Surface Mount	182	-40°C to +85°C
Quad					
OPA4241PA	2.7V to 5V	2.7V to 36V	14-Pin DIP	010	-40°C to +85°C
OPA4241UA	2.7V to 5V	2.7V to 36V	SO-14 Surface Mount	235	-40°C to +85°C
OPA251 SERIES					
Single					
OPA251PA	±15V	2.7V to 36V	8-Pin DIP	006	-40°C to +85°C
OPA251UA	±15V	2.7V to 36V	SO-8 Surface Mount	182	-40°C to +85°C
Dual					
OPA2251PA	±15V	2.7V to 36V	8-Pin DIP	006	-40°C to +85°C
OPA2251UA	±15V	2.7V to 36V	SO-8 Surface Mount	182	-40°C to +85°C
Quad					
OPA4251PA	±15V	2.7V to 36V	14-Pin DIP	010	-40°C to +85°C
OPA4251UA	±15V	2.7V to 36V	SO-14 Surface Mount	235	-40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, and $R_L = 100\text{k}\Omega$ connected to $V_S/2$ (ground for $V_S = \pm 15\text{V}$), unless otherwise noted.

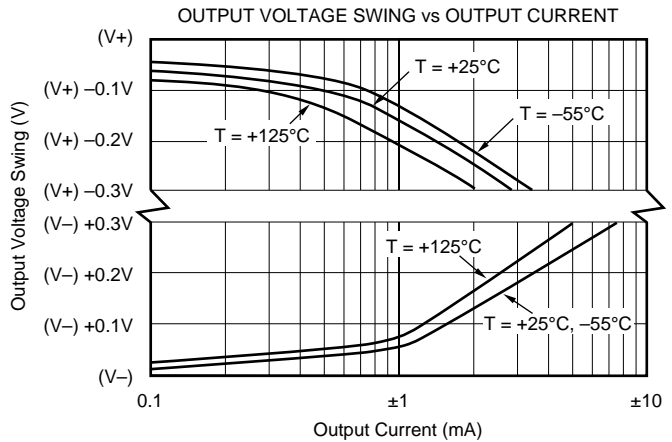
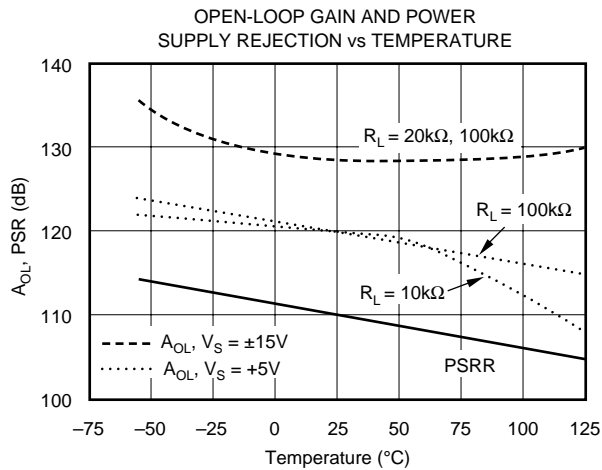
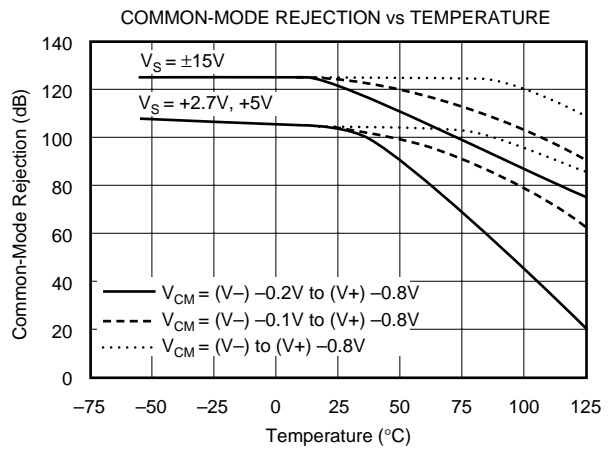
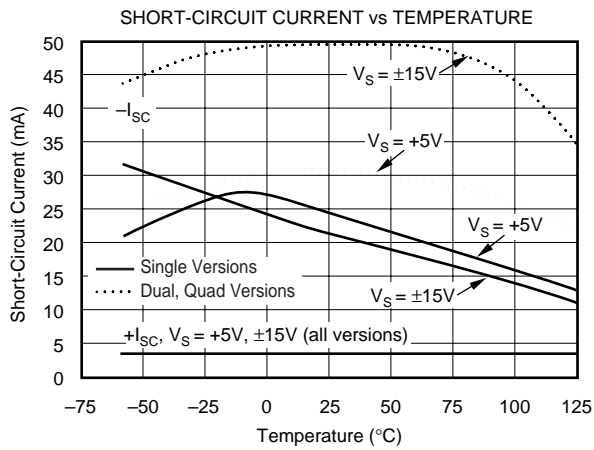
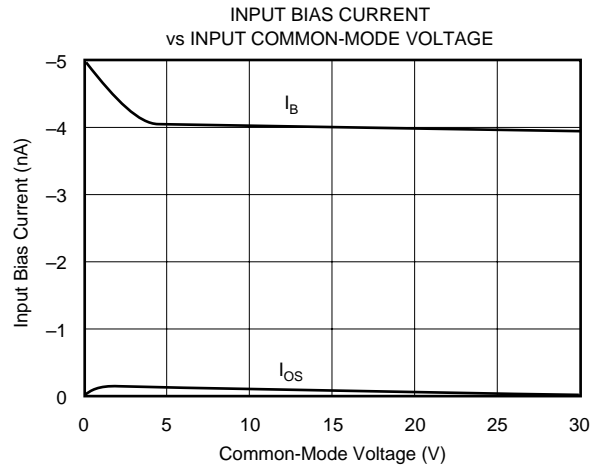
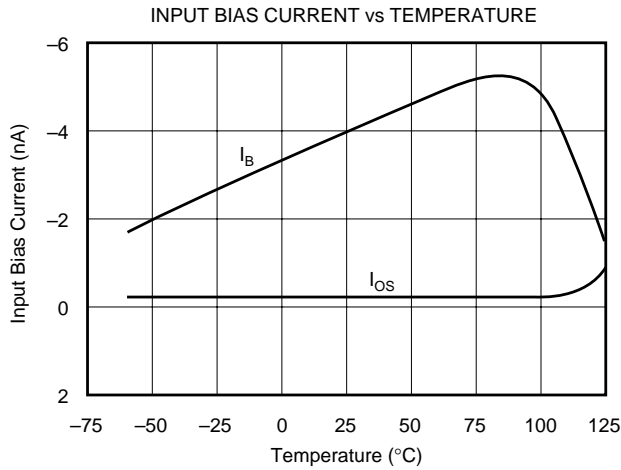
Curves apply to OPA241 and OPA251 unless specified.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, and $R_L = 100\text{k}\Omega$ connected to $V_S/2$ (ground for $V_S = \pm 15\text{V}$), unless otherwise noted.

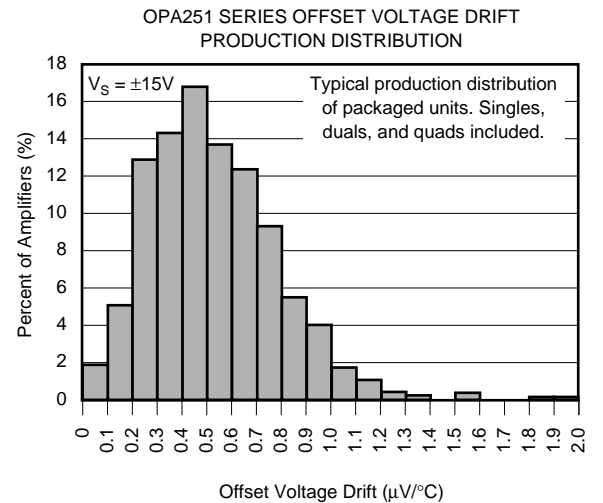
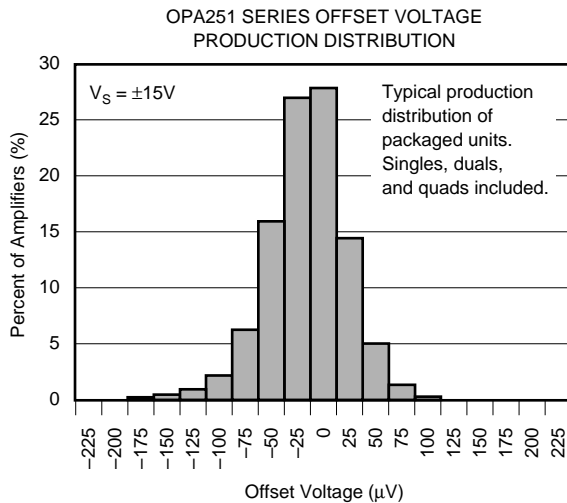
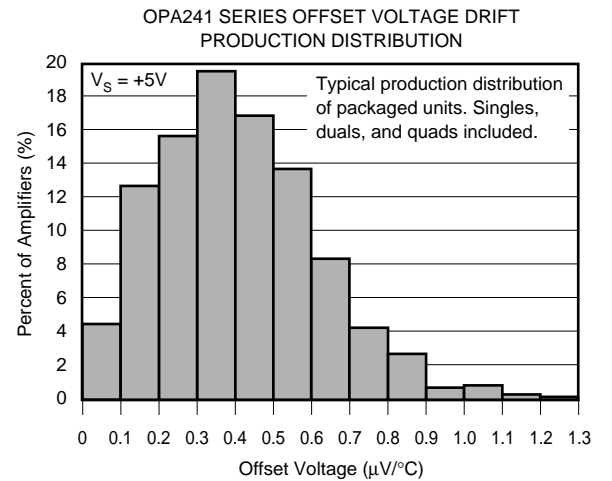
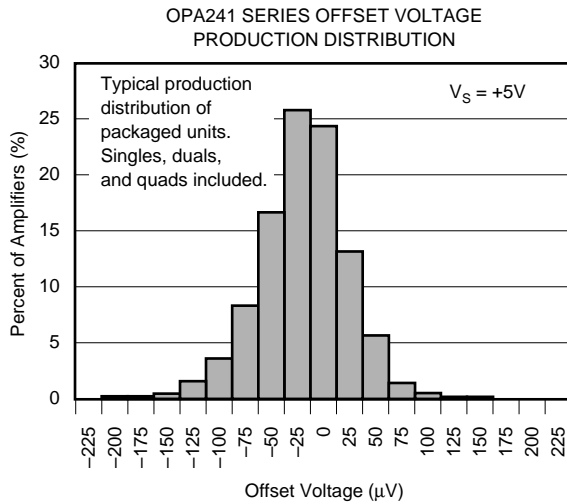
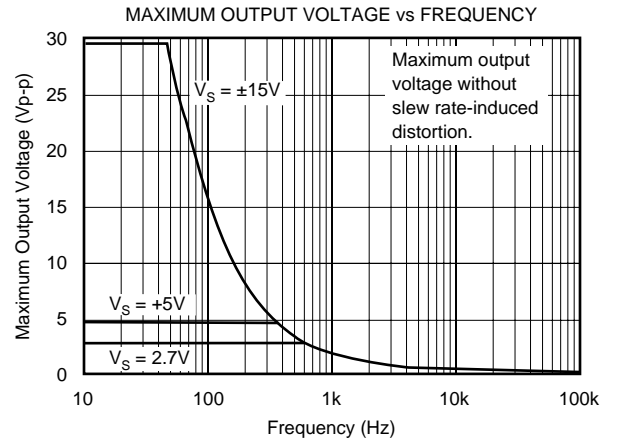
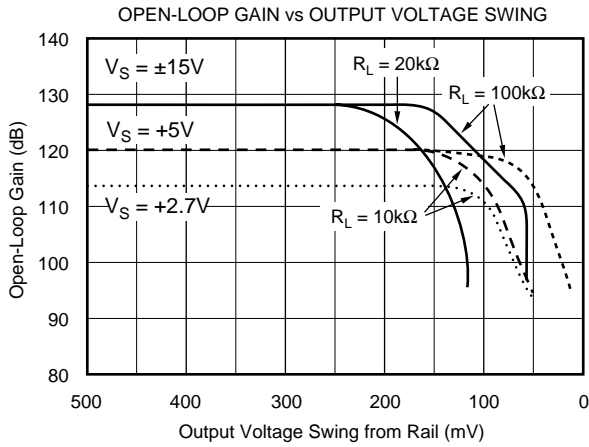
Curves apply to OPA241 and OPA251 unless specified.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, and $R_L = 100\text{k}\Omega$ connected to $V_S/2$ (ground for $V_S = \pm 15\text{V}$), unless otherwise noted.

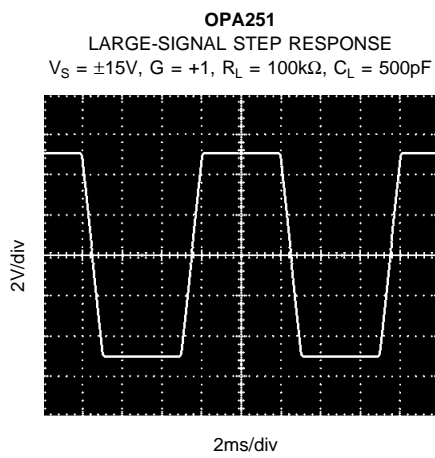
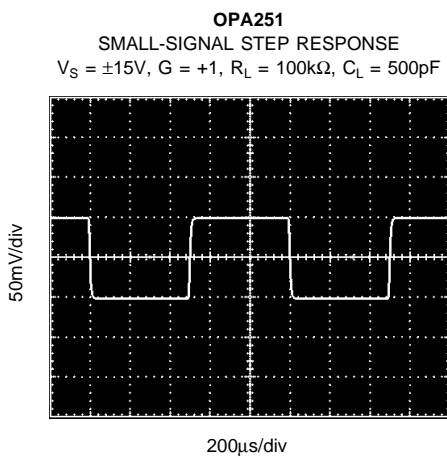
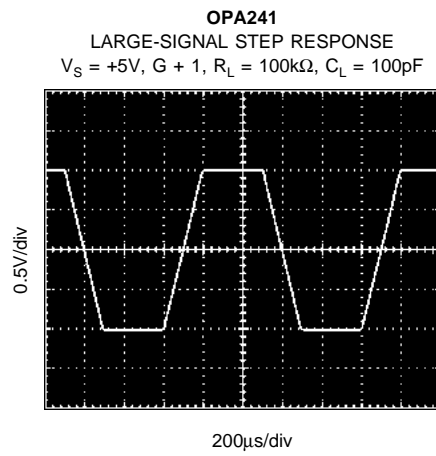
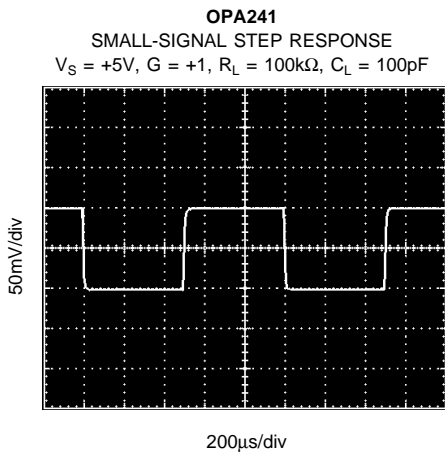
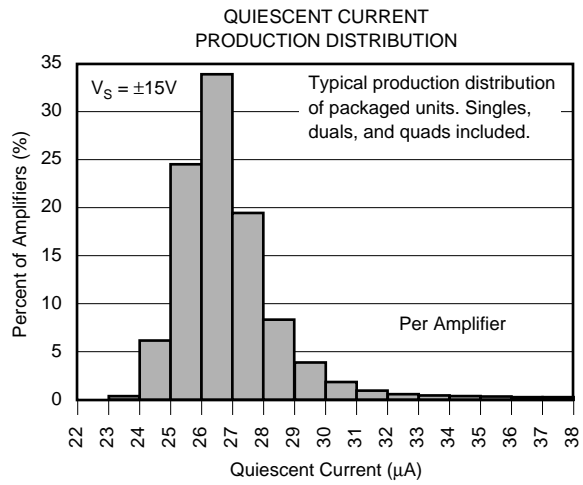
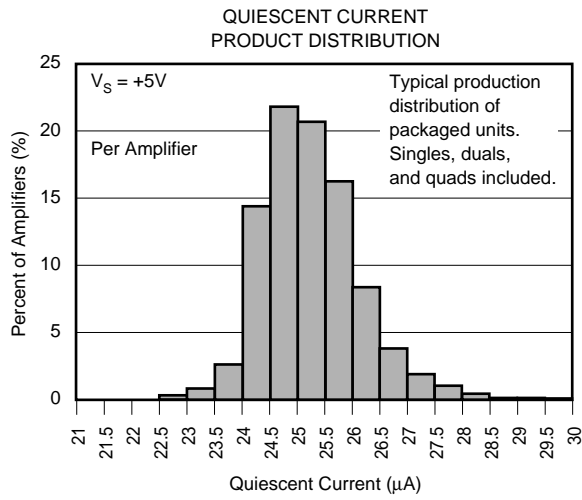
Curves apply to OPA241 and OPA251 unless specified.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, and $R_L = 100\text{k}\Omega$ connected to $V_S/2$ (ground for $V_S \pm 15\text{V}$), unless otherwise noted.

Curves apply to OPA241 and OPA251 unless specified.



APPLICATIONS INFORMATION

The OPA241 and OPA251 series are unity-gain stable and suitable for a wide range of general purpose applications. Power supply pins should be bypassed with 0.01μF ceramic capacitors.

OPERATING VOLTAGE

The OPA241 series is laser-trimmed for low offset voltage and drift at low supply voltage ($V_S = +5V$). The OPA251 series is trimmed for $\pm 15V$ operation. Both products operate over the full voltage range (+2.7V to +36V or $\pm 1.35V$ to $\pm 18V$) with some compromises in offset voltage and drift performance. However, all other parameters have similar performance. Key parameters are guaranteed over the specified temperature range, $-40^\circ C$ to $+85^\circ C$. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage or temperature are shown in typical performance curves.

OFFSET VOLTAGE TRIM

As mentioned previously, offset voltage of the OPA241 series is laser-trimmed at +5V. The OPA251 series is trimmed at $\pm 15V$. Because the initial offset is so low, user adjustment is usually not required. However, the OPA241 and OPA251 (single op amp versions) provide offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset could degrade the offset drift behavior of the op amp. While it is not possible to predict the exact change in drift, the effect is usually small.

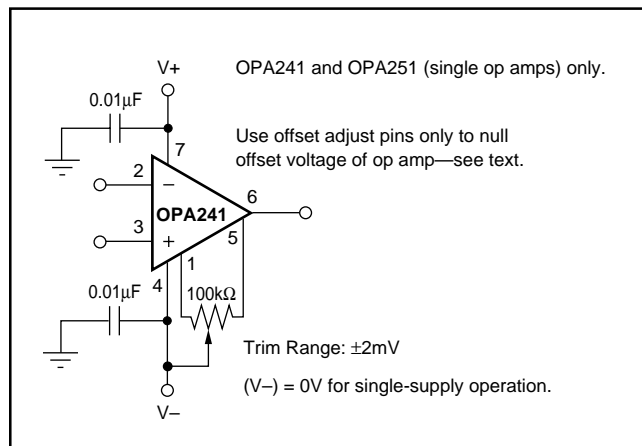


FIGURE 1. OPA241 and OPA251 Offset Voltage Trim Circuit.

CAPACITIVE LOAD AND STABILITY

The OPA241 series and OPA251 series can drive a wide range of capacitive loads. However, all op amps under certain conditions may be unstable. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability.

Figures 2 and 3 show the regions where the OPA241 series and OPA251 series have the potential for instability. As shown, the unity gain configuration with low supplies is the most susceptible to the effects of capacitive load. With $V_S = +5V$, $G = +1$, and $I_{OUT} = 0$, operation remains stable with load capacitance up to approximately 200pF. Increasing supply voltage, output current, and/or gain significantly improves capacitive load drive. For example, increasing the supplies to $\pm 15V$ and gain to 10 allows approximately 2700pF to be driven.

One method of improving capacitive load drive in the unity gain configuration is to insert a resistor inside the feedback loop as shown in Figure 4. This reduces ringing with large capacitive loads while maintaining dc accuracy. For example, with $V_S = \pm 1.35V$ and $R_S = 5k\Omega$, the OPA241 series and OPA251 series perform well with capacitive loads in excess of 1000pF. Without the series resistor, capacitive load drive is typically 200pF for these conditions. However, this method will result in a slight reduction of output voltage swing.

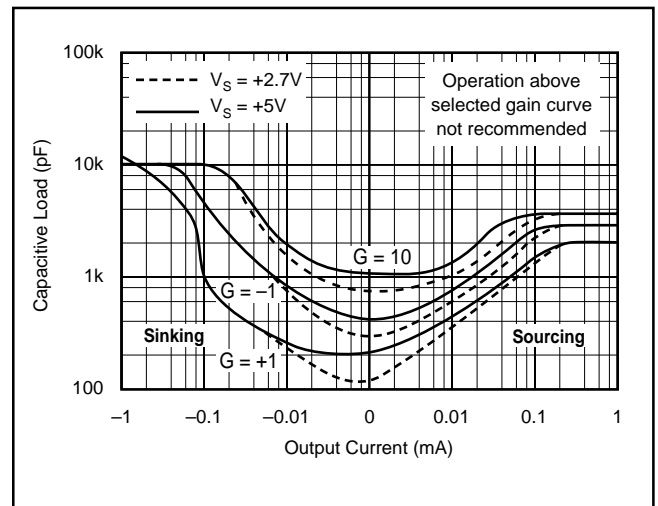


FIGURE 2. Stability—Capacitive Load versus Output Current for Low Supply Voltage.

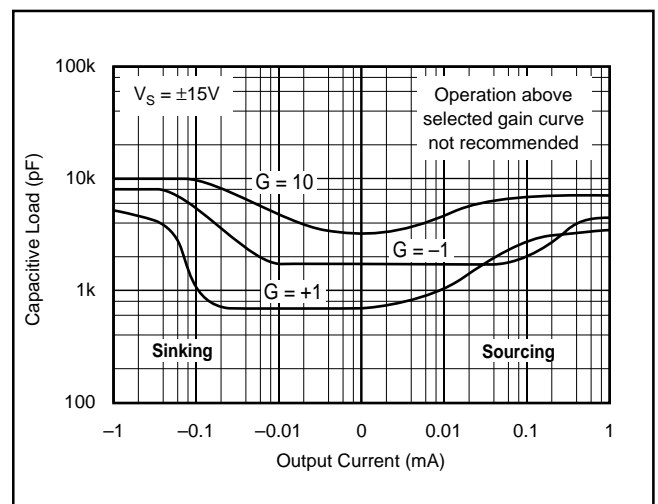


FIGURE 3. Stability—Capacitive Load versus Output Current for $\pm 15V$ Supplies.

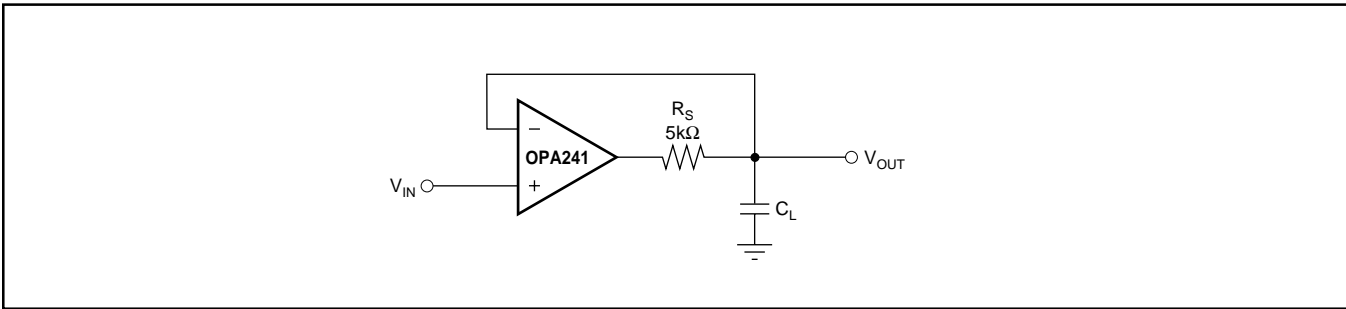


FIGURE 4. Series Resistor in Unity Gain Configuration Improves Capacitive Load Drive.

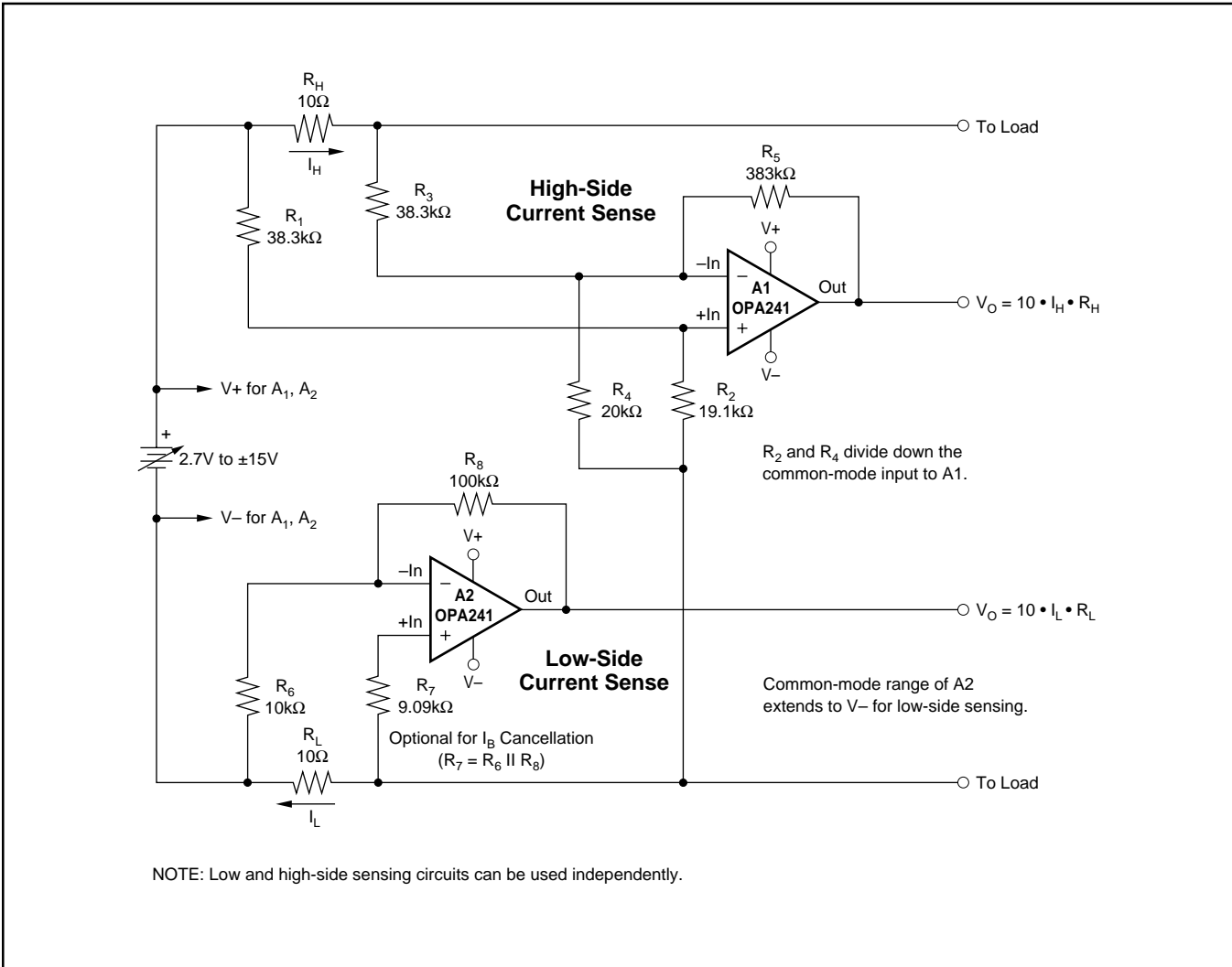


FIGURE 5. Low and High-Side Battery Current Sensing.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2241PA	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA2241PA	Samples
OPA2241PAG4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA2241PA	Samples
OPA2241UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2241UA	Samples
OPA2241UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2241UA	Samples
OPA2241UAG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2241UA	Samples
OPA2251PA	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA2251PA	Samples
OPA2251PAG4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA2251PA	Samples
OPA2251UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2251UA	Samples
OPA2251UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2251UA	Samples
OPA2251UAG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2251UA	Samples
OPA241PA	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		OPA241PA	Samples
OPA241UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 241UA	Samples
OPA241UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 241UA	Samples
OPA241UAG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 241UA	Samples
OPA251UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 251UA	Samples
OPA251UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 251UA	Samples
OPA4241PA	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA4241PA	Samples
OPA4241UA	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4241UA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4241UA/2K5	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4241UA	Samples
OPA4251UA	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4251UA	Samples
OPA4251UA/2K5	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4251UA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

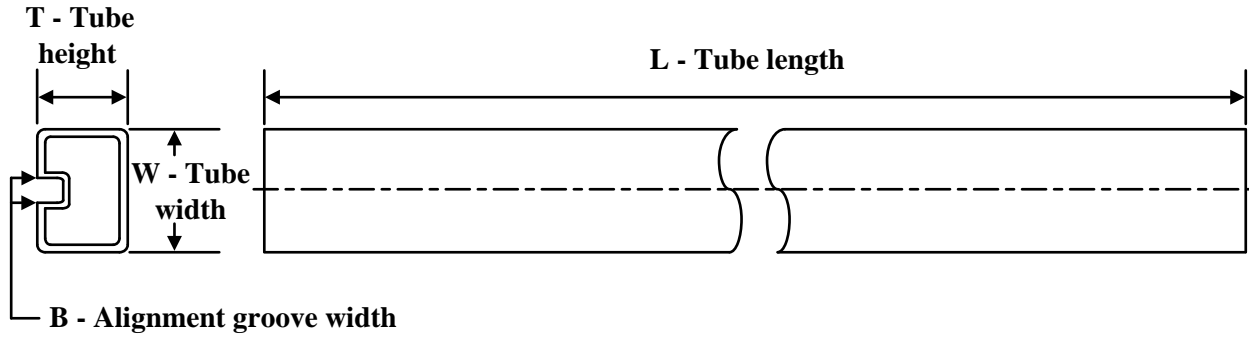

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2241UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2251UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA241UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA251UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4241UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4251UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2241UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA2251UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA241UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA251UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA4241UA/2K5	SOIC	D	14	2500	356.0	356.0	35.0
OPA4251UA/2K5	SOIC	D	14	2500	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA2241PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA2241PAG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA2241UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2241UAG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA2251PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA2251PAG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA2251UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2251UAG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA241PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA241UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA241UAG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA251UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA4241PA	N	PDIP	14	25	506	13.97	11230	4.32
OPA4241UA	D	SOIC	14	50	506.6	8	3940	4.32
OPA4251UA	D	SOIC	14	50	506.6	8	3940	4.32

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

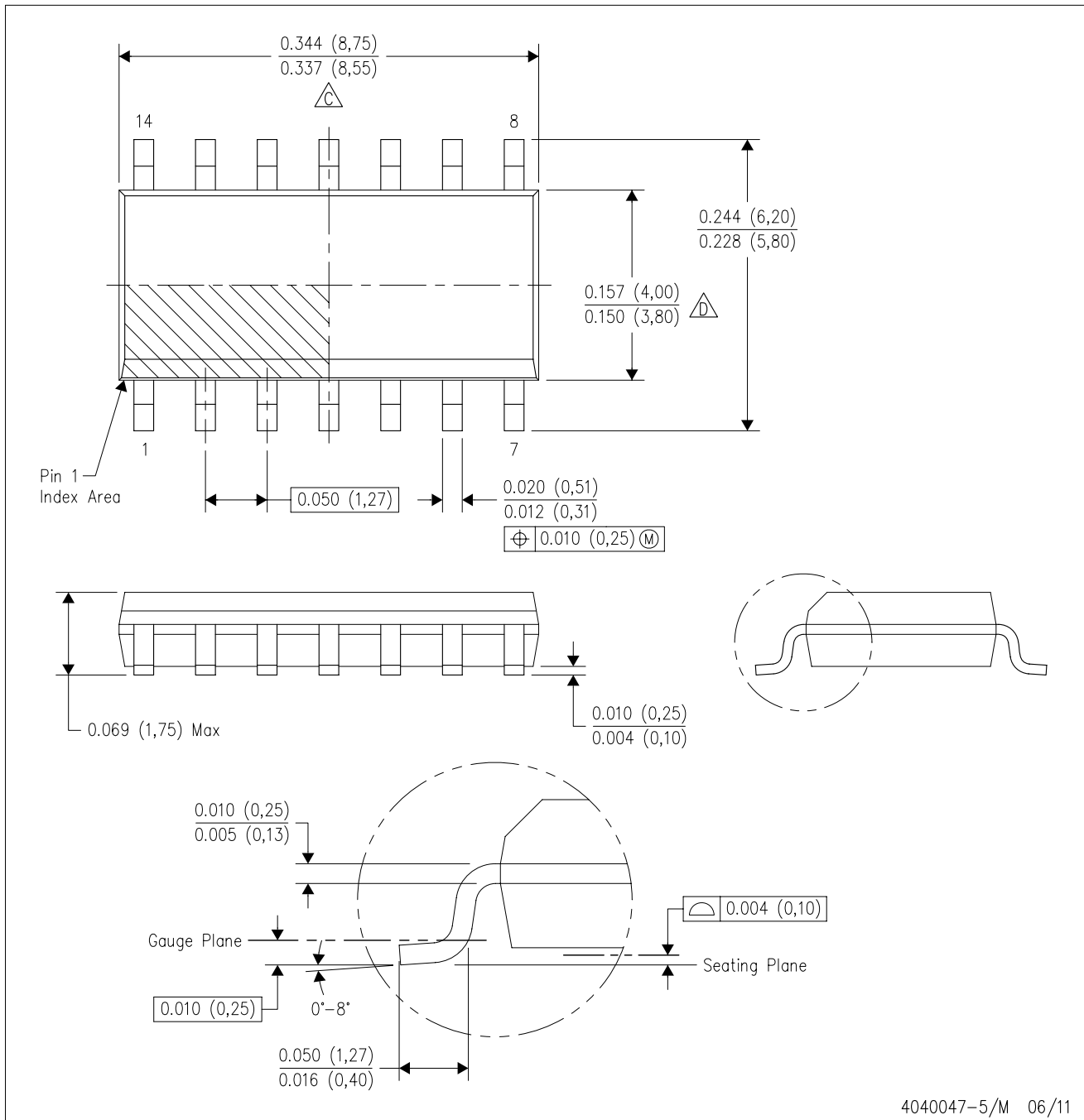
16 PINS SHOWN





- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

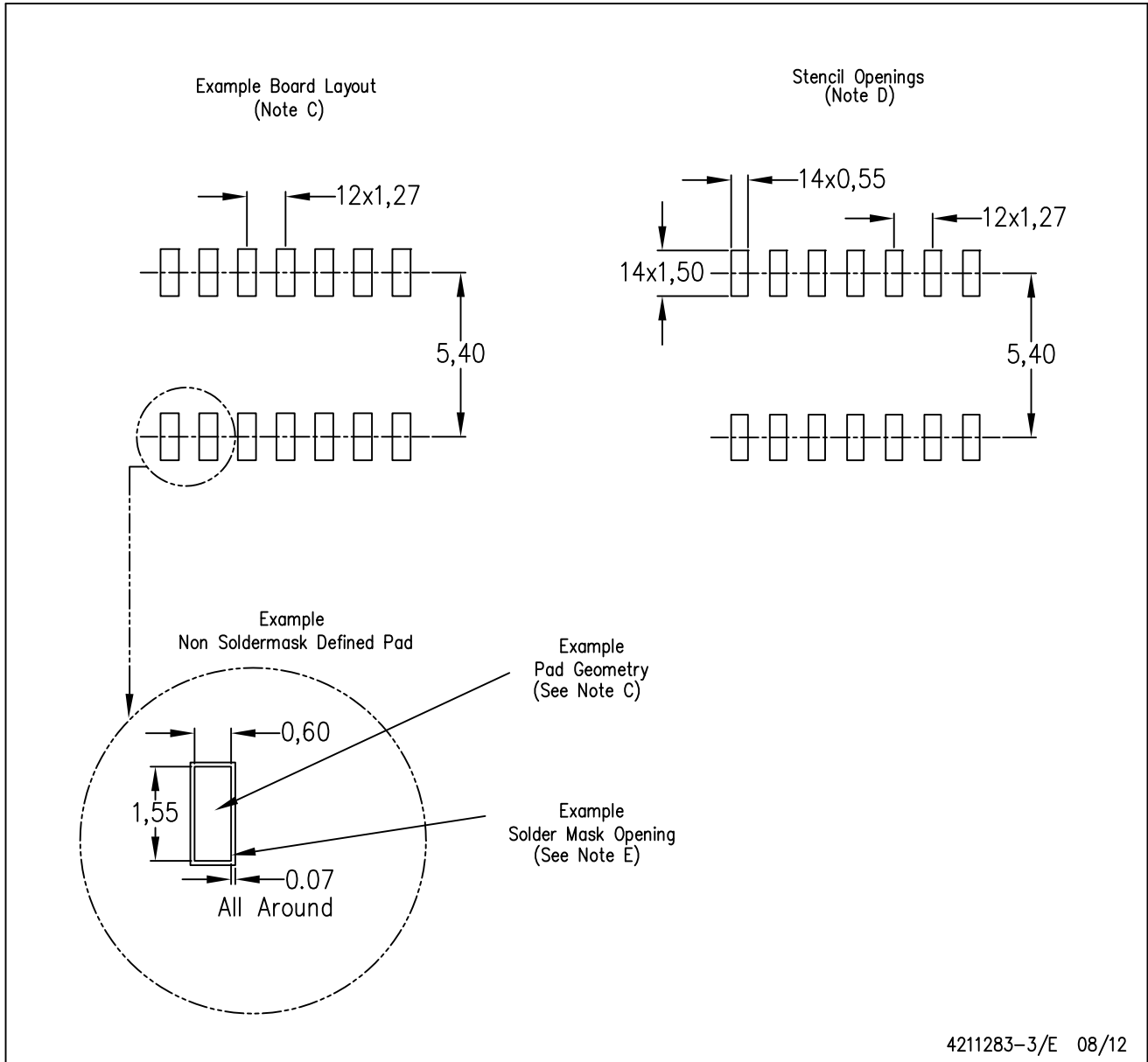
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D0008A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated