QUAZAR™ QPR8™ 1Gb (Quad Partition Rate)™ Memory

PRODUCT BRIEF: MSQ230 QPR8
(Quad Partition Rate)

Quad Partition Rate (QPR) Overview

The **QUAZAR Family of Memory** are high capacity, high-speed memory ICs that support high bandwidth, fast random memory access rates which solve critical memory access challenges for memory bottlenecked applications like network table search, statistics, buffering, security, firewall, 8k video, anomaly detection, genomics, AI and IoT.

The Quazar family is specifically designed to support the next generation of high-speed, low latency extremely high bandwidth random access memory applications. The QPR devices are x4 or x8 the capacity of the most common QDR SRAM devices which operate at approximately one eighth to one-quarter of the QPR bandwidth.

QUAZAR Family Target Goals

- Low Cost QDR alternative
- Provide high capacity
- Low tRC
- Higher bandwidth
- Lower power
- Simplified design effort
- System performance equal or better than a QDR
- *Costs significantly less than the equivalent cost of QDR components in required design time*
- Xilinx & Intel FPGA compatible

Base Features: QPR8

- 1 Gb memory single device
- High access rate SRAM class memory
- tRC 3.2 ns memory
- Up to 5 Billion transactions per second
- Two serial I/O ports (A & B) for random-access
- Replaces 8 QDR type memories
- MoSys supplies sample RTL Memory Controllers
- In a 27mm x27mm FCBGA

Application Focus

- FPGA Acceleration for Xilinx and Intel
- Ideal replacement for QDR
- SRAM with high capacity AND high speed
- High bandwidth data access application where low latency is critical
- Slower speed applications needing higher capacity single device now using SyncSRAMs

QPR (QUAD Partition Rate) Memory

- 4 independent partitions per I/O port
- Each partitions functions as a standalone random-access SRAM
- RTL controller selectable word width: up to x576b
- Bandwidth: Two Ports for higher bandwidth
  - Highest single chip bandwidth: Up to 640 Gb/s throughput (320 full duplex)
- Much lower power and less board space than the equivalent density QDR

Key Features: Few Pins / Signal Integrity

- Lower pin count and ease of PCB design
  - Highly efficient serial protocol
  - Reduction of I/O pins from QDR (close to 20x)
  - QPR8 typical system uses 32 pins
- Signal Auto-adaption feature
  - Eases board layout and signal integrity concerns
  - Operates over connectors
- Pin compatible with MoSys Blazar family of Bandwidth Engine (BE3) devices

MoSys Total Solution

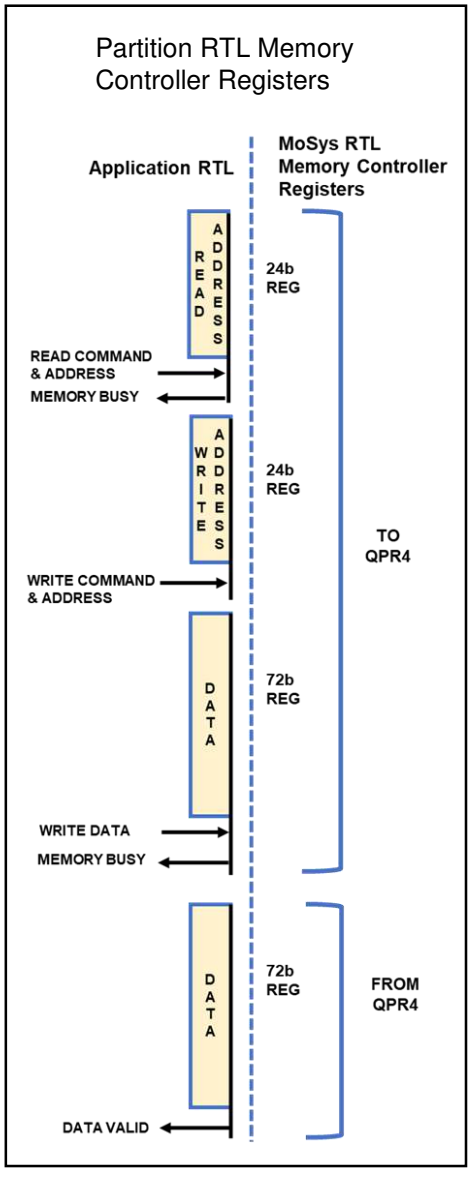
Data and information flow requires a System Memory Strategy that involves the trade offs of DRAM, SRAM and FPGA memory. It must be understood how the flow of data in and out of a memory affects performance.

Memory designs are a critical part of the system and not only decided at the component level. For memories, latency, density, access, and bandwidth, along with cost, are all key decision points.

How the memory will be accessed in the application and impact on the overall system performance, become critical factors.
The QUAZAR family was designed to take the best features of the QDR type devices and add capabilities to accelerate applications at the SYSTEM level.

QPR Total Solution

MoSys defined the QPR memory as a solution product, with the goal of providing a simple path to upgrade designs from QDR with higher capacity but with a less design effort and minimal impact on software.



Total QPR Solutions Have Three System Elements

1

- MoSys supplied RTL Memory Controller
  - QDR type RTL interface
  - Provides RTL register set for each partition
    - Instruction/Data registers to memory
    - Data registers from memory
  - Support user selectable work widths
    - Up to x576b
  - Controls the SerDes protocol (transparent to user)

2

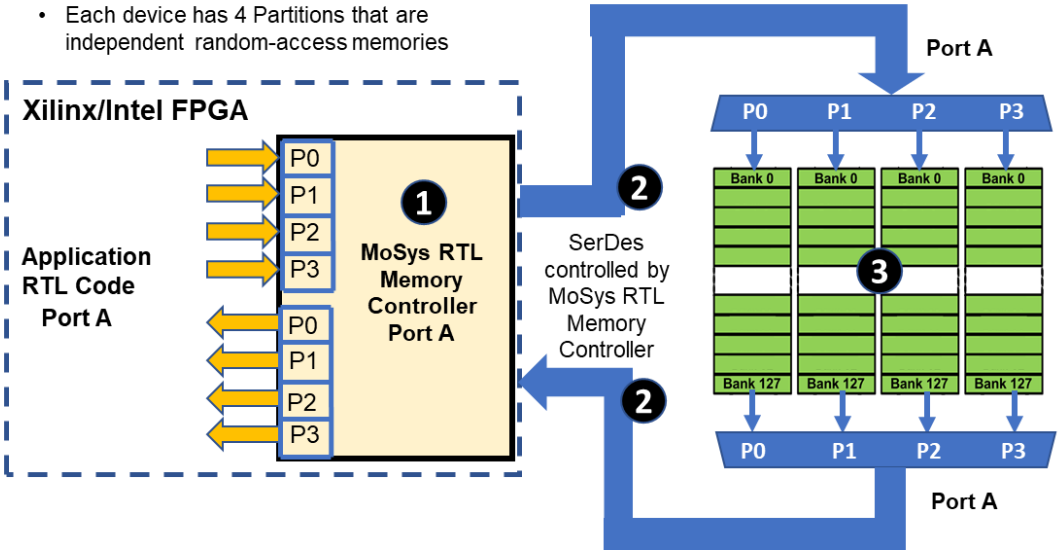
- SerDes high-speed Memory/FPGA interface
  - Most FPGAs have multiple SerDes lines
  - QPR8 device available with 15.5 Gb/s or 25 Gb/s
  - Preferred FPGA today and future interface direction
  - Lowest pin count interface…minimum of 16 FPGA pins

3

- QPR (Quad Partition Rate) memory Architecture
  - Memory architecture with Partitions divided into Banks
  - Each partition is accessed like an independent SRAM

QPR Memory Family has two memory configurations. See Product Brief for QPR4 for more information on the 567Mb device.

- MSQ220 QPR4 567Mb
- MSQ230 QPR8 1Gb
- Each device has 4 Partitions that are independent random-access memories



QPR4 Memory Modes of Operation

Overview of Operating Modes

Each partition operates as an independent Random-Access SRAMs. All of the partition are accessed each tRC clock cycle.

Bandwidth is determined by combining partition across multiple partitions. The QPR8 can achieve a maximum of 160 Gb/s Full Duplex with a 576b memory access width.

A selected MoSys RTL Memory Controller for the QPR4 provide for one of two modes of operation.

- 1 SerDes Port
  - Deep Partition Mode
  - Single Port A
  - 8 QDR capacity
  - 4 partitions of 4M x 72 each that are fully independent random-access memories Each partition is equivalent density to a QDR device
  - Maximum word width is 288b
  - Maximum bandwidth is 320 Gb/s (160 Gb/s full duplex)

- 2 SerDes Ports
  - Wide Partition Mode
  - Two Ports (A & B)
  - 8 QDR capacity
  - 8 partitions of 2M x 72 each that are fully independent random-access memories.
  - Maximum word width is 576b
  - Maximum bandwidth is 640 Gb/s (320 Gb/s full duplex)

Random-Access-Bandwidth

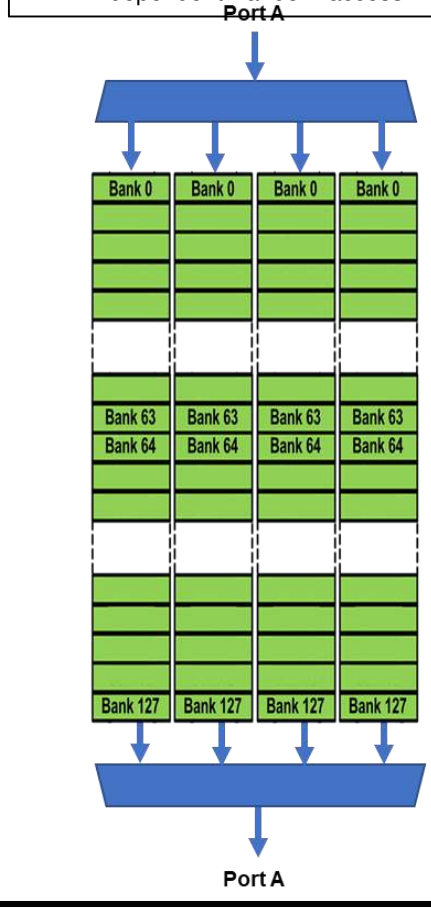
While the discussion so far has been on bandwidth horizontally across the partitions for higher bandwidth, it should be clearly stated that at this high bandwidth, each partition can still address any location within its partition independently of the other partitions accessing any location within its partition.

Memory User-Defined Word Width

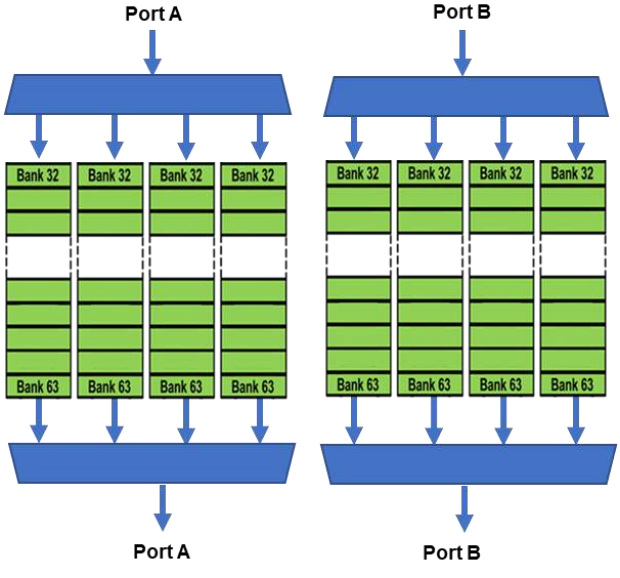
Memory controller can handle the following user selectable word widths

- Single Port A
  - Up to 288b
- Two Port A & B
  - Port A
    - Up to 288b
  - Port B
    - Up to 288b
  - Combined Port A and Port B
    - Up to 576b

QPR8-220 1Gb Memory
Deep 4 Partition RTL Memory Controller
Each Partition is 4M x 72b
Independent Random-access



QPR8-230 1Gb Memory
Wide 8 Partition RTL Memory Controller
Each Partition is 2M x 72b
Independent Random-access

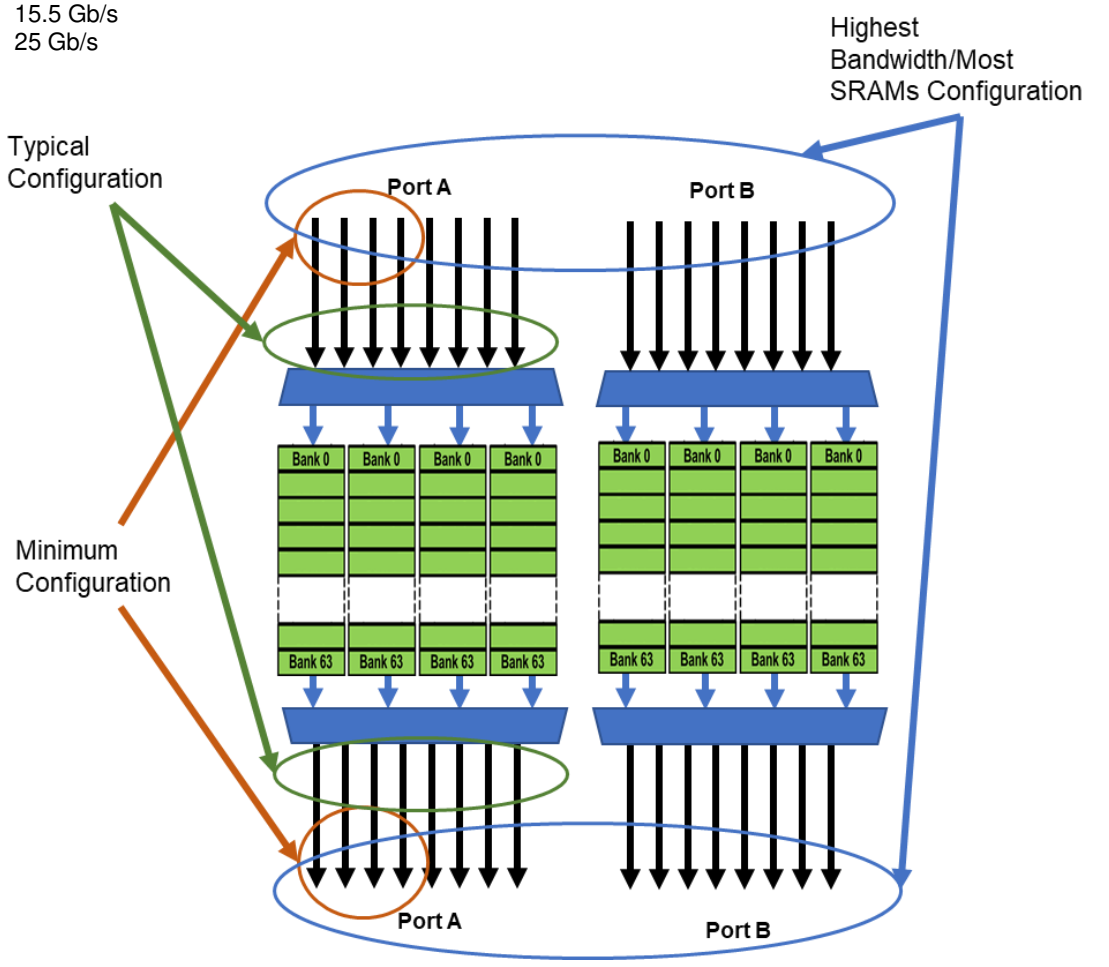


FPGA Serial I/O Ports

Overview of Serial vs Parallel FPGA Interfacing

As systems are demanding more memory the standard parallel interface has expanded from hundreds to thousand of pins and the effort to route and debug has become a tremendous engineering effort in time routing and debug.This translates to costs and reliability.
To increase bandwidth, the number of parallel pins would have to be expanded. Since all new FPGAs are adding more and more SerDes, MoSys adopted the SerDes as the key to increasing bandwidth with no pin limitation issues or design issues.
The QPR memory uses a MoSys defined Serial Protocol called GCI which has been made Open Source. MoSys also offers reference RTL Memory Controller(s) to simplify the FPGA integration to the QPR memory making the serial interface totally transparent to the designer/user.
The number of pins and the speed of the SerDes is dependent on the systems Bandwidth needs. A SerDes lane requires a Rx (Receive) and a Tx (Transmit) (total of 4 pins). These SerDes will also operate over a connectors.

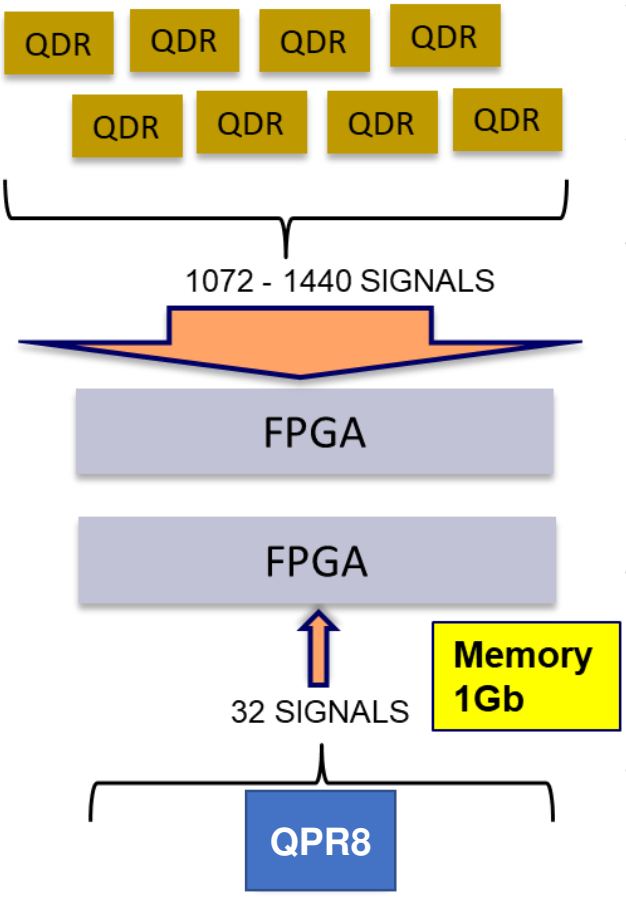
- Minimum configuration of 4 lanes, 16 pins on Port A
- Typical system is 8 lanes, 32 pins on Port A
- Highest bandwidth
  - Utilizes both Port A & Port B
  - 16 lanes, 32 SerDes, 64 Pins
- SerDes speeds available
  - 15.5 Gb/s
  - 25 Gb/s



QPR8 vs QDR-144Mb

Summary of Benefits

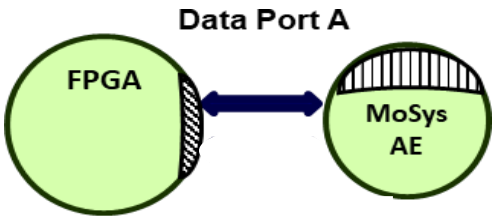
- Capacity …
  - 1Gb memory
  - Replaces 8 QDR/SyncSRAM devices
- Cost…
  - One QPR with 8x the capacity is approximately the price of three QDR memories
- Pins …
  - Typical application uses only 8 lanes, 16 signals, 32 FPGA pins

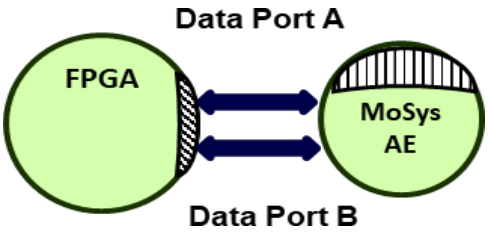


Comparison QPR vs. QDR

- Memory size
  - MSQ230: 1Gb capacity equivalent to 8 QDR-144Mb capacity per device
- Device PCB board space saving
  - 1 MSQ220 device vs 8 QDR devices
- Signal pins reductions
  - 8 QDRs: 1,072-1440 pins
  - 1 MSQ230: typical system 32 pins
  - All MoSys devices have Auto-Adaptation which handles on-board signal tuning, eliminating the need for any external components to ensure clean, reliable signals
- Cost
  - One MSQ230 with 8x the memory capacity is generally less than the price of 3 QDR memories
- Applications
  - Larger buffers, High Bandwidth networking applications like search tables
  - Allows real time operations and analysis at line or data rates
  - Eliminates need for complex parallel
  - operations using RLDRAM, HBM, or slow DRAM

MoSys Family of Memories





In-Memory	Part Number	Description	Package	Interface					Memory		Access Rate	In-Memory Functions			
			Pkg Size	Lanes	Rate per Lane Gb/s			BW MAX.	tRC	Size	Billion Transactions per second	R/W	BURST for Data Movement	RMW / ALU for Compute and Decision	Custom & User Functions with 32 RISC
			mm	Tx/Rx	10.3	12.5	15.6	25	Gb	ns	Gb					
QPR4	MSQ220	QPR4 (Quad Partition Rate) 0.5 Gb	FCBGA 19X19	16	✓	✓			320	3.2	O.5	2.5	✓			
QPR8	MSQ230	QPR8 (Quad Partition Rate) 1Gb	FCBGA 27X27	16			✓	✓	640	2.7	1	5	✓			
BURST	MSR622	Bandwidth Engine 2 Burst Serial 0.5Gb High Access Memory	FCBGA 19x19	16	✓	✓			320	3.2	0.5	3.3	✓	✓		
	MSR630	Bandwidth Engine 3 Burst Serial 1Gb High Access Memory	FCBGA 27x27	16		✓	✓	✓	640	2.7	1	6.5	✓	✓		
RMW	MSR820	Bandwidth Engine 2 RMW Serial 0.5Gb High Access Memory with ALU for RMW functions	FCBGA 19x19	16	✓	✓			320	3.2	0.5	3.3	✓	✓	✓	
	MSR830	Bandwidth Engine 3 RMW Serial 1Gb High Access Memory with ALU for RMW functions	FCBGA 27x27	16		✓	✓	✓	640	2.7	1	6.5	✓	✓	✓	
Program	MSPS30	Programmable HyperSpeed Engine Serial Interface, 1Gb Memory, 32 RISC Processor cores for custom algorithms, compute, functions	FCBGA 27x27	16		✓	✓	✓	717	2.7	1	24 Internal	✓	✓	✓	✓
RTL	RTL-AE	RTL Memory Controller for Bandwidth Engine and Programmable HyperSpeed Engine. Manages memory and the serial interface signals. Presents a QDR like parallel RTL interface to the user.	FPGA RTL Code		✓	✓	✓	✓			576Mb & 1Gb	6.5	✓	✓	✓	

BW MAX. = Aggregate of all SerDes laneS at the highest serial interface speed

QPR Pin Compatible Roadmap with higher feature BLAZER Family of Accelerator Engines

- MSP220 (QPR4) is pin compatible with the MSR622 and MSR820
- MSP230 (QPR8) is pin compatible with the MSR630 and MSR830
- MSP230 (QPR8) is pin compatible with the MSPS30

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