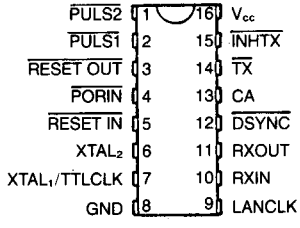
COM91C32
Local Area Network Transceiver
LANT

FEATURES

- ☐ Compatible with the COM9026 and COM90C26 LANCs
- ☐ Compatible with the HYC9058 HIT
- ☐ Compatible with the HYC9068 LAND
- ☐ Functionally compatible with the COM90C32
- ☐ Reduces node chip count
- ☐ Built-in 20MHz crystal oscillator
- ☐ Internal Power On Reset for COM9026/COM90C26
- ☐ Provides all clocks for COM9026/COM90C26
- ☐ Low power CMOS technology
- ☐ TTL compatible
- ☐ 5V only power supply

PIN CONFIGURATION*



*Check with factory for SMT package availability

GENERAL DESCRIPTION

The COM91C32 local area network transceiver (LANT) is an improved version of the COM90C32. It reduces both node cost and board real estate. The COM91C32 is a companion chip to either the COM9026 or COM90C26 local area network controller (LANC), the HYC9068 local area network driver (LAND), and the HYC9058 high impedance transceiver (HIT).

The COM91C32 contains two circuits not available on the COM90C32. A 20MHz crystal oscillator has been built in to eliminate the need for an external oscillator. In addition, the external power on reset circuit required by the COM9026/COM90C26 has been integrated inside the COM91C32 to reduce the number of components, their related costs, and board real estate.

The COM91C32 performs the functions necessary to allow simple interface to the transmission media for ARCNET® local area networks. The COM91C32 produces two 5MHz clocks for the COM9026/COM90C26. The first one (LANCLK) is free running and feeds the clock input (pin 19) of the COM9026/COM90C26. The second one (CA) has start/stop capability controlled by the $\overline{\text{DSYNC}}$ output of the COM9026/COM90C26 as well as the data received from the network.

During data reception, the COM91C32 will convert incoming serial receive data from the HIT or LAND circuit to NRZ form which will directly feed the RX input of the COM9026/COM90C26 (pin 38). During transmission, the COM91C32 converts the transmit data from the COM9026/COM90C26 $\overline{\text{TX}}$, (pin 37) into the waveforms necessary to drive the HYC9058 or HYC9068 as shown in figure 2.

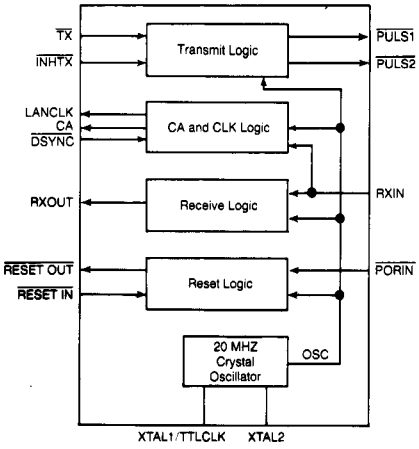


Figure 1: COM91C32 INTERNAL BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS (refer to figure 2)

PIN NO.	NAME	SYMBOL	FUNCTION
COM 9026 Interface			
2 1	PULSE 1 PULSE 2	$\overline{PULS1}$ $\overline{PULS2}$	$\overline{PULS1}$ AND $\overline{PULS2}$ carry the transmit data information encoded in pulse format.
3	RESET OUT	$\overline{RESET\ OUT}$	This output signal provides a reset signal capable of ensuring proper reset of the COM9026/COM90C26. It is TTL compatible. The $\overline{RESETOUT}$ pulse width equals 102.4μsec + ($\overline{RESETIN}$ or $\overline{PORIN}$ pulse width).
10	RECEIVE IN	RXiN	This input carries the receive data information from the cable interface circuitry.
11	RECEIVE OUT	RXOUT	This output provides the NRZ encoded receive data to the COM9026/COM90C26.
12	DELAYED SYNC	$\overline{DSYNC}$	This active low input is asserted by the COM9026 and is used to synchronize the CA clock.
13	CA	CA	This output is a 5 MHz start/stop clock that halts when $\overline{DSYNC}$ goes active. It is used to synchronize the CA clock output to the RX OUT received data.
14	TRANSMIT DATA	$\overline{TX}$	This input represents the serial data transmitted by the COM9026/COM90C26.
15	TRANSMIT INHIBIT	$\overline{INHTX}$	This active low input inhibits the COM91C32 from transmitting by forcing $\overline{PULS1}$ and $\overline{PULS2}$ high.
System Clock Interface			
4	POWER ON RESET IN	$\overline{PORIN}$	This input signal, which is controlled by C_1 (fig. 2) on Power up, disables the transmitter portion of the COM91C32 and generates the $\overline{RESET\ OUT}$ signal. This pin has a schmitt trigger input.
5	RESET IN	$\overline{RESET\ IN}$	This input signal disables the transmitter portion of the COM91C32 and generates the $\overline{RESET\ OUT}$ signal. This pin has a TTL compatible input.
7 6	CRYSTAL	XTAL1 XTAL2	An external 20 MHz crystal is connected to these pins. If an external 20 MHz TTL clock is used, it should be connected to XTAL1 (pin 7) with a 390 ohm pullup resistor; XTAL2 must be left floating.
9	LAN CLOCK	LANCLK	This output supplies a 5 MHz free running clock for the COM9026/COM90C26.
8	GROUND	GND	Ground
16	+5V SUPPLY	VCC	+5 Volt Power Supply

FUNCTIONAL DESCRIPTION

The COM9026/COM90C26, when transmitting data on $\overline{TX}$, will produce a negative pulse of 200 nanoseconds to indicate a logic "1" and no pulse to indicate a logic "0." Referring to figure 4, a 200 nanosecond pulse on $\overline{TX}$ is converted to 2, 100 nanosecond nonoverlapping pulses shown as $\overline{PULS1}$ and $\overline{PULS2}$. The signals $\overline{PULS1}$ and $\overline{PULS2}$ drive the HYC9058 or the HYC9068 which in turn creates a 200 nanosecond dipulse signal on the cable as shown in figure 2.

At the receiving nodes, each dipulse appearing on the cable is coupled through the RF transformer of the HYC9058 or HYC9068 to produce a positive pulse. These pulses are captured by the COM91C32 and are converted to NRZ data. As each byte is received by the COM91C32, the CA clock is stopped by the COM9026/COM90C26 (via $\overline{DSYNC}$) until the zero bit of the next byte is received. This will automatically restart the CA clock. The COM9026/COM90C26 uses the CA clock to sample the NRZ data and these samples points are shown in figure 5.

Typically, RXIN pulses occur at multiples of 400 nanoseconds. The COM91C32 can tolerate distortion of plus or minus 100 nanoseconds and still correctly capture and convert the RXIN pulses to NRZ format.

RESETTING THE COM91C32

The $\overline{PORIN}$ active low input signal is generated by turning the power on to generate the $\overline{RESET\ OUT}$ signal to the COM9026/COM90C26. The recommended capacitor value (C1 in figure 2) required to properly reset the COM9026/COM90C26 on power up is 0.1 μF.

The $\overline{RESET\ IN}$ active low input signal is provided to generate the $\overline{RESET\ OUT}$ signal used to reset the COM9026/COM90C26. The pulse width of the $\overline{RESET\ OUT}$ signal is 102.4 microseconds, which is wide enough to properly reset the COM9026/COM90C26 local area network controller device.

$\overline{RESET\ OUT}$ = $\overline{RESET\ IN}$ (pulse width) + 102.4 microseconds

$\overline{RESET\ OUT}$ = $\overline{PORIN}$ (pulse width) + 102.4 microseconds

In addition to initializing the COM91C32 to an idle state, the $\overline{RESET\ IN}$ signal disables the transmitter portion of the COM91C32 during reset.

During reset, the COM91C32 output pins are as follows:

$\overline{PULS1}$ - is inactive (high)
$\overline{PULS2}$ - is inactive (high)
LANCLK - is free running during and after reset
CA - is free running during and after reset

The minimum $\overline{RESET\ IN}$ pulse width is 120 nanoseconds (or 2T + 20 nanoseconds for input clocks different than 20 MHz). For the 20 MHz clocks, T equals 50 nanoseconds.

RESET IN/OUT TIMING

The COM91C32 incorporates a digital filter that will suppress glitches on the $\overline{RESET\ IN}$ and $\overline{POR\ IN}$ pins. The digital filter will filter all $\overline{RESET\ IN}$ and $\overline{PORIN}$ glitches that are narrower than 40ns (1T-10ns). It will allow $\overline{RESET\ IN}$ and $\overline{POR\ IN}$ pulses that are wider than 120 ns (2T+20ns). The $\overline{RESET\ OUT}$ pulse width is equal to the $\overline{RESET\ IN}$ pulse width plus 102.4 microseconds.

THE INTERNAL OSCILLATOR

The COM91C32 incorporates on-board circuitry which, in conjunction with an external parallel resonant crystal, forms an oscillator. The oscillator frequency may vary between 8 MHz and 20 MHz to allow for a variable data rate from 1.0 Mbps to 2.5 Mbps.

The oscillator input is divided by 4 to produce the CA and the LANCLK output clocks to the COM9026/COM90C26.

The COM91C32 XTAL oscillator has been designed to work with a parallel resonant crystal and does not require an external resistor. Only two capacitors are needed (one from each leg of the XTAL to ground.) The values of the capacitors are two times the load capacitance of the crystal. Typical capacitor values are 22 pF.

The external crystal must have an accuracy of 0.020% or better.

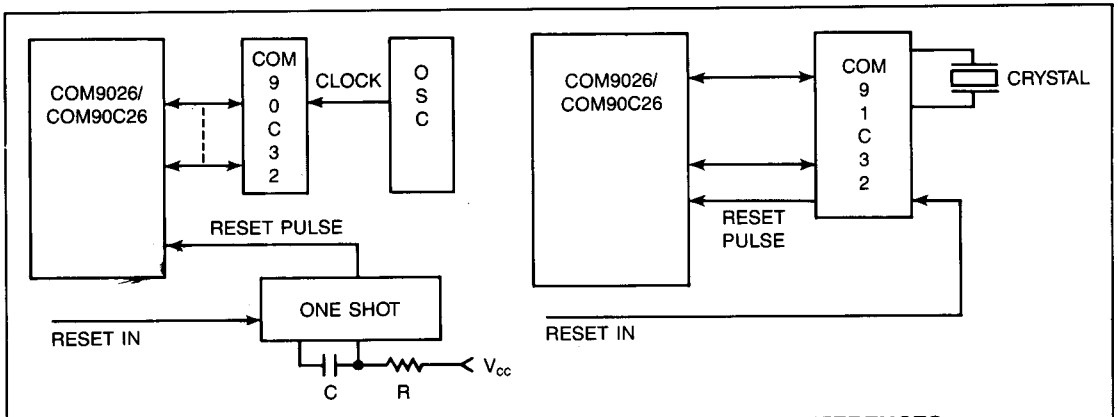


FIGURE 2: COM90C32 AND 91C32 IMPLEMENTATION DIFFERENCES

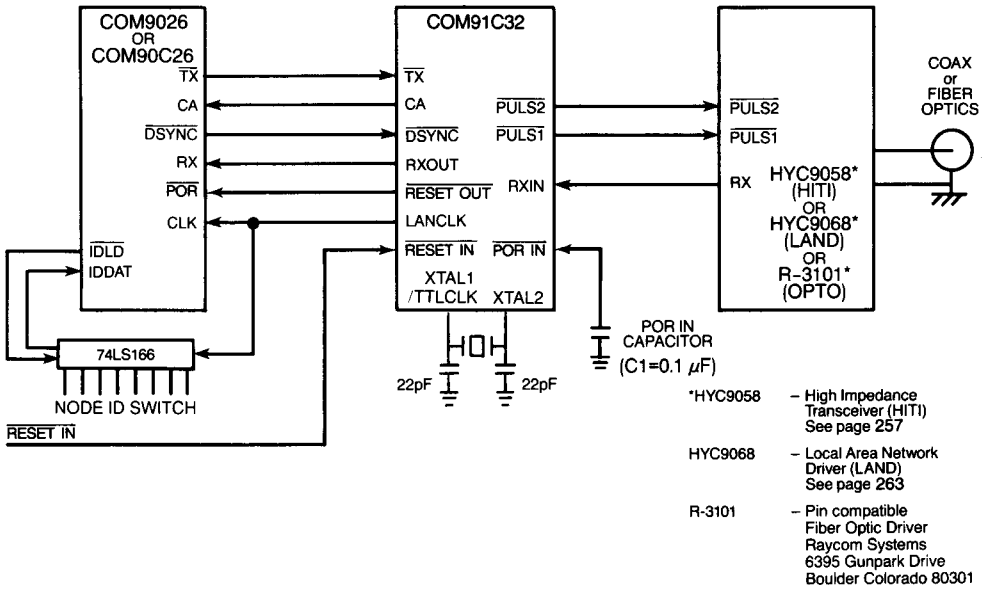


FIGURE 3: COM91C32 SYSTEM INTERFACE

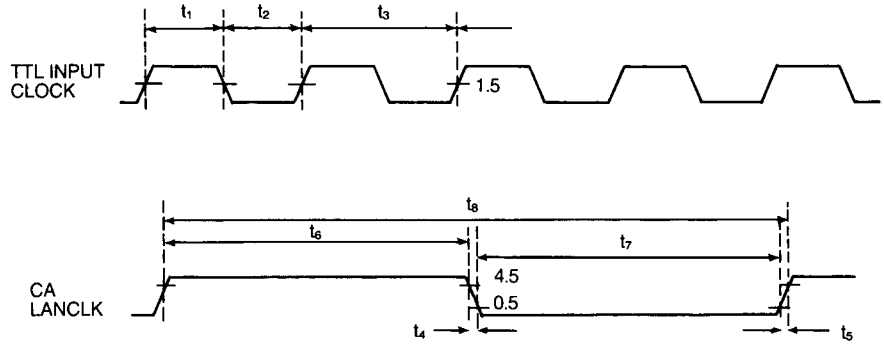


FIGURE 4: COM91C32 CLOCK TIMING

TABLE 1 - COM91C32 ELECTRICAL CHARACTERISTICS

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-55°C to 150°C
Lead Temperature (soldering, 10 sec.)	325°C
Positive Voltage on any Pin	V_{cc} + 0.3
Negative Voltage on any Pin	-0.3V
Maximum V_{cc}	+ 7.0V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

DC CHARACTERISTICS (T_a = 0°C to +70°C, V_{cc} =5V ± 5%)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
INPUT VOLTAGES					
V_{IH1} High Input Voltage	2.7			V	except for TTL CLK and $\overline{PORIN}$
V_{IL1} Low Input Voltage			0.8	V	
V_{IH2} High Input Voltage	V_{cc}-0.5V			V	for TTL CLK IN
V_{IL2} Low Input Voltage			1	V	
V_{IH3} High Input Voltage	3.6			V	for $\overline{PORIN}$
V_{IL3} Low Input Voltage			1.0	V	
OUTPUT VOLTAGES					
V_{OH1} High Output Voltage	V_{cc}-1.0			V	IOH = 400 μA except for CA, LANCLK
V_{OL1} Low Output Voltage			0.4	V	IOL = 4.0 mA except for CA, LANCLK
V_{OH2} High Output Voltage	V_{cc}-0.5			V	IOH = 100 μA for CA, LANCLK
V_{OL2} Low Output Voltage			0.4	V	IOL = 100 μA for CA, LANCLK
INPUT LEAKAGE CURRENT					
IL		±10		μA	
INPUT CAPACITANCE					
C_{IN}			15	pF	
POWER SUPPLY CURRENT					
I_{cc}			20	mA	

AC CHARACTERISTICS (T_a = 0°C to +70°C, V_{cc} =5V ± 5%)

FIG NO.	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
	TTL CLOCK INPUT TIMING					
Fig. 3	t_1 Input Clock High Time	20			ns	@ V_{cc}-0.5V
	t_2 Input Clock Low Time	20			ns	@ 1V
	t_3 Input Clock Period		50		ns	
	CA, LANCLK OUTPUT TIMING					
Fig. 3	t_4 Clock Out Fall Time			20	ns	@ 50 pF max
	t_5 Clock Out Rise Time			20	ns	@ 50 pF max
	t_6 Clock Out High Time	75			ns	@ 50 pF max
	t_7 Clock Out Low Time	75			ns	@ 50 pF max
	t_8 Clock Out Period		200		ns	@ 50 pF max
	TRANSMIT TIMING					
Fig. 4	t_9 TX Setup to CA falling edge	50			ns	
	t_{10} TX Hold after CA falling edge	10			ns	
	t_{11} Xtal rising edge to $\overline{PULS1/2}$		60		ns	
	t_{12} $\overline{PULS1/2}$ Pulse Width		2 (t_3)		ns	
	t_{13} $\overline{INHTX}$ to Pulse inactive			100	ns	
	RECEIVE TIMING					
Fig. 5	t_{15} RXIN Pulse Width	10			ns	
	t_{16} RXIN to RXOUT delay		5 (t_3) + 70		ns	
	t_{17} RXOUT Pulse Width		400		ns	
	t_{18} XTAL RISING EDGE TO RXOUT			70	ns	
	$\overline{DSYNC}$, CA TIMING					
Fig. 5	t_{19} $\overline{DSYNC}$ Setup to CA rising edge		20		ns	
	RESET TIMING					
Fig. 6	t_{30} $\overline{RESET\ IN}$ Pulse Width	120			ns	(NOTE 1)
	t_{31} $\overline{RESET\ IN}$ falling edge to $\overline{RESET\ OUT}$ falling edge			170	ns	(NOTE 2)
	t_{32} $\overline{RESET\ IN}$ rising edge to $\overline{RESET\ OUT}$ rising edge	102	102.4	103	us	
	t_{33} $\overline{RESET\ OUT}$ Pulse Width		$t_{30}+t_{32}-2t_3$			
	INPUT CLOCK FREQUENCY	8.0		20	MHz	

NOTE 1: For Input clock frequencies of less than 20 MHz, $t_{30} = 2t_3 + 20$ ns
NOTE 2: For Input clock frequencies of less than 20 MHz, $t_{31} = 2t_3 = 70$ ns

*ALL TYPICAL VALUES ARE AT V_{cc} = 5.0 V and TEMPERATURE = 25°C

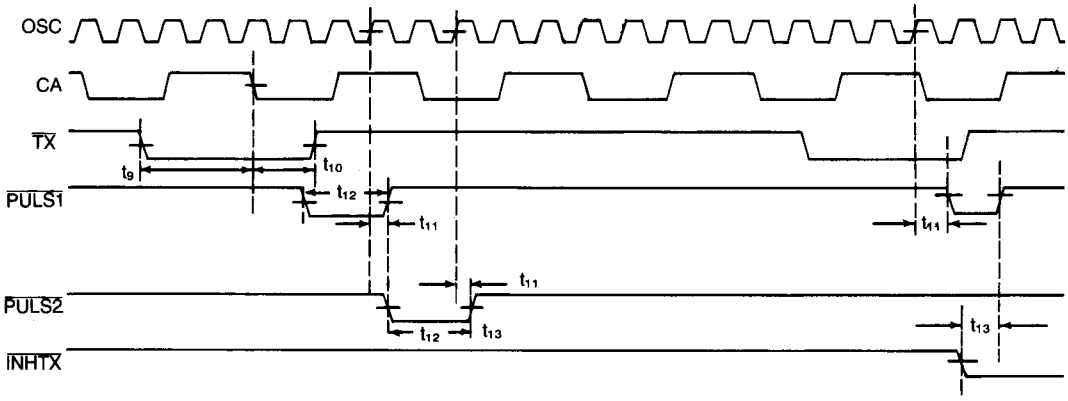


FIGURE 5: TRANSMIT TIMING PARAMETERS

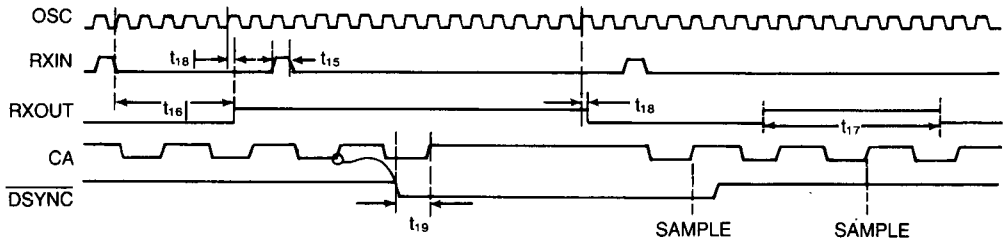


FIGURE 6: RECEIVE TIMING PARAMETERS

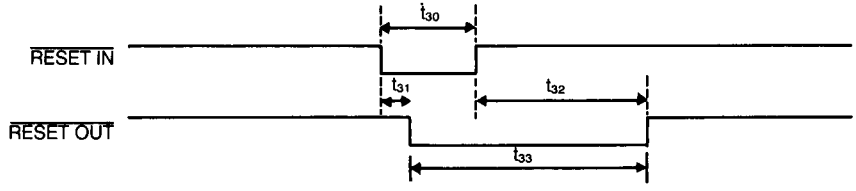


FIGURE 7: RESET IN - TO - RESET OUT TIMING

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35 Marcus Blvd Hauppauge N.Y 11788
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