

# 74LVC00A

## Low-Voltage CMOS Quad 2-Input NAND Gate

### With 5 V-Tolerant Inputs

The 74LVC00A is a high performance, quad 2-input NAND gate operating from a 1.2 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5 V allows 74LVC00A inputs to be safely driven from 5 V devices.

Current drive capability is 24 mA at the outputs.

#### Features

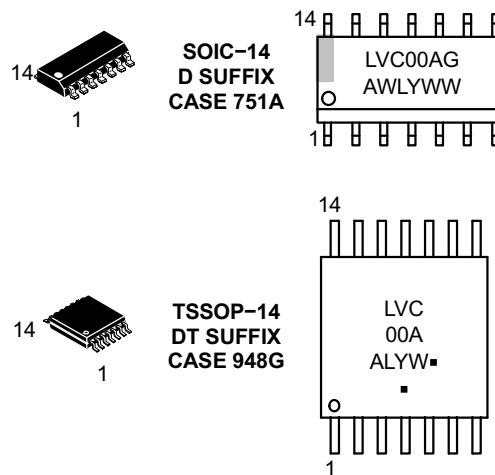
- Designed for 1.2 V to 3.6 V  $V_{CC}$  Operation
- 5 V Tolerant Inputs – Interface Capability With 5 V TTL Logic
- 24 mA Output Sink and Source Capability
- Near Zero Static Supply Current (10  $\mu$ A) Substantially Reduces System Power Requirements
- ESD Performance: Human Body Model >2000 V  
Machine Model >200 V
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



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#### MARKING DIAGRAMS



A = Assembly Location  
L, WL = Wafer Lot  
Y = Year  
W, WW = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# 74LVC00A

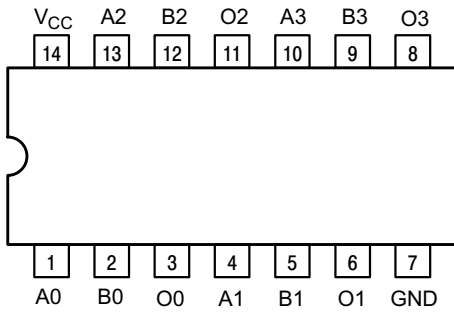


Figure 1. Pinout: 14-lead (Top View)

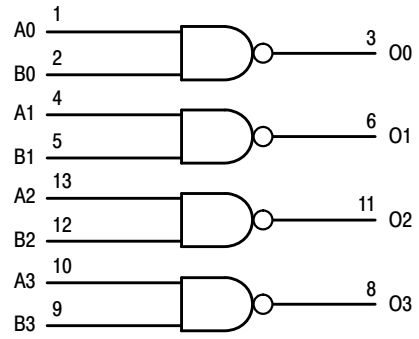


Figure 2. Logic Diagram

## PIN NAMES

Pins	Function
An, Bn	Data Inputs
On	Outputs

## TRUTH TABLE

Inputs		Outputs
An	Bn	On
L	L	H
L	H	H
H	L	H
H	H	L

H = High Voltage Level

L = Low Voltage Level

For I<sub>CC</sub> reasons, DO NOT FLOAT Inputs

# 74LVC00A

## MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
$V_{CC}$	DC Supply Voltage	-0.5 to +6.5		V
$V_I$	DC Input Voltage	$-0.5 \leq V_I \leq +6.5$		V
$V_O$	DC Output Voltage	$-0.5 \leq V_O \leq V_{CC} + 0.5$	Output in HIGH or LOW State (Note 1)	V
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA
$I_{CC}$	DC Supply Current Per Supply Pin	$\pm 100$		mA
$I_{GND}$	DC Ground Current Per Ground Pin	$\pm 100$		mA
$T_{STG}$	Storage Temperature Range	-65 to +150		°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds	$T_L = 260$		°C
$T_J$	Junction Temperature Under Bias	$T_J = 135$		°C
$\theta_{JA}$	Thermal Resistance (Note 2)	SOIC = 85 TSSOP = 100		°C/W
MSL	Moisture Sensitivity		Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- $I_O$  absolute maximum rating must be observed.
- Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
$V_{CC}$	Supply Voltage Operating Functional	1.65 1.2		3.6 3.6	V
$V_I$	Input Voltage	0		5.5	V
$V_O$	Output Voltage HIGH or LOW State	0		$V_{CC}$	V
$I_{OH}$	HIGH Level Output Current $V_{CC} = 3.0\text{ V} - 3.6\text{ V}$ $V_{CC} = 2.7\text{ V} - 3.0\text{ V}$			-24 -12	mA
$I_{OL}$	LOW Level Output Current $V_{CC} = 3.0\text{ V} - 3.6\text{ V}$ $V_{CC} = 2.7\text{ V} - 3.0\text{ V}$			24 12	mA
$T_A$	Operating Free-Air Temperature	-40		+125	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate $V_{CC} = 1.65\text{ V to } 2.7\text{ V}$ $V_{CC} = 2.7\text{ V to } 3.6\text{ V}$	0 0		20 10	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# 74LVC00A

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	-40°C to +85°C			-40°C to +125°C			Unit
			Min	Typ (Note 3)	Max	Min	Typ (Note 3)	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 x V <sub>CC</sub>	-	-	0.65 x V <sub>CC</sub>	-	-	
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	-	
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	-	
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	-	0.12	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35 x V <sub>CC</sub>	-	-	0.35 x V <sub>CC</sub>	
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	-	0.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	-	0.8	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>							V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	-	-	V <sub>CC</sub> - 0.3	-	-	
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	1.05	-	-	
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.8	-	-	1.65	-	-	
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	2.05	-	-	
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	2.4	-	-	2.25	-	-	
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.2	-	-	2.0	-	-	
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>							V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	-	-	0.3	
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	-	0.65	
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	-	-	0.8	
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	-	0.6	
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	-	0.8	
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = 5.5V or GND V <sub>CC</sub> = 3.6 V	-	±0.1	±5	-	±0.1	±20	μA
I <sub>OFF</sub>	Power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 0.0 V	-	±0.1	±10	-	±0.1	±20	μA
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 3.6 V	-	0.1	10	-	0.1	40	μA
ΔI <sub>CC</sub>	Additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 2.7 V to 3.6 V	-	5	500	-	5	5000	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. All typical values are measured at T<sub>A</sub> = 25°C and V<sub>CC</sub> = 3.3 V, unless stated otherwise.

# 74LVC00A

## AC ELECTRICAL CHARACTERISTICS ( $t_R = t_F = 2.5 \text{ ns}$ )

Symbol	Parameter	Conditions	-40°C to +85°C			-40°C to +125°C			Unit
			Min	Typ <sup>1</sup>	Max	Min	Typ <sup>1</sup>	Max	
$t_{pd}$	Propagation Delay (Note 5)	$V_{CC} = 1.2 \text{ V}$	-	12.0	-	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.5	3.8	8.4	0.5	-	9.7	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.5	2.2	4.8	0.5	-	5.7	ns
		$V_{CC} = 2.7 \text{ V}$	0.5	2.3	5.1	0.5	-	5.9	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	0.5	2.0	4.3	0.5	-	5.1	ns
$t_{sk(0)}$	Output Skew Time (Note 6)	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	1.0	-	-	1.5	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Typical values are measured at  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 3.3 \text{ V}$ , unless stated otherwise.

5.  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ); parameter guaranteed by design.

## DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25^\circ\text{C}$			Unit
			Min	Typ	Max	
$V_{OLP}$	Dynamic LOW Peak Voltage (Note 7)	$V_{CC} = 3.3 \text{ V}, C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$ $V_{CC} = 2.5 \text{ V}, C_L = 30 \text{ pF}, V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$		0.8 0.6		V
$V_{OLV}$	Dynamic LOW Valley Voltage (Note 7)	$V_{CC} = 3.3 \text{ V}, C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$ $V_{CC} = 2.5 \text{ V}, C_L = 30 \text{ pF}, V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$		-0.8 -0.6		V

7. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
$C_{IN}$	Input Capacitance	$V_{CC} = 3.3 \text{ V}, V_I = 0 \text{ V or } V_{CC}$	4.0	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = 3.3 \text{ V}, V_I = 0 \text{ V or } V_{CC}$	5.0	pF
$C_{PD}$	Power Dissipation Capacitance (Note 8)	Per input; $V_I = \text{GND or } V_{CC}$		pF
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	5.6	
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	8.9	
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	11.8	

8.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

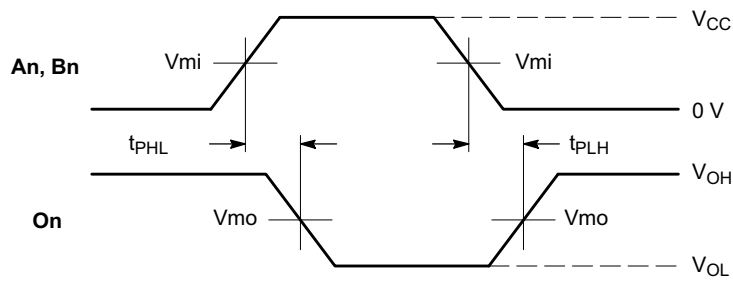
$f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz

$C_L$  = output load capacitance in pF  $V_{CC}$  = supply voltage in Volts

$N$  = number of outputs switching

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

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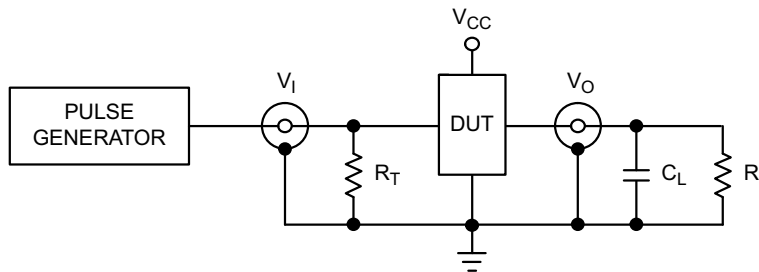


**WAVEFORM 1 - PROPAGATION DELAYS**

$t_R = t_F = 2.5 \text{ ns}$ , 10% to 90%;  $f = 1 \text{ MHz}$ ;  $t_W = 500 \text{ ns}$

Symbol	Vcc		
	3.3 V ± 0.3 V	2.7 V	V <sub>CC</sub> < 2.7 V
V <sub>mi</sub>	1.5 V	1.5 V	V <sub>CC</sub> /2
V <sub>mo</sub>	1.5 V	1.5 V	V <sub>CC</sub> /2

**Figure 3. AC Waveforms**



$C_L$  includes jig and probe capacitance  
 $R_T = Z_{OUT}$  of pulse generator (typically 50  $\Omega$ )

Supply Voltage	Input		Load	
	V <sub>CC</sub> (V)	V <sub>I</sub> , t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>
1.2	V <sub>CC</sub>	≤ 2 ns	30 pF	1 k $\Omega$
1.65 - 1.95	V <sub>CC</sub>	≤ 2 ns	30 pF	1 k $\Omega$
2.3 - 2.7	V <sub>CC</sub>	≤ 2 ns	30 pF	500 $\Omega$
2.7	2.7 V	≤ 2.5 ns	50 pF	500 $\Omega$
3 - 3.6	2.7 V	≤ 2.5 ns	50 pF	500 $\Omega$

**Figure 4. Test Circuit**

## ORDERING INFORMATION

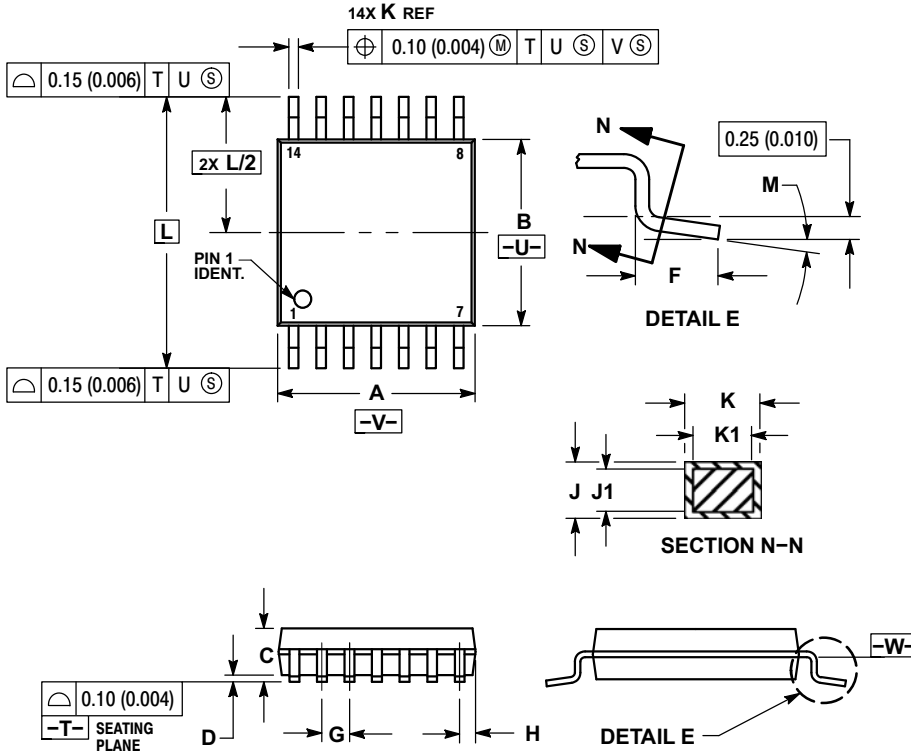
Device	Package	Shipping†
74LVC00ADR2G	SOIC-14 NB (Pb-Free)	2500 / Tape & Reel
74LVC00ADTR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# 74LVC00A

## PACKAGE DIMENSIONS

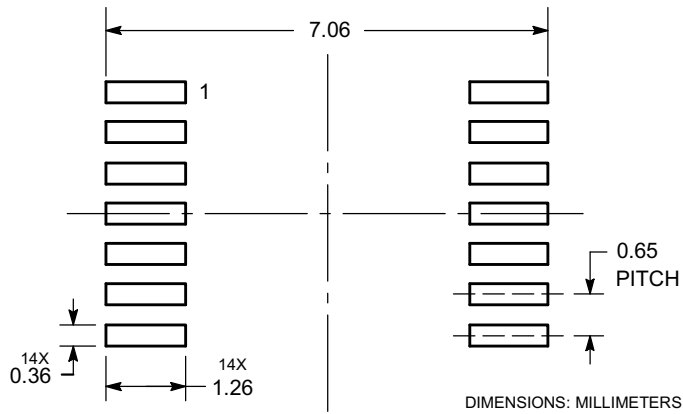
TSSOP-14  
CASE 948G  
ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE  $-W-$ .

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0° 8°		0° 8°	

### SOLDERING FOOTPRINT\*

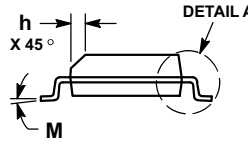
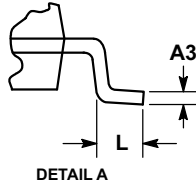
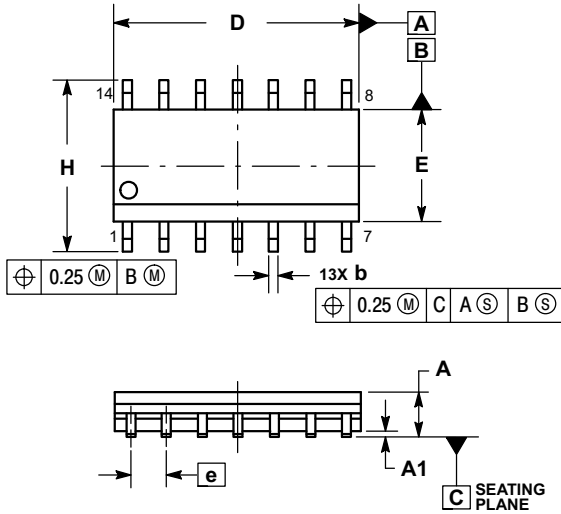


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# 74LVC00A

## PACKAGE DIMENSIONS

### SOIC-14 NB CASE 751A-03 ISSUE K

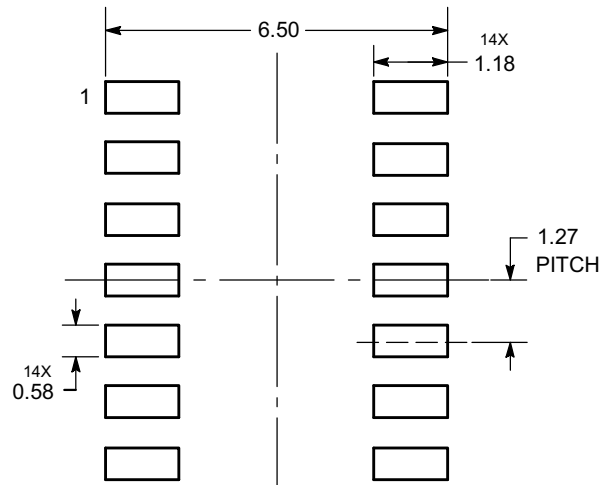


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°		7°	

### SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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