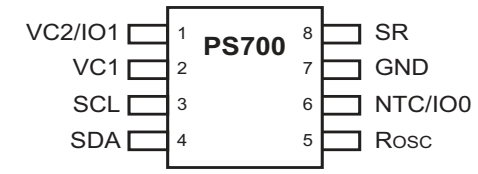
PS700

Battery Monitor

Features

- Measures, maintains and reports all critical rechargeable battery parameters with high accuracy
- Supports Lithium (1-cell and 2-cell) battery packs
- Current measurement with 16-bit integrating A/D accurate to less than ±0.5% error
- Temperature measurement accurate to within ±2°C absolute, using on-chip temperature sensor or external thermistor
- Accumulation of charge current, discharge current, temperature and voltage in independent 32-bit registers
- 512-byte nonvolatile EEPROM stores factory programmed, measured and user-defined parameters
- In-system offset calibration compensates for offset error in current measurement
- Industry standard SMBus/I^{2}C™ compatible 2-wire communications interface
- 8-pin TSSOP package
- -20°C to +85°C operating temperature range
- NTC pin can be configured as a thermistor input or GPIO
- VC2 pin can be configured as a cell input or a GPIO
- Flexible power operating modes allow low-power monitoring of battery conditions during system full operating and standby conditions:
  - Run: Continuous Conversion; 80 µA typ.
  - Sample: Sample interval from 0.5-64s @ 45 µA typ.
  - Sample-Sleep: Sample interval from 0.5-138s min. @ 20 µA typ.
- Shelf-Sleep mode reduces power consumption during pack storage conditions to 300 nA typ., with automatic wake-up upon pack insertion

Pin Description



8-pin 150 mil TSSOP Package

Pin Summary

Pin Name	Description
VC2/IO1	Cell voltage input for cell 2 in a 2-series Li Ion pack or general purpose I/O #1
VC1	Cell voltage input for cell 1
SCL	SMBus clock line
SDA	SMBus data I/O
ROSC	Oscillator bias resistor
NTC/IO0	External thermistor connection or general purpose I/O #0
GND	Power supply ground
SR	Sense resistor input

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1.0 PRODUCT OVERVIEW

The PS700 is a cost-effective, highly accurate IC that measures, stores and reports all of the critical parameters required for rechargeable battery monitoring with a minimum of external components. It precisely measures charge/discharge current as well as voltage and temperature of a battery pack. In addition, the PS700 accurately accumulates both charge and discharge current as independent parameters. Temperature history can also be maintained for calculating self-discharge effects.

The PS700 integrates a highly accurate 16-bit integrating A/D converter that performs current measurement to within ±0.5% error. On-chip counters precisely track battery charge/discharge and temperature history. Also included are an on-chip voltage regulation circuit, non-crystal time base and on-chip temperature sensor. The operating voltage range of the PS700 is optimized to allow a direct interface to 1 or 2-series Li Ion/Li Poly battery packs. 512 bytes of general purpose nonvolatile EEPROM storage are provided to store factory programmed, measured and user defined parameters.

Efficient communication is provided through an industry standard SMBus/I^2C™ compatible 2-wire communications interface. This interface allows the host to determine accurate battery status for effective system power management and for communication to the end user. A battery management solution utilizing the PS700 delivers both space and total system component cost savings for a wide variety of battery operated applications.

FIGURE 1-1: PS700 INTERNAL BLOCK DIAGRAM

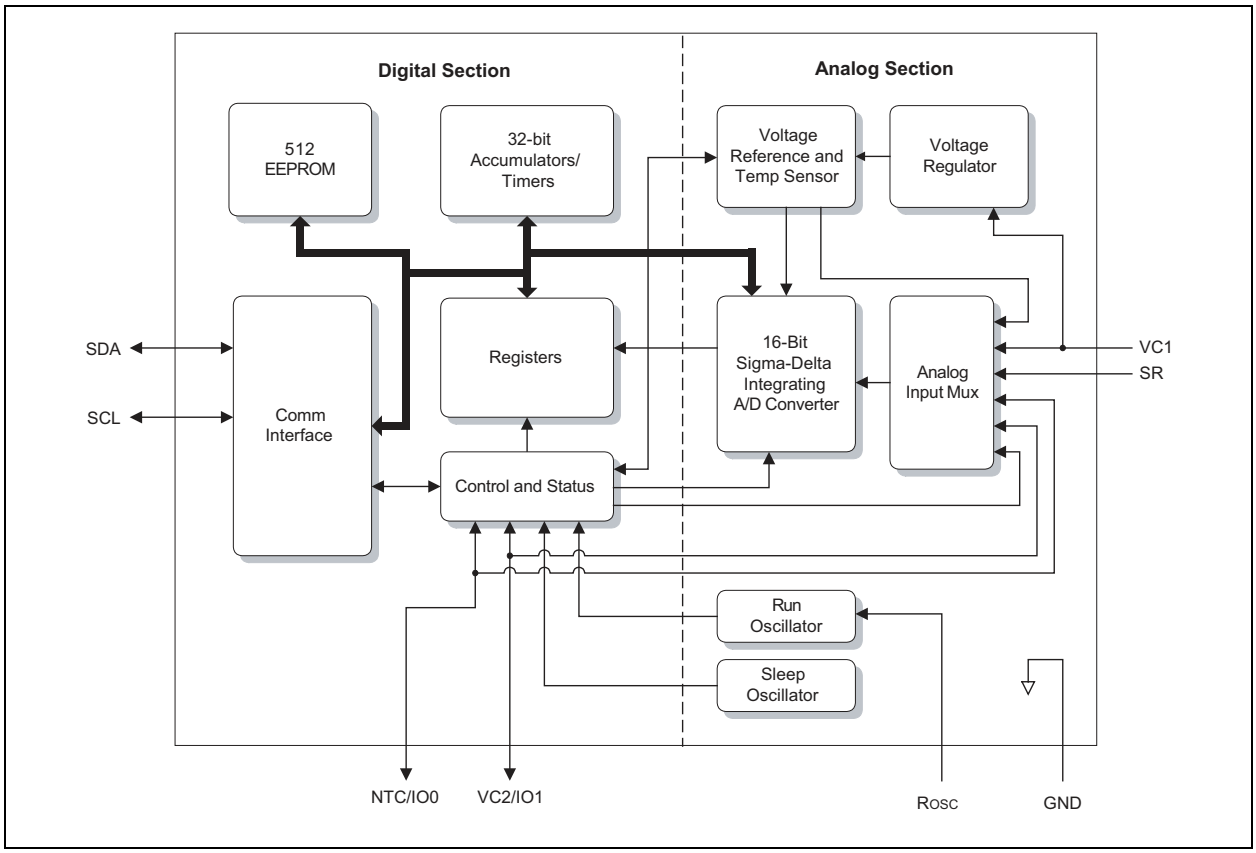

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FIGURE 1-2: APPLICATION SCHEMATIC – PS700-BASED BATTERY PACK

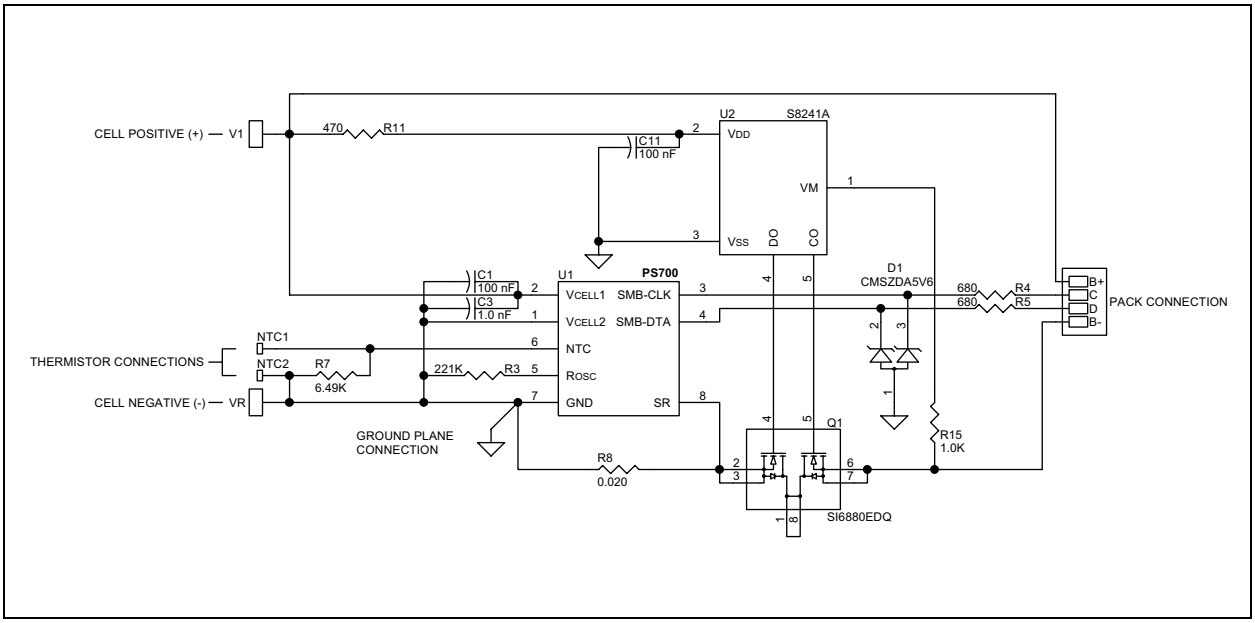

TABLE 1-1: PIN DESCRIPTIONS

Pin No.	Pin Name	Description
1	VC2/IO1	Cell input connection for lowest cell in a 2-cell series Li Ion pack. Can also be configured as an open-drain general purpose input/output.
2	VC1	Cell input connection for highest cell in a 2-cell series Li Ion pack. Connects to the positive terminal of 1-cell series packs. VC1 serves as the power supply input for the PS700.
3	SCL	SMBus/I^2C clock line connection.
4	SDA	SMBus/I^2C data line connection.
5	ROSC	External bias resistor.
6	NTC/IO0	Input for an external temperature sensor using a 103ETB-type thermistor. Can also be configured as a general purpose input/output pin.
7	GND	Analog and digital ground.
8	SR	Current measurement A/D input from positive side of the current sense resistor.

2.0 ARCHITECTURAL OVERVIEW

The PS700 contains a complete analog “front-end” for battery monitoring as well as digital logic for control, measurement accumulation, timing and communications. Major functions within the PS700 include:

- Voltage Regulator
- Precision Time Base
- Temperature Sensor
- 512-Byte EEPROM Memory
- 32-Byte RAM Memory
- Analog-to-Digital (A/D) Converter
- 32-bit Accumulators/Timers
- SMBus/I^2C Communications Interface

Figure 1-1 is a block diagram of the internal circuitry of the PS700. Figure 1-2 is a schematic diagram that depicts the PS700 in a typical single cell Lithium Ion application. The function of each of the blocks listed above is summarized in the following sections.

2.1 Internal Voltage Regulator

The PS700 incorporates an internal voltage regulator that supports 1 or 2-cell series lithium pack configurations. The internal regulator draws power directly from the VC1 input. No other external components are required to regulate internal supply voltage.

2.2 Precision Time Base

The integrated precision time base is a highly accurate RC oscillator that provides precise timing for the sigma-delta A/D and for the on-chip elapsed time counters without the need for an external crystal. This time base is trimmed during manufacturing to a nominal frequency of 131,072 Hz.

2.3 Temperature Sensor

An integrated temperature sensor is provided that can eliminate the need for an external thermistor. As an option, a connection is provided for an external thermistor for applications where the battery pack is physically located at a distance away from the PS700.

2.4 EEPROM Memory

512 bytes of EEPROM memory are incorporated for storage of nonvolatile parameters, such as PowerSmart® 3D cell models for use with host driver firmware. An initialization block is reserved within the EEPROM array for values that are loaded into PS700 registers following a power-on condition.

2.5 RAM Memory

32 bytes of general purpose RAM memory are provided for storage of temporary parameters.

2.6 A/D Converter

The PS700 incorporates an integrating sigma-delta A/D converter together with an analog mux that has inputs for charge and discharge current, cell and pack voltages, the on-chip temperature sensor and an off-chip thermistor. The converter can be programmed to perform a conversion with resolutions of 8 to 15 bits plus sign while utilizing either a ±340 mV or a ±170 mV reference.

2.7 32-Bit Accumulators/Timers

The PS700 incorporates four 32-bit accumulators and four 32-bit elapsed time counters. The Discharge Current Accumulator (DCA) and the Charge Current Accumulator (CCA) are intended to record discharge and charge capacity values. The Discharge Time Counter (DTC) and the Charge Time Counter (CTC) are intended to maintain the total discharge time and charge time. Accumulated charge and discharge values can be used to determine state of charge of the battery as well as cycle count information. With information provided by the elapsed time counters, average charge and discharge currents over an extended period of time can be calculated.

2.8 SMBus/I^2C Communications Interface

The communications port for the PS700 is a 2-wire industry standard SMBus/I^2C interface. All commands, status and data are read or written from the host system via this interface.

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3.0 OPERATIONAL DESCRIPTION

3.1 A/D and Accumulator/Timer Operation

3.1.1 A/D CONVERSION CYCLE

When the A/D converter is enabled and active, it repeatedly performs a cycle of 1 to 8 conversions as programmed by the user through 8 A/D Control registers. These registers determine the input source, resolution, reference voltage source and sequence of conversions during an A/D converter cycle. During the cycle, the A/D logic accesses each register in sequence and performs the conversion specified by the bits within the register. This register contains an enable bit, a resolution field, a select bit for a single-ended or differential reference and a select field for the analog input mux. The results from each conversion are stored in one of eight corresponding16-bit result registers.

If the “enable” bit is set within a control register, a conversion will be performed. If it is disabled, that conversion will be skipped and the logic will move on to the next register. In this manner, the user can specify a sequence of conversions that will be performed during each A/D cycle.

As stated above, the input source for each of the registers is programmable. The 3-bit mux field within each control register selects one of seven possible input sources for the A/D conversion. The list of input sources is as follows:

- Charge/Discharge Current (voltage from SR pin to GND)
- Internal Temperature Sensor
- External Thermistor (constant current source on NTC pin)
- Battery Pack Voltage
- VC1 Voltage
- VC2 Voltage
- A/D Offset (conversion performed with input shorted internally to determine offset error associated with the converter)

However, the accumulator/timer functions are “hard wired” to specific A/D Result registers. For this reason, the control/result registers are given names which indicate their primary intended usage (see Table 3-1).

TABLE 3-1: A/D CONTROL/RESULT REGISTERS

A/D Register #	Control Register	Result Register	Intended Input Source
0	Ictrl	Ires	Battery Pack Current (via sense resistor)
1	ITctrl	ITres	Internal Temperature Sensor
2	ETctrl	ETres	External Temperature Sensor
3	VPctrl	VPres	Battery Pack Voltage (VC1 to GND)
4	VC1ctrl	VC1res	Battery Cell Voltage (VC1 to VC2)
5	VC2ctrl	VC2res	Battery Cell Voltage (VC2 to GND)
6	OFFSctrl	OFFSres	Internal A/D Offset Voltage (A/D input automatically internally shorted to GND)
7	AUXctrl	AUXres	Any

The 3-bit “resolution” field in each A/D Control register determines the resolution of the conversion, from a minimum of 9 bits (8 bits plus sign bit) to a maximum of 16 bits (15 bits plus sign bit). The time required to complete the conversion is a function of the number of bits of resolution (n) selected. The conversion time can be calculated as follows:

$$T_{ADC} = 30.52\ \mu s * 2^n$$

where:

“n” is the number of bits of resolution selected

The “Ref” bit selects the magnitude of the reference voltage. Either a ±340 mV or a ±170 mV reference is available. The ±170 mV reference is typically used for current readings and the ±340 mV reference for all other measurements.

The value of the LSB can be expressed as a function of the resolution selected as follows:

$$\text{A/D LSB} = 680/340\ \text{mV}/2^n$$

where:

“n” is the number of bits of resolution selected

The result value is given in sign/magnitude format (i.e., a sign bit with a 15-bit magnitude).

15	0
S	Magnitude

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3.1.2 CURRENT MEASUREMENT

Charge and discharge currents are measured using a 5 to 600 mΩ sense resistor that is connected between the SR and GND pins. The maximum input voltage at SR is ±150 mV. The sense resistor should be properly sized to accommodate the systems lowest and highest expected charge and discharge currents including suspend and/or standby currents.

In order to perform charge and discharge current measurements, the Ictrl register must be programmed with the SR pin as the analog input source. If charge and discharge accumulation is desired, the Ictrl and corresponding Ires registers should be used to select current measurement since the DCA, DTC, CCA and DCA registers are updated by the measurement results from the Ires register.

Ictrl programming in a typical application is as follows.

TABLE 3-2: Ictrl PROGRAMMING

Bit(s)	Name	Value	Function
7	En	1	Enables A/D conversion
6-4	Res	111	Selects 16-bit resolution
3	Ref	0	Selects ±170 mV reference
2-0	Sel	000	Selects VSR as converter input

Using the maximum resolution of 16 bits, the voltage value of the LSB is:

$$\text{A/D LSB} = 340\ \text{mV}/2^{16} = 5.19\ \mu\text{V}$$

Using a sense resistor value of 20 mΩ, the value of the LSB in units of current is:

$$5.19\ \mu\text{V}/20\ \text{m}\Omega = 259\ \mu\text{A}$$

3.1.3 VOLTAGE MEASUREMENTS

Analog mux inputs are provided to support measurement of individual cell and battery pack voltages. A/D control registers VPctrl, VC1ctrl and VC2ctrl are used to specify the measurement to be made. In typical applications, voltage measurement at the cell or pack level is done using the +340 mV reference and a resolution of 10 bits plus sign bit.

The value of the LSB in a pack voltage measurement using a 340 mV reference voltage is given by the formula:

$$V_{PACK}\ \text{LSB} = 10.2\text{V}/2^{n}$$

Where “n” is the resolution selected. For typical applications where n = 10:

$$V_{PACK}\ \text{LSB} = 10.2\text{V}/2^{10} = 10.2\text{V}/1024 = 9.96\ \text{mV}$$

The value of the LSB in a cell voltage measurement using a 340 mV reference voltage is given by the formula:

$$V_{CELL}\ \text{LSB} = 6.23\text{V}/2^{n}$$

Where “n” is the resolution selected. For typical applications where n = 10:

$$V_{CELL}\ \text{LSB} = 6.23\text{V}/2^{10} = 6.23\text{V}/1024 = 6.08\ \text{mV}$$

The following table shows LSB values for 9-bit plus sign resolution, so n = 9.

TABLE 3-3: LSB VALUES FOR 10-BIT RESOLUTION

Measurement	VR	Divider	Bits	LSB
VPACK	340	1/30	9 + sign	19.92
VCELL	340	1/18.33	9 + sign	12.17

VPctrl programming in a typical application is as follows.

TABLE 3-4: VPctrl PROGRAMMING

Bit(s)	Name	Value	Function
7	En	1	Enables A/D conversion
6-4	Res	001	Selects 10-bit resolution
3	Ref	1	Selects ±340 mV reference
2-0	Sel	011	Selects VSR as converter input

The input source fields for the VPctrl, VC1ctrl and VC2ctrl registers must be programmed to select pack voltage (on VC1), VC1 cell voltage and VC2 cell voltage in order for these registers to control their intended measurements.

3.1.4 TEMPERATURE MEASUREMENTS

A/D input channels are provided for temperature measurement using either the internal temperature sensor or an external thermistor.

3.1.4.1 Internal Temperature

The output of the internal temperature sensor is a voltage range with limits that correspond to operating temperature limits as follows:

-20°C $\rightarrow$ 239 mV
+70°C $\rightarrow$ 312 mV

The output voltage of the internal sensor as a function of temperature can be given as:

$$V_{IT}\ (\text{mV}) = 239 + 0.82 * (T + 20)$$

Defined within the ITctrl registers are the settings for the reference utilized and the resolution desired for measurement of temperature using the internal temperature sensor. Because of input voltage range described above, the 340 mV reference should be selected. Typically, 10-bit plus sign of resolution are selected which results in the following temperature resolution:

$$\text{LSB (Voltage)} = \text{Full Scale Range}/\#\ \text{of steps} = 340\ \text{mV}/2^{10} = 332\ \mu\text{V/LSB}$$

$$\text{LSB (°C)} = 332\ \mu\text{V/LSB} * (1 / 820)\ °\text{C}/\mu\text{V} = 0.404°\text{C/LSB}$$

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3.1.4.2 External Temperature

For temperature measurement using an external sensor, the NTC pin supplies a constant current source of 12.5 µA. For proper operation, an industry standard 10 kOhm at 25°C negative temperature coefficient (NTC) device of the 103ETBtype, should be connected between NTC and GND. The NTC reference output is only enabled during an external temperature measurement in order to minimize power consumption.

The output of the current source, connected to the external thermistor, produces a voltage range with limits that correspond to operating temperature limits, as follows:

-20°C $\rightarrow$ 263 mV
+70°C $\rightarrow$ 317 mV

The output voltage of the external sensor as a function of temperature can be given as:

V_{EX} (mV) = 263 + 0.6 * (T + 20)

Defined within the ETctrl registers are the settings for the reference utilized and the resolution desired for measurement of temperature using the external temperature sensor. Again, the 340 mV reference should be selected. The following temperature results in a 10-bit conversion:

LSB (Voltage) = Full Scale Range/# of steps
= 340 mV/2^{10} = 332 µV/LSB

LSB (°C) = 332 µV/LSB * (1/600)°C/µV
= 0.553°C/LSB

3.1.5 OFFSET COMPENSATION

The host software can perform offset compensation by using an offset measurement value read from the PS700. When the offset calibration is enabled within the OFFSctrl register, the converter inputs are internally shorted together and an A/D conversion is performed at the specified resolution. The offset value is stored in the OFFSres register.

3.1.6 ACCUMULATION/TIMING

The PS700 incorporates four 32-bit accumulators and four 32-bit elapsed time counters. The Discharge Current Accumulator (DCA) and the Charge Current Accumulator (CCA) are intended to record discharge and charge capacity values. The Discharge Time Counter (DTC) and the Charge Time Counter (CTC) are intended to maintain the total discharge time and charge time. Accumulated charge and discharge values can be used to determine state of charge of the battery as well as cycle count information. With information provided by the elapsed time counters, average charge and discharge currents over an extended period of time can be calculated.

Each of the four 32-bit accumulator registers is assigned a fixed “source” A/D Result register. When the accumulator is enabled, it is updated every 500 ms by adding the contents of the assigned result register value to the previous accumulator value. The accumulators are listed in Table 3-5 with their assigned source registers.

TABLE 3-5: ACCUMULATOR REGISTERS

Abbr.	Accumulator Name	Source
DCA	Discharge Current Accumulator	Ires (Sign bit = 1)
CCA	Charge Current Accumulator	Ires (Sign bit = 0)
TA	Temperature Accumulator	ITres or ETres
VC2A	VC2 Accumulator	VC2res

The resolution of the accumulated value is equal to the resolution selected for the associated conversion, up to a converter resolution of 15-bit plus sign. If a 15-bit plus sign A/D value is being accumulated, then the accumulator resolution in microvolt seconds is:

Accumulator LSB (µVs) = (Full Scale Range/# of steps) * 0.5s = (340 mV/2^{15}) * 0.5s = 5.19 µVs

3.1.7 CHARGE/DISCHARGE ACCUMULATORS

The DCA register is intended to accumulate discharge current and the CCA register is intended to accumulate charge current. Both use the Ires register as its source. For this reason, in most applications, current measurement defined in the A/D Control registers should be programmed to measure current by reading the voltage across the Sense Resistor pin (SR).

During charging, a negative voltage will exist across the SR pin to ground. Following a conversion, a positive voltage measurement results in the sign bit = 0 in the Ires register. When the sign bit = 0, the measured result will be added to the CCA register contents and the sum is returned to CCA.

In this way, the total charge current will be accumulated in CCA.

Similarly, during discharge, a positive voltage will exist between the SR pin and ground. In this case, the conversion will result with sign bit = 1 in the Ires register, indicating a negative value or discharge current condition. Under this condition, the DCA register will be updated with the discharge current measured during that conversion.

The value stored in the DCA or CCA register can be interpreted as illustrated in the following example. Using a 16-bit signed conversion for current measurement and a 20 mΩ sense resistor, the LSB can be expressed in units of capacity in micro amp seconds as follows:

Accumulator LSB (µAs) = Voltage LSB/R_{SENSE} = (2.59 µVs)/20 mΩ = 130 µAs

The “Accum” bit in the Accumctrl register must be enabled for accumulation to occur in both the CCA and DCA registers.

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3.1.8 CHARGE/DISCHARGE TIME COUNTERS

The Charge Time Counter (CTC) will increment at the rate of 2 counts every second as long as a negative voltage is measured at the SR pin. The CTC can thereby maintain a time count representing the total time that charge current has flowed into the battery.

The Discharge Time Counter (DTC) will increment at the rate of 2 counts every second as long as a positive voltage is measured at the SR pin. The DTC can thereby maintain a time count representing the total time that discharge current has flowed from the battery.

3.1.9 GENERAL PURPOSE ACCUMULATORS

There are two general purpose accumulators, TA and VC2A. For typical applications, these accumulators have been assigned specific functions. The user can redefine the use of these accumulators to fit the design requirements.

TA can be used to accumulate results from the ITres or ETres registers. Accumulation to TA must be enabled in the Accumctrl register bit “AccT”. The selection for accumulation of the values represented by the internal or external thermistor is also determined in the Accumctrl register bit “tsel”.

VC2A can be used to accumulate results from VC2res. Accumulation in VC2A must be enabled in the Accumctrl register bit “AccV”. The value stored in VC2res corresponds to the measurement as defined in the A/D Control register VC2ctrl. This function is utilized if the VC2 pin is configured as an independent A/D input and not connected to the cell stack.

The “Accum” bit in the Accumctrl register must be enabled for accumulation to occur in TA and VC2A.

3.1.10 GENERAL PURPOSE TIMERS

There are two general purpose timers that are enabled by accumulation in the TA and VC2A accumulators.

TAT is used to maintain a time count during accumulation in the TA register. This timer increments at a frequency of 2 counts every second.

VC2T is used to maintain a time count during accumulation in the VC2A register. This timer increments at a frequency of 2 counts every second.

3.2 Power Modes

The PS700 has four operational power modes: Run, Sample, Sample-Sleep and Shelf-Sleep. Each consumes power according to the configuration settings as described in the following sections.

3.2.1 RUN MODE

During Run mode, the PS700 performs continuous A/D conversion cycles per the programming of the A/D conversion cycle documented in **Section 3.1.1 “A/D Conversion Cycle”**. As described above, during each cycle, between 1 and 8 conversions are performed and the accumulators/time counters are updated as programmed by the user.

Run mode is entered following a Power-on Reset when the pack voltage (V_{PACK}) applied on the VC1 pin rises above the V_{POR} threshold. Run mode can also be entered from the Sample, Sample-Sleep and Shelf-Sleep modes as described below.

The PS700 will remain in Run mode as long as the pack voltage is above the V_{POR} threshold and the Sample, Sample-Sleep and Shelf-Sleep modes are not active.

3.2.2 SAMPLE MODE

In Sample mode, A/D measurements are not continuously performed as in Run mode. Instead, they are performed at a user selectable rate. The purpose of Sample mode is to reduce power consumption during periods of low rate charge or discharge. The power advantage of Sample mode comes from the reduction in frequency of A/D measurements.

Sample mode is entered by programming the “Samp” bit = 1 in the A/D Configuration register. The PS700 will remain in Sample mode as long as “Samp” bit = 1 and the VC1 voltage is above the V_{POR} threshold and the Sample-Sleep and Shelf-Sleep modes are not active. Run mode will be resumed when the Samp bit is cleared to ‘0’.

The Sample mode rate is selected using the “SampDiv” bits within the A/D Configuration register. The sample interval is 2**(SampDiv) * 0.5 sec. The possible sample rate intervals are as follows.

TABLE 3-6: SAMPLE RATE INTERVALS

“SampDiv”	Sample Interval
Value = 0	0.5s
Value = 1	1.0s
Value = 2	2.0s
Value = 3	4.0s
Value = 4	8.0s
Value = 5	16.0s
Value = 6	32.0s
Value = 7	64.0s

In Sample mode, much of the analog circuitry remains on. Therefore, the power savings are not as great as in Sample-Sleep mode (described below). Refer to **Section 6.0 “Electrical Characteristics”** for a specification of the amount of current consumed in Sample mode.

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3.2.3 SAMPLE-SLEEP MODE

In Sample-Sleep mode, the PS700 goes into the Sleep state and wakes up at user-programmed intervals to perform a set of conversions as programmed for the A/D cycle. The purpose of Sample-Sleep is to achieve the minimum power consumption possible while periodically measuring specified parameters.

While the PS700 is in the Sleep portion of Sample-Sleep interval, all of the analog circuitry is shut off. The Sleep interval time is driven by an independent low-power on-chip RC oscillator that is separate from the primary oscillator. The Sleep oscillator consumes much less power than the primary oscillator, but is less accurate. While in Sample-Sleep mode, the device consumes average current in the range of 20 µA. During the active portion of Sample-Sleep mode, a single set of conversions is performed and a Run mode current in the range of 85 µA will be consumed for the duration of the measurements.

Sample-Sleep mode is invoked by one of the following actions:

1. Cell voltage on VC1 or VC2 drops below the trip point programmed in the VCtrip register with the corresponding “VC1ent” or “VC2ent” bit set in the TRIPctrl register. This action can be used to prevent excessive battery discharge in the event of a dangerously low cell voltage. Be aware that Sample-Sleep will not be entered if the “Iex” bit is set, enabling wake-up based on charge current and the measured current is above the threshold set in the I+trip register.
2. Setting the SSLP bit in the OpMode register. The host can take this action when the system is entering a low-power standby condition and it is desired to periodically measure and accumulate current, voltage, or temperature.
3. Current less than the I-trip register value when “Ient” bit is set in the TRIPctrl register.

The Sample-Sleep interval is determined by the programming of the “Sampdiv” bits within the A/D Configuration register, together with the “SSLPdiv” bits within the OpMode register. The sample interval is 2**(Sampdiv) * 2**(SSLPdiv) * 0.5 sec. The possible Sample-Sleep interval time, therefore, ranges from a minimum of 0.5 sec to over 136 minutes.

Exit from Sample-Sleep mode to Run mode can be accomplished by clearing the “SSLP” bit or by programming a wake-up based on pack voltage or current. Wake-up based on charge current will occur when the “Iex” bit is set in the TRIPctrl register and the charging current value is above the threshold programmed in the I+trip register. Wake-up based on pack voltage will occur when the “VPex” bit is set in the TRIPctrl register and the pack voltage rises above the threshold programmed in the SStrip register.

3.2.4 SHELF-SLEEP MODE

Shelf-Sleep mode is the lowest power mode and is intended to preserve battery capacity when the battery pack is shipped or stored or if the battery voltage drops below a specified threshold. While in Shelf-Sleep mode, no measurements occur, no accumulation is performed and no SMBus communications are recognized. In addition, volatile memory is not maintained.

Entry to Shelf-Sleep mode is enabled by programming the “SHent” bit = 1 or if V_{PACK} is less than VPtrip. The Shelf-Sleep mode will then be entered when the SMBus pins (both SDA and SCL) drop from a high to a low level for a minimum time period specified by t_{SHELF}. This action will also occur if the battery pack is physically disconnected from the system.

Exit from the Shelf-Sleep mode back to Run mode will occur when the SMBus pins (both SDA and SCL) are both pulled from a low to high condition and remain high for a minimum time of t_{WAKE}, signifying system activity or the connection of the pack to the host.

3.3 General Purpose Input/Outputs

The NTC and VC2 pins have alternate functions of general purpose I/O; IO0 and IO1, respectively. These pins can be configured as digital general purpose inputs/outputs if their normal application functions of temperature and cell monitoring are not needed. Their configuration is controlled in the GPIOctrl register.

The IO0 (NTC) pin may be configured as a push-pull output, an open-drain driver with internal pull-up, or as a tri-stated pin. When configured as a push-pull or open-drain output, the output high voltage is the 3.0V internally regulated supply. When the output function is disabled, an external circuit may drive the pin as an input with a voltage range of 0-3.0V. The input function may be used whether or not the pin is driven by the PS700. In addition, the input function may be disabled, in which case the input buffer is powered down, preventing current drain if the NTC pin rests at an intermediate level.

The IO1 (VC2) pin is similar to that of NTC except it is an open-drain output only. IO1 has no explicit output enable control; therefore, if the output is set to a logic ‘1’, the internal pull-down is turned off which tri-states the pin. The input function is the same as IO0.

Note:	If the IO0 and/or IO1 pins are being used for their analog functions, their respective GPIO output and input functions must be disabled. The GPIO function may be totally disabled by clearing the appropriate GPIOctrl bit.

3.4 SMBus/I^{2}C Interface

The PS700 supports a 2-wire bidirectional bus and data transmission protocol that is fully compatible with the industry standard SMBus V1.1 based on the I^{2}C interface. This interface is used to read and write data from/to the on-chip registers and EEPROM. The device responds to the same SMBus slave address for access to all functions. The following is a brief overview of the SMBus/I^{2}C operational implementation in the PS700. Please refer to the SMBus v1.1 specification for complete operational details of this industry standard interface. This specification can be obtained at the SMBus Implementer's Forum web site at www.smbus.org.

3.4.1 SMBus OVERVIEW

SMBus is a two-wire multi-master bus, meaning that more than one device capable of controlling the bus can be connected to it. A master device initiates a bus transfer and provides the clock signals. A slave device can receive data provided by the master or can in return provide data to the master.

Since more than one device may attempt to take control of the bus as a master, SMBus provides an arbitration mechanism based on I^{2}C and relying on the wired-AND connection of all SMBus devices residing on the bus. If two or more masters try to place information on the bus, the first to produce a "one" when the other(s) produce a "zero" loses arbitration and has to release the bus.

The clock signals during arbitration are a wired-AND combination of all the clocks provided by SMBus masters. Bus clock signals from a master can only be altered by clock stretching or by other masters and only during a bus arbitration situation. In addition to bus arbitration, SMBus implements the I^{2}C method of clock low extending in order to accommodate devices of different speeds on the same bus.

SMBus version 1.1 can be implemented at any voltage between 3 and 5 Volts ±10%. Devices can be powered by the bus V_{DD} or by their own power source (such as Smart Batteries) and they will interoperate flawlessly as long as they adhere to the SMBus electrical specifications.

3.4.2 SMBus DATA TRANSFERS

A device that sends data onto the SMBus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a "master". The devices that are controlled by the master are "slaves". The SMBus must be controlled by a master device that generates the serial clock (SCL), controls the bus access and generates Start and Stop conditions. The PS700 operates as a slave on the two-wire bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL.

SMBus operates according to the following bus protocol:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

The SMBus specification defines the following bus conditions:

Bus Not Busy: Both data and clock lines remain high.

Start Data Transfer: A change in the state of the data line from high to low, while the clock is high, defines a Start condition.

Stop Data Transfer: A change in the state of the data line from low to high, while the clock line is high, defines the Stop condition.

Data Valid: The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between Start and Stop conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver Acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

A device that Acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the Stop condition.

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FIGURE 3-1: SMBus DATA TRANSFER

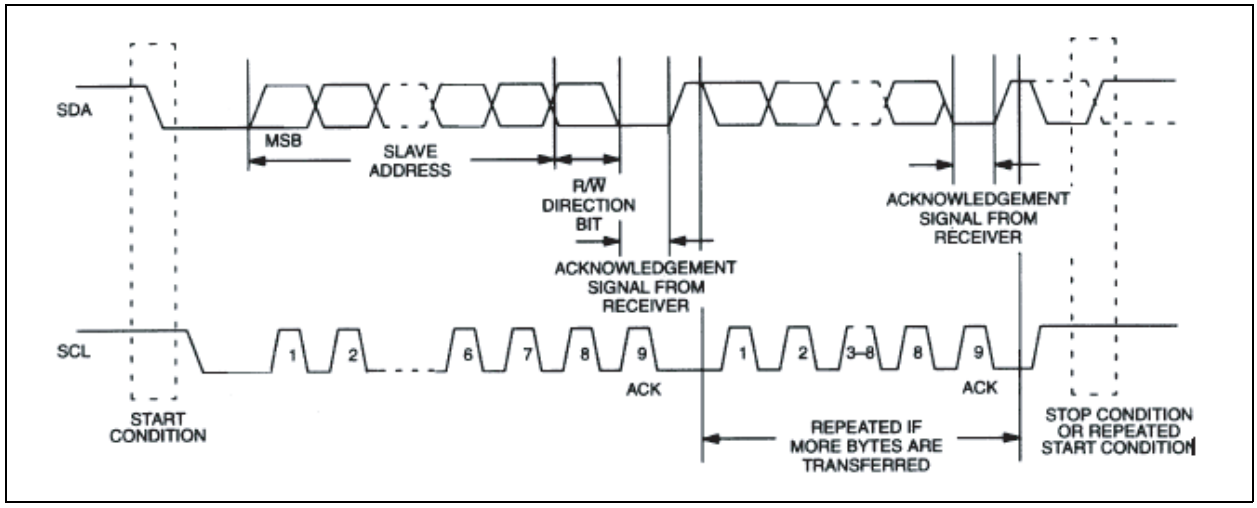


Figure 3-1 details how data transfer is accomplished on the SMBus. Depending upon the state of the R/W bit, two types of data transfer are possible:

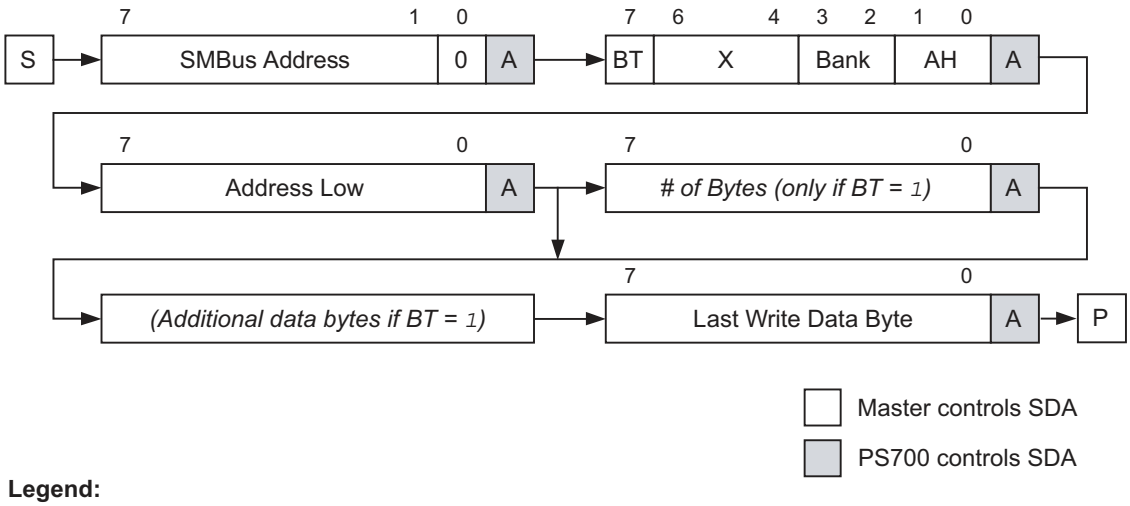
1. **Data transfer from a master transmitter to a slave receiver:** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an Acknowledge bit after each received byte.
2. **Data transfer from a slave transmitter to a master receiver:** The first byte (slave address) is transmitted by the master. The slave then returns an Acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an Acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'Not Acknowledge' is returned.

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer is ended with a Stop condition or with a Repeated Start condition. Since a Repeated Start condition is also the beginning of the next serial transfer, the bus will not be released.

The PS700 may operate in the following two modes:

1. **Slave Receiver mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an Acknowledge bit is transmitted. Start and Stop conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
2. **Slave Transmitter mode:** The first byte is received and handled as in the Slave Receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the PS700 while the serial clock is input on SCL. Start and Stop conditions are recognized as the beginning and end of a serial transfer.

FIGURE 3-2: PS700 SMBus WRITE TRANSACTION



Legend:

S	- Start
P	- Stop
RS	- Repeated Start
A	- Acknowledge
A	- Negative Acknowledge (terminates transaction)
BT	- Block mode indicator bit
Bank	- Controls selection of bank: 00: EEPROM 01: RAM/Registers 10: Reserved 11: Reserved
AH	- High-order address bits (2)
Address low	- Low-order address bits (8)

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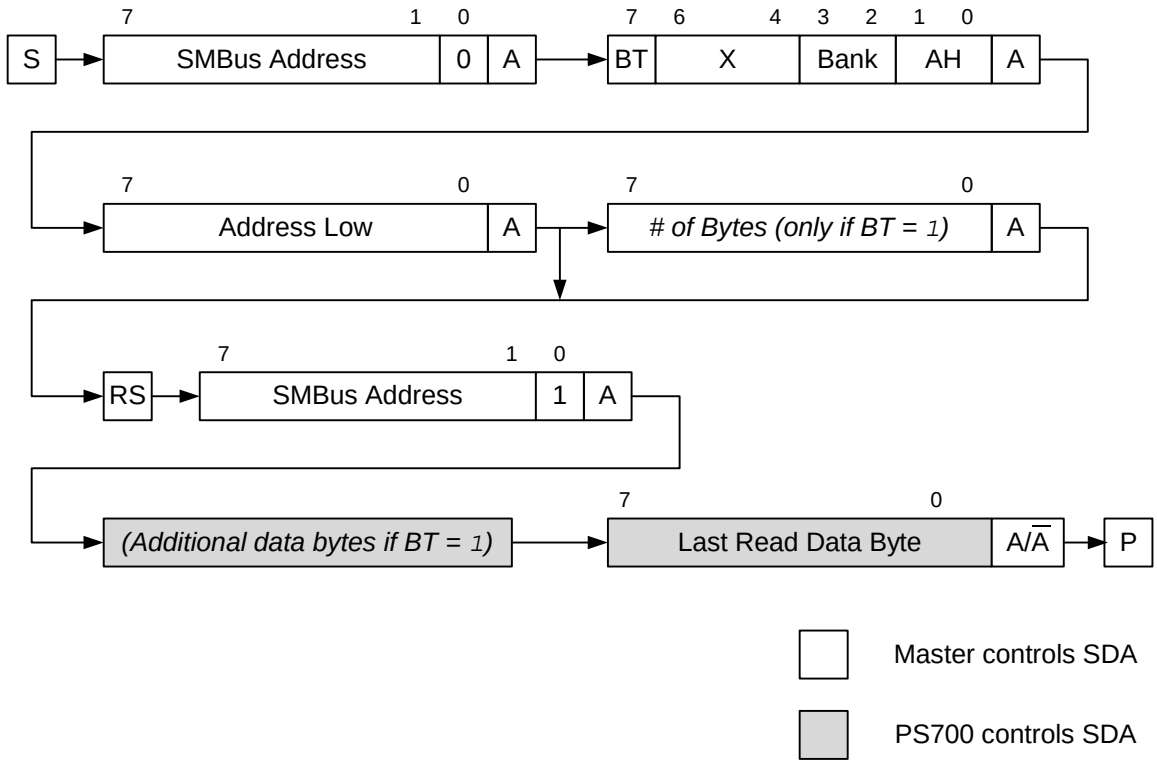
FIGURE 3-3: PS700 SMBus READ TRANSACTION



Legend:

S	- Start
P	- Stop
RS	- Repeated Start
A	- Acknowledge
$\overline{A}$	- Negative Acknowledge (terminates transaction)
BT	- Block mode indicator bit
Bank	- Controls selection of bank:
	00: EEPROM
	01: RAM/Registers
	10: Test Mode Registers
	11: Reserved
AH	- High-order address bits (2)
Address Low	- Low-order address bits (8)

4.0 MEMORY/OPERATIONAL REGISTER DESCRIPTION

4.1 Memory/Register Map

The PS700 internal structure is accessible on a strict memory mapped basis. The only action directly taken by the PS700 in response to an SMBus command is to read or write registers, RAM or EEPROM. Any actions taken by PS700 happen as a result of values written to internal control registers.

Addressing in PS700 consists of 10 bits plus two bank select bits. Therefore, there are a total of 4 Kbyte locations that are addressable within the PS700, organized as 4 banks of 1024 locations each. Bank 0 is dedicated to EEPROM, Bank 1 contains RAM/Registers, Bank 2 contains Test registers and Bank 3 is reserved.

Table 4-1 describes the PS700 memory map. The notation is y:0xzzz, where 'y' is the bank and 'zzz' is the address in hex.

4.2 EEPROM

The 512-byte EEPROM is located in Bank 0 and occupies addresses 0:0x000 to 0:0x1FF. All critical PS700 parameters, calibration factors and learned data are stored in the PS700 integrated EEPROM. See Table 4-2 for the PS700 EEPROM map. The EEPROM can be read using Byte or Block Transfer modes, but can only be written a byte at a time. Writing the EEPROM takes approximately 4 ms/byte. An EEPROM write cycle command from the SMBus is immediately Acknowledged by the PS700 if no other EEPROM write cycles are in progress. If a EEPROM write cycle is attempted while a previous request to write is in progress, a negative Acknowledge will be returned until the previous write cycle is completed. A EEPROM read cycle also results in a negative Acknowledge or an Acknowledge depending on whether or not a EEPROM write cycle is in progress

The data EEPROM does not write reliably at temperatures less than 0°C and supply voltages less than 3.3V. A read or write to a register or RAM location will not be affected by an EEPROM write cycle in progress.

4.3 General Purpose RAM

32 bytes of general purpose RAM are provided as temporary storage and are located in Bank 1 at 1:0x000 through 1:0x01F. The RAM may be read or written using either the Byte or Block Transfer modes.

4.4 Operational Registers

The following is a detailed description of all operational registers within the PS700 and all control, status, result bits and fields that are contained therein.

4.4.1 DCA – DISCHARGE COUNT ACCUMULATOR

The DCA is a 32-bit register that holds the total accumulated capacity discharged from the battery. Each time a conversion is performed with the sign bit of Ires = 1 and current accumulation is enabled, the measured value is added to DCA. As a result, the register is updated whenever a current measurement is performed with a negative voltage across the sense resistor (V_{SR} < GND).

The DCA register will rollover if it is allowed be updated beyond 0xFFFFFFFF, so proper register maintenance by the host system is necessary. The DCA register may be cleared using the ACCclr register bit, CLR0, described in Register 4-6.

4.4.2 DTC – DISCHARGE TIME COUNT REGISTER

The DTC records the length of accumulated time that the battery is in a discharge condition as indicated by a negative voltage on the SR pin. This register is incremented using a 2 Hz internal clock rate; therefore, the DTC is incremented at the rate of 2 counts per second or 7200 counts per hour so long as current accumulation is enabled and the Ires register returns a '1' in the sign bit following a current conversion.

The DTC register will rollover if it is allowed to count beyond 0xFFFFFFFF; therefore, proper register maintenance by the host system is necessary. The DTC register may be cleared using the ACCclr register bit, CLR1, described in Register 4-6.

4.4.3 CCA – CHARGE COUNT ACCUMULATOR

The CCA is a 32-bit register that holds the total accumulated current delivered as charge into the battery. Each time a current conversion is performed with the sign bit of Ires = 0 and current accumulation is enabled, the measured value is added to CCA. As a result, the register is updated whenever a current measurement is performed with a positive voltage across the sense resistor (V_{SR} > GND).

The CCA register will rollover if it is allowed to be updated beyond 0xFFFFFFFF; therefore, proper register maintenance by the host system is necessary. The CCA register may be cleared using the ACCclr register bit, CLR2, described below.

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TABLE 4-1: PS700 MEMORY MAP

Function	Byte 3	Byte 2	Byte 1	Byte 0	Bank:Address (Byte 0)
EEPROM					0:0x000
					0:0x004
	↓	↓	↓	↓	
					0:0x00C
	Register Initialization Values (Reserved Locations must = 0x00)				0:0x020
	↓	↓	↓	↓	
	Register Initialization Values (Reserved Locations must = 0x00)				0:0x084
					0:0x088
	↓	↓	↓	↓	
					0:0x1F8
					0:0x1FC
Reserved	Reserved				0:0x201
	↓		↓	↓	
	Reserved				0:0x3FC
General Purpose RAM					1:0x000
					1:0x004
					1:0x008
	↓	↓	↓	↓	
					1:0x018
					1:0x01C
Operational Registers: **Accumulators/ Timers, A/D Registers, Mode Control**	DCA				1:0x020
	DTC				1:0x024
	CCA				1:0x028
	CTC				1:0x02C
	TA				1:0x030
	TAT				1:0x034
	VC2A				1:0x038
	VC2T				1:0x03C
	ADconfig	Ictrl (ADc0)	Ires (ADr0)		1:0x040
	Reserved	ITctrl (ADc1)	ITres (ADr1)		1:0x044
		ETctrl (ADc2)	ETres (ADr2)		1:0x048
		VPctrl (ADc3)	VPres (ADr3)		1:0x04C
	GPIOctrl	VC1ctrl (ADc4)	VC1res (ADr4)		1:0x050
	Reserved	VC2ctrl (ADc5)	VC2res (ADr5)		1:0x054
		OFFSctrl (ADc6)	OFFSres (ADr6)		1:0x058
		AUXctrl (ADc7)	AUXres (ADr7)		1:0x05C
	ACCcontrol	ACCclr	I+trip		1:0x060
	Reserved	Reserved	I-trip		1:0x064
			VPtrip		1:0x068
			VCtrip		1:0x06C
			SStrip		1:0x070
		TRIPctrl	Reserved		1:0x074
		OpMode			1:0x078
		Reserved			1:0x07C
Reserved	Reserved				2:0x004
	↓	↓	↓	↓	
	Reserved				2:0x0FC
Cal/Setup Registers	MOsct	VREFT	VBGT	SMBAdd	2:0x080
	Reserved	AOsct	Reserved	Reserved	2:0x084
Reserved	Reserved				2:0x088
	↓	↓	↓	↓	
	Reserved				2:0x3FC
Reserved	Reserved				3:0x000
	↓	↓	↓	↓	
	Reserved				3:0x3FC

TABLE 4-2: P7 EEPROM

ADR	Name	LEN	Units	DFLT	Description
Unused					
0x00	(available)	(32)	—		(not used)
Factory					
0x88	PATTERN	2	—		EEPROM Pattern ID
0x8A	TESTER_ID	2	—		Tester Program ID/Version
0x8C	CAL_STATUS	1	—	0	Bit Flags – Calibration Status
0x8D	CF_CURR	2	—		Calibration Factor – Gain – Current
0x8F	CO_CURR	1	A/D		Calibration Factor – Offset – Current
0x90	CF_PACK	2	—		Calibration Factor – Gain – Pack
0x92	CF_VCELL1	2	—		Calibration Factor – Gain – VCELL1
0x94	CF_VCELL2	2	—		Calibration Factor – Gain – VCELL2
0x96	CO_PACK	1	A/D		Calibration Factor – Offset – Pack
0x97	CO_VCELL1	1	A/D		Calibration Factor – Offset – VCELL1
0x98	CO_VCELL2	1	A/D		Calibration Factor – Offset – VCELL2
0x99	CF_TEMPI	2	—		Calibration Factor – Gain – Internal Temperature
0x9B	CO_TEMPI	2	—		Calibration Factor – Offset – Internal Temperature
0x9D	CF_TEMPE	2	—		Calibration Factor – Gain – External Temperature
0x9F	CO_TEMPE	2	—		Calibration Factor – Offset – External Temperature
0xA1	RESERVED	4	—		Reserved
	TOTAL	**29**			
Fuel Gauge					
0xA5	VERSION	2	N/A	0x0101	Fuel Gauge Version Number
0xA7	VEOD	2	mV		EOD Voltage Threshold
0xA9	VEOC	2	mV		EOC Voltage Threshold
0xAB	IEOC	2	mA		EOC Current Threshold
0xAD	EOD_CAP	2	mAh		EOD Capacity
0xAF	MODE	1	bits		Fuel Gauge Mode Bits
0xB0	SERIAL_NO	2	N/A		Serial Number – Battery ID
0xB2	CAP_FULL	2	mAh		Full Charge Capacity
0xB4	CYCLES	2	cycles		Cycle Count
0xB6	VEOD_C	3	XmA		VEOD LUT Current Axis
0xB9	VEOD_T	7	XdegC		VEOD LUT Temperature Axis
0xC0	VEOD	32	XmV		VEOD Voltage Threshold(s)
0xE0	RCAP_T	7	XdegC		RCAP LUT – Residual Capacity Temperature Axis
0xE7	RCAP	8	XmAh		Residual Capacity
	TOTAL	**74**			
Unused					
0xEF	(available)	(17)			(not used)

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4.4.4 CTC – CHARGE TIME COUNT REGISTER

CTC records the length of accumulated time that the battery is in a charge condition as indicated by a positive voltage on the SR pin. This register is incremented using a 2 Hz internal clock rate; therefore, the CTC is incremented at the rate of 2 counts per second or 7200 counts per hour so long as current accumulation is enabled and the Ires register returns a '0' in the sign bit following a current conversion.

The CTC register will rollover if it is allowed to count beyond 0xFFFFFFFF; therefore, proper register maintenance by the host system is necessary. The CTC register may be cleared using the ACCclr register bit, CLR3, described below.

4.4.5 TA – TEMPERATURE ACCUMULATOR

TA is the accumulated 32-bit value of temperature measurements from the internal or external temperature sensor. TA is updated by the Itres or ETres registers. Selection of the internal temperature sensor, or external thermistor connected to the NTC pin, is made in the Accumctrl register, bit tsel.

The TA register will rollover if it is allowed be updated beyond 0xFFFFFFFF; therefore, proper register maintenance by the host system is necessary. The TA register may be cleared using the ACCclr register bit, CLR4, described below.

4.4.6 TAT – TEMPERATURE TIME COUNT REGISTER

The TAT register records the length of accumulated time that the PS700 is sensing temperature and accumulating the value in register TA. TAT is incremented using a 2 Hz internal clock rate and is incremented at the rate of 2 counts per second, or 7200 counts per hour, as long as temperature accumulation is enabled.

The TAT register will rollover if it is allowed to count beyond 0xFFFFFFFF; therefore, proper register maintenance by the host system is necessary. The TAT register may be cleared using the ACCclr register bit, CLR5, described below.

4.4.7 VC2A – VC2 ACCUMULATOR

VC2A is a 32-bit register that holds the total accumulated value measured on the VC2 pin. At the completion of each measurement, VC2A is incremented by the value of VC2res. This function is enabled when the Accumctrl register, bit AccV is a '1'.

The VC2A register will rollover if it is allowed to count beyond 0xFFFFFFFF; therefore, proper register maintenance by the host system is necessary. The VC2A register may be cleared using the ACCclr register bit, CLR6, described below.

4.4.8 VC2T – VC2 TIME COUNT REGISTER

VC2T records accumulated time for which measurements are taken on the VC2 pin. This register is incremented using a 2 Hz internal clock rate; therefore, VC2T is incremented at the rate of 2 counts per second or 7200 counts per hour.

The VC2T register will rollover if it is allowed to count beyond 0xFFFFFFFF; therefore, proper register maintenance by the host system is necessary. The VC2T register may be cleared using the ACCclr register bit, CLR7, described below.

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4.4.9 ADCONFIG – A/D CONFIGURATION REGISTER

REGISTER 4-1: ADCONFIG: A/D CONFIGURATION REGISTER (ADDRESS 43 HEX/67 DECIMAL)

ADEN	Samp	Reserved	SampDiv<2:0>
bit 7			bit 0

bit 7 **ADEN:** Master A/D Enable bit

If no conversions are desired, the A/D converter must be disabled using this bit.

1 = A/D conversions enabled
0 = A/D conversions disabled

bit 6 **Samp:** Sample Mode Enable bit

This bit controls the enabling of Sample mode when the PS700 is not in a Power-on Reset, Sample-Sleep or Shelf-Sleep mode. When set to '1', Sample mode is enabled and conversions will be performed at a periodic rate determined by the programming of the SampDiv bits. When cleared, Sample mode is disabled and the PS700 will operate in Run mode.

1 = Sample mode enabled
0 = Sample mode disabled

bit 5-3 **Reserved:** Reserved bit location

bit 2-0 **SampDiv:** Sample Period Interval bits

The SampDiv bits determine the interval between sample periods when the PS700 is operating in Sample mode. The programmed interval will be 2**(SampDiv) * 0.5 sec.

Legend:		
'1' = Bit is set	'0' = Bit is cleared	R = Reserved bit

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4.4.10 Accumctrl – ACCUMULATOR CONTROL REGISTER

REGISTER 4-2: Accumctrl: ACCUMULATOR CONTROL REGISTER (ADDRESS 63 HEX/99 DECIMAL)

Accum	Accl	AccT	AccV	tsel	Reserved
bit 7					bit 0

bit 7 **Accum:** Accumulator Master Enable bit

"Accum" is a master enable for Accl, AccT and AccV. If any combination of "Accl", "AccT" and "AccV" are enabled, Accum must also be enabled to permit accumulation. If "Accum" is '0', no accumulation will occur regardless of the settings in "Accl", "AccT" and "AccV".

1 = Accumulation enabled
0 = Accumulation disabled

bit 6 **Accl:** Current Accumulation Enable bit

When "Accl" is set to a '1', current accumulation is enabled. The DCA and CCA registers will periodically add the value of the Ires register. Also, the DCT and CCT elapsed time counter registers will count during discharge and charge, respectively. When "Accl" is cleared to '0', current accumulation is disabled.

1 = Current accumulation enabled
0 = Current accumulation disabled

bit 5 **AccT:** Accumulate Temperature Enable bit

When "Acct" is set to a '1', accumulation will be enabled in TA. TA will accumulate results from the AD5 Result register and the TAT elapsed time counter will increment. When "Acct" is cleared to '0', TA accumulation will be disabled.

1 = Accumulate temperature enabled
0 = Accumulate temperature disabled

bit 4 **AccV:** Accumulate Voltage from VC2 Enable bit

When "AccV" is '0', accumulation in TA will be updated by the VC1res register. When "AccV" is '1', accumulation in TA will be updated by the VC2res register.

bit 3 **tsel:** Temperature Selection bit

When "tsel" is '0', the internal temperature sensor is used for accumulation. When "tsel" is '1', the external temperature sensor is used for accumulation.

1 = External temperature sensor selected
0 = Internal temperature sensor selected

bit 2-0 **Reserved:** Reserved bit location

Legend:		
'1' = Bit is set	'0' = Bit is cleared	R = Reserved bit

4.4.11 A/D CONTROL REGISTERS

The eight A/D Control registers are defined as follows.

TABLE 4-3: A/D CONTROL REGISTERS

A/D Reg. #	Name	Function	Location (HEX)
ADc0	Ictrl	Current measurement control	42
ADc1	ITctrl	Internal temperature measurement control	46
ADc2	ETctrl	External temperature measurement control	4A
ADc3	VPctrl	Pack voltage measurement control	4E
ADc4	VC1ctrl	VC1 voltage measurement control	52
ADc5	VC2ctrl	VC2 voltage measurement control	56
ADc6	OFFSctrl	Offset measurement control	5A
ADc7	AUXctrl	Auxiliary measurement control	5E

The following register defines the bits contained in the eight A/D Control registers.

REGISTER 4-3: A/D CONTROL REGISTERS

Enable	Resolution	Reference	Select
bit 7			bit 0

bit 7 **Enable:** A/D Measurement Enable bit

A '1' in this bit enables the measurement defined by bits 0-6.

bit 6-4 **Resolution:** A/D Resolution Selection bits

These three bits control the resolution of the conversion performed for the corresponding A/D Result register as follows:

Resolution = 0: 8-bit + sign conversion
Resolution = 1: 9-bit + sign conversion
Resolution = 2: 10-bit + sign conversion
Resolution = 3: 11-bit + sign conversion
Resolution = 4: 12-bit + sign conversion
Resolution = 5: 13-bit + sign conversion
Resolution = 6: 14-bit + sign conversion
Resolution = 7: 15-bit + sign conversion

bit 3 **Reference:** A/D Reference Selection bit

Reference = 0: VR = 170 mV
Reference = 1: VR = 340 mV

bit 2-0 **Select:** A/D Input Selection bits

Selects the analog mux input for the pending conversion as follows:

Select = 0: Current (SR pin voltage)
Select = 1: Internal temperature sensor
Select = 2: External temperature sensor (NTC pin voltage)
Select = 3: VPACK (pack voltage)
Select = 4: VC1 voltage
Select = 5: VC2 voltage
Select = 6: Offset voltage
Select = 7: Offset voltage

Legend:		
'1' = Bit is set	'0' = Bit is cleared	R = Reserved bit

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In order for the A/D control registers to function according to their names, their select fields should be programmed as follows.

TABLE 4-4: A/D CONTROL REGISTER FUNCTIONS

A/D Reg. #	Name	Select Value
ADc0	Ictrl	0
ADc1	ITctrl	1
ADc2	ETctrl	2
ADc3	VPctrl	3
ADc4	VC1ctrl	4
ADc5	VC2ctrl	5
ADc6	OFFSctrl	6
ADc7	AUXctrl	X

4.4.12 A/D RESULT REGISTERS

The eight 16-bit ADres registers are defined as follows.

TABLE 4-5: A/D RESULT REGISTERS

A/D Reg. #	Name	Function	Location (HEX)
ADr0	Ictrl	Current measurement result	40
ADr1	ITctrl	Internal temperature measurement result	44
ADr2	ETctrl	External temperature measurement result	48
ADr3	VPctrl	Pack voltage measurement result	4C
ADr4	VC1ctrl	VC1 voltage measurement result	50
ADr5	VC2ctrl	VC2 voltage measurement result	54
ADr6	OFFSctrl	Offset measurement result	58
ADr7	AUXctrl	Auxiliary measurement result	5C

The following register defines the bits contained in the eight 16-bit ADres registers.

REGISTER 4-4: ADres REGISTERS

Sign	Magnitude
bit 15	bit 0

bit 15 **Sign:** Polarity of the A/D Measurement bit
The Sign bit shows the polarity of the given result where:
1 = The value is negative
0 = The value is positive

bit 14-0 **Magnitude:** Magnitude of A/D Output bits
Magnitude reports the value of the A/D measurement, with all '0's representing a 0 value and all '1's representing full scale.

Legend:		
'1' = Bit is set	'0' = Bit is cleared	R = Reserved bit

Note: The resolution bits, as defined in the ADctrl register, specify the measurement resolution and therefore, number of bits stored in the ADres registers. The value stored in the ADres registers is left justified. Bits beyond the selected resolution should be ignored.

4.4.13 GPIOctrl – GPIO CONTROL REGISTER

REGISTER 4-5: GPIOctrl: GPIO CONTROL REGISTER (ADDRESS 53 HEX/83 DECIMAL)

pp0	OE0	IE1	IE0	OUT1	OUT0	IN1	IN0
bit 7							bit 0

bit 7 **pp0:** Push-Pull Output IO0 bit

Setting this bit to a '1', with bit OE0 set to a '1', will configure the IO0 (NTC) pin as a push-pull digital output. If pp0 is a '0', with OE0 set to '1', the IE0 is an open-drain output with a 300 kOhm pull-up to internal V_{DD}.

bit 6 **OE0:** Output Enable IO0 bit

Setting this bit to a '1' will allow the PS700 to control NTC as either a push-pull (pp0 = 1) or open-drain (pp0 = 0) output. If OE0 is a '0', the NTC pin is tri-state (pp0 = 1) or pulled up to internal V_{DD} with a 300 kOhm resistor (pp0 = 0).

bit 5 **IE1:** Input Enable IO1 bit

Setting this bit to a '1' will enable IO1 (VC2) as a digital input. If IE1 is a '0', the digital input buffer on IO1 is powered down and IN1 will always read logic '0'.

bit 4 **IE0:** Input Enable IO0 bit

Setting this bit to a '1' will enable IO0 (NTC) as a digital input. If IE0 is a '0' the digital input buffer on IO0 is powered down and IN0 will always read logic '0'.

bit 3 **OUT1:** Output Data GPIO1 bit

Setting this bit to a '0' turns on the open-drain pull-down on IO1 (VC2) (forcing a logic '0' on the output). Setting this bit to a '1' turns off the pull-down resistor.

bit 2 **OUT0:** Output Data GPIO0 bit

If OE0 is a '1', the logic value of OUT0 is driven onto the IO0 (NTC) pin by the PS700.

bit 1 **IN1:** Input Data GPIO1 bit

Current logic state of the IO1 (VC2) pin (read-only).

bit 0 **IN0:** Input Data GPIO0 bit

Current logic state of the IO0 (NTC) (read-only).

Legend:		
'1' = Bit is set	'0' = Bit is cleared	R = Reserved bit

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4.4.14 ACCclr – ACCUMULATOR CLEAR REGISTER

A '1' in any ACCclr bits will clear the associated accumulator. Following the clear operation, all of the bits in ACCclr will be cleared to '0'.

REGISTER 4-6: ACCclr: ACCUMULATOR CLEAR REGISTER (ADDRESS 62 HEX/98 DECIMAL)

CLR7	CLR6	CLR5	CLR4	CLR3	CLR2	CLR1	CLR0
bit 7							bit 0

bit 7 **CLR7:** Clear Accumulator 7 bit
A '1' in this register will clear the VC2T accumulator.

bit 6 **CLR6:** Clear Accumulator 6 bit
A '1' in this register will clear the VC2A accumulator.

bit 5 **CLR5:** Clear Accumulator 5 bit
A '1' in this register will clear the TAT accumulator.

bit 4 **CLR4:** Clear Accumulator 4 bit
A '1' in this register will clear the TA accumulator.

bit 3 **CLR3:** Clear Accumulator 3 bit
A '1' in this register will clear the CTC accumulator.

bit 2 **CLR2:** Clear Accumulator 2 bit
A '1' in this register will clear the CCA accumulator.

bit 1 **CLR1:** Clear Accumulator 1 bit
A '1' in this register will clear the DTC accumulator.

bit 0 **CLR0:** Clear Accumulator 0 bit
A '1' in this register will clear the DCA accumulator.

Legend:		
'1' = Bit is set	'0' = Bit is cleared	R = Reserved bit

4.4.15 TPV – TRIP POINT VALUE REGISTERS

There are 5 registers that are utilized to set up Trip Point Values. These registers are used when enabled by the TRIPctrl register to enter or exit various power modes. Three of these Trip Point Value registers contain voltage values and two contain current values. The Trip Point Value registers, their corresponding Compare registers and their enable locations are listed below:

TPV Register	Location (HEX)	Comparison Register	Enable Bit
I+trip	60	Ires	Iex
I-trip	64	Ires	Ient
VPtrip	68	VPres	VPex
VCtrip	6C	VC1res or VC2res	VC1ent or VC2ent
SHtrip	70	VPres	SHent

VPtrip, VCtrip and SHtrip are used as voltage values to be compared to VPres, VC1res or VC2res and VPres, respectively, for transition in and out of various power modes. I+trip and I-trip are used as current values to be compared to Ires for transition in and out of various power modes. The format for data in these registers is left justified. For the purpose of this trip point, only magnitude is compared, the sign is ignored.

REGISTER 4-7: TPV: TRIP POINT VALUE REGISTERS

Sign	Magnitude
bit 15	bit 0

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4.4.16 OpMode – OPERATION MODE CONTROL REGISTER

REGISTER 4-8: OpMode: OPERATION MODE CONTROL REGISTER (ADDRESS 7A HEX/DECIMAL 122)

SSLP	Reserved	SSLPdiv	Shelf	POR	sPOR
bit 7					bit 0

bit 7 **SSLP:** Sample-Sleep Enable bit

Setting this bit to a '1' immediately enables Sample-Sleep mode. The low-power oscillator is enabled and the A/D sampling rate is reduced. Clearing this bit to '0' disables Sample-Sleep mode.

1 = Sample-Sleep mode enabled
0 = Sample-Sleep mode disabled

bit 6 **Reserved:** Reserved bit location

bit 5-3 **SSLPdiv:** Sample-Sleep Divider bits

These bits set the interval between sampling of the A/D during Sample-Sleep. The timing is set as: Sampling Interval = (.5 sec * 2 ** Sampdiv * 2 ** SSLPdiv)

bit 2 **SHELF:** Shelf-Sleep Enable bit

Writing a '1' to this register will place the device in Shelf-Sleep mode. Volatile memory will not be maintained. The Shelf-Sleep mode will not actually be entered until a SMBus Stop condition occurs and then SDA and SCL go low.

bit 1 **POR:** Power-on Reset bit

A '1' in this register indicates that a Power-on Reset has occurred. Write this register to '0' to clear this indicator.

bit 0 **sPOR:** Soft Power-on Reset bit

Writing a '1' to this register will cause the device to re-initialize by writing the contents of the EEPROM into all working registers.

Legend:		
'1' = Bit is set	'0' = Bit is cleared	R = Reserved bit

4.4.17 TRIPctrl – TRIP CONTROL REGISTERS

REGISTER 4-9: TRIPctrl: TRIP CONTROL REGISTERS (ADDRESS 76 HEX/118 DECIMAL)

lex	lent	VPex	VC1ent	VC2ent	SHent	Reserved	OV
bit 7							bit 0

bit 7 **Iex:** Current Exit from Sample-Sleep Mode bit

A '1' in this register will enable an exit from Sample-Sleep mode upon the following condition: **|**current**|** > I+trip.

bit 6 **Ient:** Enter Sample-Sleep Mode on Current bit

A '1' in this register will enable entry to Sample-Sleep mode under the following condition: **|**current**|** < I-trip.

bit 5 **VPex:** Pack Voltage Exit from Sample-Sleep Mode bit

A '1' in this register will enable an exit from Sample-Sleep mode upon the following condition: Pack Voltage > VPtrip.

bit 4 **VC1ent:** Enter Sample-Sleep Mode on VC1 Voltage bit

A '1' in this register will enable entry to Sample-Sleep mode upon the following condition: VC1 < VCtrip.

bit 3 **VC2ent:** Enter Sample-Sleep Mode on VC2 Voltage bit

A '1' in this register will enable entry to Sample-Sleep mode upon the following condition: VC2 < VCtrip.

bit 2 **SHent:** Enter Shelf-Sleep Mode on Pack Voltage bit

A '1' in this register will enable entry to Shelf-Sleep mode upon the following condition: $V_{PACK} < V_{SHENT}$

bit 1 **Reserved:** Reserved bit location

bit 0 **OV:** Overflow bit

PS700 sets this bit when the input voltage is greater than the maximum value of the voltage range for an A/D conversion.

Legend:		
'1' = Bit is set	'0' = Bit is cleared	R = Reserved bit

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4.5 Power-on Reset

When power is first applied to the VC1 input, the PS700 automatically executes a Power-on Reset sequence. The device is held in a Reset state while the voltage is below the minimum operating threshold, V_{POR}. When the voltage on the VC1 input rises above the V_{POR} threshold, the PS700 will initialize itself as described below. When initialization is complete, the PS700 will enter Run mode.

During the Power-on Reset sequence, the registers are loaded with initial values from EEPROM locations 0x020-0x087. These locations are reserved to contain register initialization values. In a battery pack application, a Power-on Reset typically happens only at the time of pack manufacture, when the cells are first connected to the battery monitoring pcb containing the PS700.

Data in the EEPROM locations, (Bank 0) 0:0x020-0:0x07F, will be loaded into the corresponding register locations in (Bank 1) 1:0x020-1:0x07F. Data in the EEPROM locations, (Bank 1) 0:0x080-0:0x084, will be loaded into the corresponding Cal/Setup register locations in (Bank 2) 2:0x080-2:0x084. **In all cases, EEPROM register initialization locations corresponding to "Reserved" register locations must contain the value of 0x00h in order to insure proper operation following a Power-on Reset.**

Note:	Do not overwrite the factory trimmed values.

4.6 Factory Register Initialization

The EEPROM register initialization locations are programmed with a set of default values at the time that the PS700 is manufactured. This programming results in the following general operational state of a PS700 following a Power-on Reset:

- All accumulators and time counters disabled and reset to '0'
- All A/D conversion disabled
- A/D registers programmed with their anticipated input source, resolution and input reference
- Sample and Shelf-Sleep modes disabled
- All Sample-Sleep mode entry methods disabled and trip point values zeroed
- GPIO inputs on VC2 and NTC disabled
- SMBus address = 0x16
- Factory calibrated trim values for band gap, voltage reference, auxiliary oscillator and main oscillator

Table 4-6 lists in detail the values that are programmed into the EEPROM register initialization locations.

TABLE 4-6: PS700 FACTORY REGISTER INITIALIZATION

Function	Byte 3	Byte 2	Byte 1	Byte 0	Bank:Address (Byte 0)
Operational Registers: Accumulators/ Timers A/D Registers Mode Control	DCA: 0x00000000				1:0x020
	DTC: 0x00000000				1:0x024
	CCA: 0x00000000				1:0x028
	CTC: 0x00000000				1:0x02C
	TA: 0x00000000				1:0x030
	TAT: 0x00000000				1:0x034
	VC2A: 0x00000000				1:0x038
	VC2T: 0x00000000				1:0x03C
	ADCONFIG: 00000000b = 0x00	Ictrl (ADc0): 01110000b = 0x70	Ires (ADr0): 0x0000		1:0x040
	Reserved 0x00	ITctrl (ADc1): 00101001b = 0x29	ITres (ADr1): 0x0000		1:0x044
		ETctrl (Adc2): 00101010b = 0x2A	ETres (ADr2): 0x0000		1:0x048
		VPctrl (ADc3): 00101011b = 0x2B	VPres (ADr3): 0x0000		1:0x04C
	GPIOctrl	VC1ctrl (ADc4): 00100100b = 0x24	VC1res (ADr4): 0x0000		1:0x050
	Reserved: 0x00	VC2ctrl (ADc5): 00100101b = 0x25	VC2res (ADr5): 0x0000		1:0x054
		OFFSctrl (ADc6): 01110110b = 0x76	OFFSres (ADr6): 0x0000		1:0x058
		AUXctrl (ADc7): 00000110b = 0x06	AUXres (ADr7): 0x0000		1:0x05C
	Accumctrl: 00000000b = 0x00	ACCclr: 00000000b = 0x00	I+trip: 0x0000		1:0x060
	Reserved: 0x00	Reserved: 0x00	I-trip: 0x0000		1:0x064
			VPtrip: 0x0000		1:0x068
			VCtrip: 0x0000		1:0x06C
			SStrip: 0x0000		1:0x070
		TRIPctrl: 00000000b = 0x00	Reserved: 0x00		1:0x074
		OpMode: 00000000b = 0x00			1:0x078
		Reserved: 00000000b = 0x00			1:0x07C
Cal/Setup Registers	MOsct: 0xxxxxxxb (‘xxxxxxx’ = factory trim value)	VREFT: 0xxxxxxxb (‘xxxxxxx’ = factory trim value)	VBGT: 0000xxxxb (‘xxxx’ = factory trim value)	SMBAdd: 00010110b	2:0x080
	Reserved: 0x00	AOsct: 000xxxxxb (‘xxxxxxx’ = factory trim value)	Reserved: 0x00	Reserved: 0x00	2:0x084

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5.0 CAL/SETUP MODE AND REGISTERS

Cal/Setup mode allows the designer to reprogram the default SMBus address and/or change the calibration parameters programmed at the factory for band gap, voltage reference and main oscillator trim values.

Entering Cal/Setup mode requires the host to request three consecutive and specific incorrect SMBus addresses with no interruptions between requests. These addresses are:

Addr1	HEX 50
Addr2	HEX 52
Addr3	HEX 74

After each address is sent, the PS700 will NACK the address. Once the sequence is complete, the PS700 will enter Cal/Setup mode and allow access to the Cal/Setup registers located in memory Bank 2.

To exit Cal/Setup mode, re-enter the same address sequence or power-down the part. The PS700 will always power-up with Cal/Setup mode disabled.

The following registers are only available in Cal/Setup mode.

5.1 Cal/Setup Mode Registers

REGISTER 5-1: SMBAdd: SMBus ADDRESS REGISTERS (ADDRESS 80 HEX/128 DECIMAL)

SMBAdd	Reserved
bit 7	bit 0

bit 7-1 **SMBAdd:** SMBus Address Register bits
The value placed in bits <7:1> of this register defines the SMBus address for this device.

bit 0 **Reserved:** Reserved bit location

Legend:		
'1' = Bit is set	'0' = Bit is cleared	R = Reserved bit

REGISTER 5-2: V_{BGT}: BAND GAP TRIM REGISTER (ADDRESS 81 HEX/129 DECIMAL)

Reserved	V_{BGT}
bit 7	bit 0

bit 7-4 **Reserved:** Reserved bit location

bit 3-0 **V_{BGT}:** Band Gap Voltage Trim bits
This value is set by the factory.

Legend:		
'1' = Bit is set	'0' = Bit is cleared	R = Reserved bit

REGISTER 5-3: VREFT: VOLTAGE REFERENCE TRIM REGISTER (ADDRESS 82 HEX/130 DECIMAL)

GPIOen1	GPIOen0	VREFT
bit 7		bit 0

bit 7 **GPIOen1:** Enable VCELL2 as GPIO bit

Writing this bit to a '1' will configure the VCELL2 pin as a GPIO. If enabled as GPIO, the accumulation function in the Accumctrl register and the trip function in the TRIPctrl register should be disabled.

bit 6 **GPIOen0:** Enable NTC as GPIO bit

Writing this register to a '1' will configure the NTC pin as a GPIO. If enabled as GPIO, the accumulation function in the Accumctrl register should be disabled.

bit 5-0 **VREFT:** Voltage Reference Trim bits

Bits 5-0 of this register store the trim value for both the +340 mV and ±170 mV references. This value is factory programmed.

Legend:		
'1' = Bit is set	'0' = Bit is cleared	R = Reserved bit

REGISTER 5-4: MOsct: MAIN OSCILLATOR TRIM REGISTER (ADDRESS 83 HEX/131 DECIMAL)

ROSC_sel	MOsct
bit 7	bit 0

bit 7 **Rosc_sel:** Resistor Oscillator Select bit

Writing this register to a '1' requires the use of a low temperature coefficient 221 kΩ resistor on the ROSC pin. Writing this register to a '0' will allow the use of an internal 221 kΩ resistor. (The precision of the internal time base will be affected by the selection of the resistor with the lowest variance of resistance over the systems operating range.)

bit 6-0 **MOsct:** Main Oscillator Trim bits

Bits 0-6 of this register are used to trim the internal time base. This value is factory programmed.

Legend:		
'1' = Bit is set	'0' = Bit is cleared	R = Reserved bit

REGISTER 5-5: AOsct: AUXILIARY OSCILLATOR TRIM REGISTER (ADDRESS 86 HEX/134 DECIMAL)

Reserved	AOsct
bit 7	bit 0

bit 7-5 **Reserved:** Reserved bit location

bit 4-0 **AOsct:** Auxiliary Oscillator Trim bits

Trim bits for the secondary oscillator used in low-power modes.

Legend:		
'1' = Bit is set	'0' = Bit is cleared	R = Reserved bit

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6.0 ELECTRICAL CHARACTERISTICS

TABLE 6-1: ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
VCx	Voltage at any VC(x) pin	-0.5	10.0	V
VPIN	Voltage directly at any pin (except VCELLX)	-0.5	7.0	V
TBIAS	Temperature under bias	-20	85	°C
TSTORAGE	Storage temperature (package dependent)	-35	120	°C

Note: These are stress ratings only. Stress greater than the listed ratings may cause permanent damage to the device. Exposure to absolute maximum ratings for an extended period may affect device reliability. Functional operation is implied only at the listed operating conditions below.

TABLE 6-2: DC CHARACTERISTICS (T_A = -20°C TO +85°C; V_{DD} (INTERNAL) = +3.3V ±10%)

Symbol	Description	Min	Typ.	Max	Units	Condition
VC1	Supply Voltage	2.7	—	9.0	V	
VDD	Internal Regulated Supply Voltage	—	3.3	—	V	
IDD	Supply Current – Run mode	—	80	190	µA	A/D active **(Note 1)**
IDDINS	Supply Current – Sample mode	—	45	—	µA	A/D inactive **(Note 1, 2)**
IDDSLP	Supply Current – Sample-Sleep mode	—	20	—	µA	Sample-Sleep mode **(Note 1)**
IDDSSLP	Supply Current – Shelf-Sleep mode	—	300	—	nA	Shelf-Sleep mode **(Note 1)**
VIL	Input Low Voltage – IO0, IO1	—	—	0.2 * VDD	V	
VIH	Input High Voltage – IO0, IO1	0.8 * VDD	—	—	V	
IIL-IOPU	GPIO Input Low Current – Pull-up mode	—	7	—	µA	
IL-IO	Leakage Current – IO pins programmed as outputs or inputs without pull-up	—	1	2	µA	
VOL-IO	Output Low Voltage for IO1, IO0	—	—	0.4	V	IOL = 0.5 mA
VOH-IO	Output High Voltage for IO1 configured as push-pull	2.0	—	—	V	IOH = 100 µA
VSR	Sense Resistor Input Voltage Range	-150	—	150	mV	VR = 170 mV
INTC	Thermistor Output Current	—	12.5	—	µA	
VIL-SMB	Input Low Voltage for SMBus pins	-0.5	—	0.8	V	
VIH-SMB	Input High Voltage for SMBus pins	2.0	—	5.5	V	
VOL-SMB	Output Low Voltage for SMBus pins	—	—	0.4	V	IPULLUP = 350 µA
VOH-SMB	Output High Voltage for SMBus pins	2.1	—	5.5	V	
IPULLUP-SMB	Current through Pull-up Resistor or Current Source for SMBus pins	100	—	350	µA	
ILEAK-SMB	Input Leakage Current – SMBus pins	—	—	±8	µA	

Note 1: Does not include current consumption due to external loading on pins.

2: Sample mode current is specified during an A/D inactive cycle. Sample mode average current can be calculated using the formula: Average Sample Mode Supply Current = (IDDRUN + (n – 1) * IDDINS)/n; where “n” is the programmed sample rate.

TABLE 6-3: AC CHARACTERISTICS (T_A = -20°C TO +85°C; V_{DD} (INTERNAL) = +3.3V ± 10%)

Symbol	Description	Min	Typ.	Max	Units	Condition
f_{RC}	Internal RC Oscillator Frequency	130,613	131,072	131,530	Hz	
$f_{A/D}$	Internal A/D Operating Clock	—	$f_{RC}/4$	—	Hz	
t_{POR}	Power-on Reset Delay	—	2	10	ms	Delay from time when VC1 voltage exceeds 2.7V
t_{SHELF}	Delay to entry of Shelf-Sleep mode	1	—	—	ms	(SHent = 1 or V_{PACK} < VPtrip) and (SDA and SCL go low)
t_{WAKE}	Delay to exit of Shelf-Sleep mode	1	—	—	ms	SDA and SCL go high

TABLE 6-4: AC CHARACTERISTICS – SMBus (T_A = -20°C TO +85°C; V_{DD} (INTERNAL) = +3.3V ± 10%)

Symbol	Description	Min	Typ.	Max	Units	Condition
f_{SMB}	SMBus Clock Operating Frequency	10	—	100	kHz	Slave mode
t_{BUF}	Bus Free Time between Start and Stop	4.7	—	—	µs	
t_{SHLD}	Bus Hold Time after Repeated Start	4.0	—	—	µs	
$t_{SU:STA}$	Setup Time before Repeated Start	4.7	—	—	µs	
$t_{SU:STOP}$	Stop Setup Time	4.0	—	—	µs	
t_{HLD}	Data Hold Time	0	—	—	ns	
t_{SETUP}	Data Setup Time	250	—	—	ns	
t_{LOW}	Clock Low Period	4.7	—	—	µs	
t_{HIGH}	Clock High Period	4.0	—	50	µs	**(Note 1)**
$t_{LOW:SEXT}$	Message Buffering Time	—	—	10	ms	**(Note 2)**
$t_{HIGH:MEXT}$	Message Buffering Time	—	—	10	ms	**(Note 3)**
t_F	Clock/Data Fall Time	—	—	300	ns	**(Note 4)**
t_R	Clock/Data Rise Time	—	—	1000	ns	**(Note 4)**

Note 1: t_{HIGH} max. provides a simple, ensured method for devices to detect bus Idle conditions.

2: $t_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to the stop.

3: $t_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from Start-to-Ack, Ack-to-Ack or Ack-to-Stop.

4: Rise and fall time is defined as follows: $t_R = (V_{ILMAX} – 0.15)$ to $(V_{IHMIN} + 0.15)$

$t_F = 0.9V_{DD}$ to $(V_{ILMAX} – 0.15)$

TABLE 6-5: A/D CONVERTER CHARACTERISTICS (T_A = -20°C TO +85°C; V_{REG} (INTERNAL) = +3.3V ±10%)

Symbol	Description	Min	Typ.	Max	Units	Condition
AD_{RES}	A/D Converter Resolution	9	—	16	bits	**(Note 1)**
t_{CONV}	A/D Conversion Measurement Time, n-bit	—	$2^{(n+1)}/f_{A/D}$	—	s	
V_{ADIN}	A/D Converter Input Voltage Range (internal)	-152	—	152	mV	VR = 170 mV
		0	—	309	mV	VR = 340 mV
E_{VGAIN}	Supply Voltage Gain Error	—	—	0.100	%	
$E_{VOFFSET}$	Compensated Offset Error	—	—	0.100	%	
E_{TEMP}	Temperature Gain Error	—	—	0.100	%	
E_{INL}	Integrated Nonlinearity Error	—	—	0.004	%	

Note 1: Voltage is internal at A/D converter inputs. V_{SR} and V_{NTC} are measured directly. VC(x) inputs are measured using internal level translation circuitry that scales the input voltage range appropriately for the converter.

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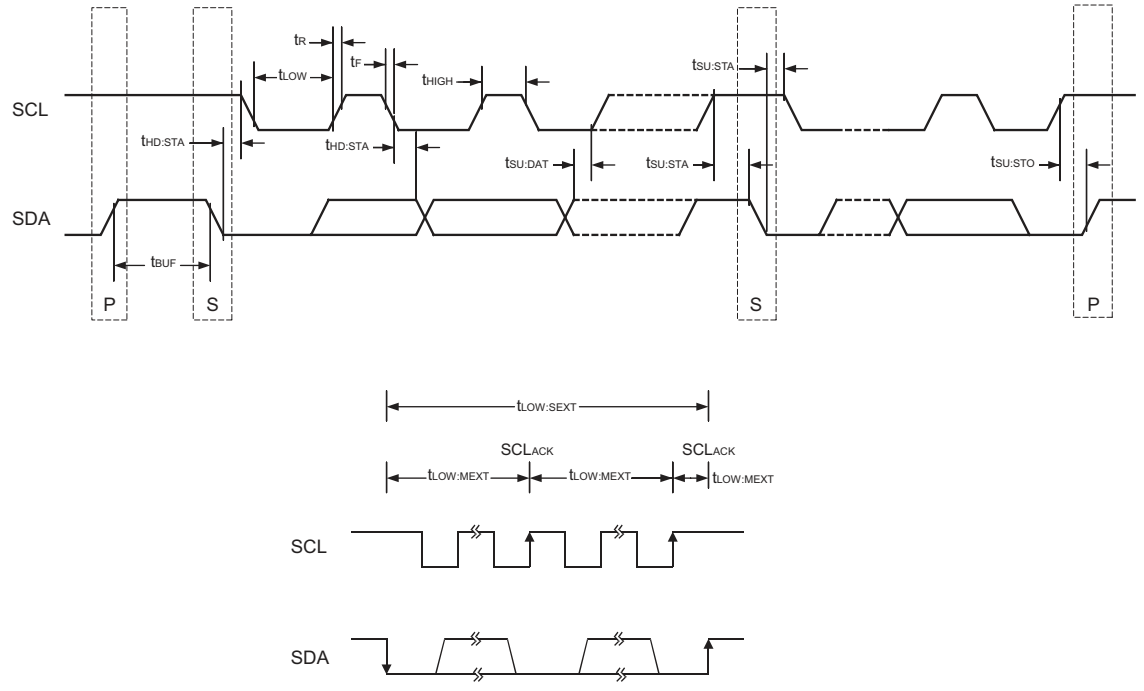
FIGURE 6-1: SMBus AC TIMING DIAGRAMS



Note: SCLACK is the Acknowledge related clock pulse generated by the master.

TABLE 6-6: SILICON TIME BASE CHARACTERISTICS (T_A = -20°C TO +85°C; V_{REG} (INTERNAL) = +3.3V ±10%)

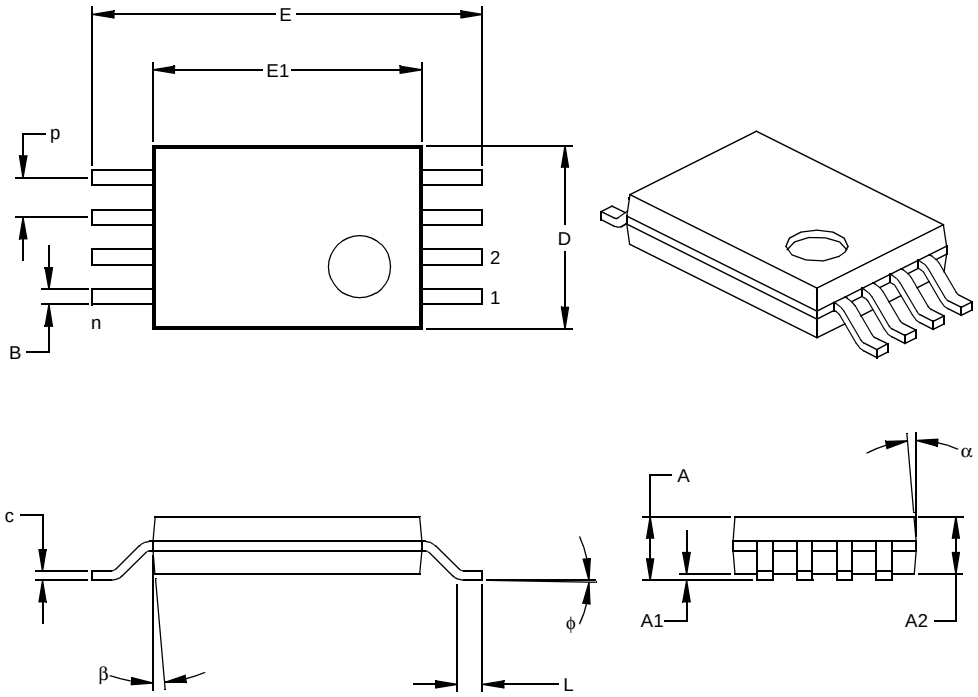
Symbol	Description	Min	Typ.	Max	Units	Condition
ETIME	Silicon Time Base Error			0.35	%	Bias resistor ROSC tolerance = 1%, TL = ±25 ppm

TABLE 6-7: TEMPERATURE MEASUREMENT ACCURACY (T_A = -20°C TO +85°C; V_{REG} (INTERNAL) = +3.3V ±10%)

Symbol	Description	Min	Typ.	Max	Units	Condition
TRES	Reported Temperature Resolution	—	1	—	°K	
TACC	Reported Temperature Accuracy	-3	—	3	°K	
TDRIFT	Reported Temperature Drift	—	-2	—	°K/V	

7.0 PACKAGING INFORMATION

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-086

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APPENDIX A: PS700 DATA SHEET REVISION HISTORY

Revision A-B (July 2003)

Removed Preliminary condition tag. Updated Figure 3-3 (page 13). Changed format of all operational registers in **Section 4.4 "Operational Registers"**.

Revision B-C (April 2004)

Removed PEC – pages 1, 10, 12 (Figure 3-2) and 13 (Figure 3-3). Removed NiMH 3-6 cell – pages 1, 2 and 4. Updated Figure 1-2 – page 3. Removed independent A/D input on pin 1 – page 3. Changed resolution nomenclature to bit + sign – pages 5 and 20 (Register 4-3). Added Table 3-3 – page 6. Added **Section 3.1.4.1 "Internal Temperature"** and **Section 3.1.4.2 "External Temperature"**. In **Section 3.2.2 "Sample Mode"**, added Sample-Sleep entry exception – page 9. Updated memory map, Table 4-1 – page 15. Added Table 4-2: PS700 EEPROM Map – page 16. Changed SMBus address factory default from 0x06 to 0x16 – pages 27 and 28.

Revision C-D (May 2004)

Operating temperature typo correction, 70°C to 85°C – pages 32 and 33.

Revision D-E (July 2004)

Corrected errors in **Section 3.1.4.2 "External Temperature"**. Changed internal to external and corrected V_{EX} equation. Added **Appendix A "Revision History"**. Changed value of Bits column in Table 3-3 from "10" to "9 + sign". Changed reference to "10 bits of resolution" in **Section 3.1.4.1 "Internal Temperature"** to "10-bit plus sign of resolution". Changed references to "16 bits of resolution" in **Section 3.1.6 "Accumulation/ Timing"** to "15-bit plus sign". Added information to **Section 4.2 "EEPROM"** about temperature and voltage limits for data EEPROM writes.

Revision F (August 2004)

Corrected errors in Features section, Shelf-Sleep mode. Corrected errors in **Section 2.6 "A/D Converter"** and **Section 3.1.1 "A/D Conversion Cycle"**. Updated accumulator equation in **Section 3.1.6 "Accumulation/ Timing"**. Changed V_{SR} values in Table 6-2.

NOTES:

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