

5 V ECL ÷4 Divider

MC10EL33, MC100EL33

Description

The MC10EL/100EL33 is an integrated ÷4 divider. The differential clock inputs and the V_{BB} allow a differential, single-ended or AC coupled interface to the device. The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset allows for the synchronization of multiple EL33's in a system.

The 100 Series contains temperature compensation.

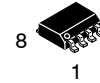
Features

- 650 ps Propagation Delay
- 4.0 GHz Toggle Frequency
- ESD Protection:
 - ◆ > 1 kV Human Body Model
 - ◆ > 100 V Machine Model
- PECL Mode Operating Range: $V_{CC} = 4.2 \text{ V}$ to 5.7 V with $V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range: $V_{CC} = 0 \text{ V}$ with $V_{EE} = -4.2 \text{ V}$ to -5.7 V
- Internal Input Pulldown Resistors on CLK(s) and R.
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity:
 - ◆ Level 1 for SOIC-8 NB
 - ◆ For Additional Information, see Application Note [AND8003/D](#)
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 95 Devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



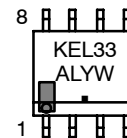
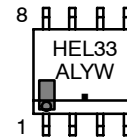
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SOIC-8 NB
D SUFFIX
CASE 751-07

MARKING DIAGRAM



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
■ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

| Device | Package | Shipping |
|-------------|---------------------|-----------------|
| MC10EL33DG | SOIC-8 (Pb-Free) | 98 Units / Tube |
| MC100EL33DG | SOIC-8 (Pb-Free) | 98 Units / Tube |

MC10EL33, MC100EL33

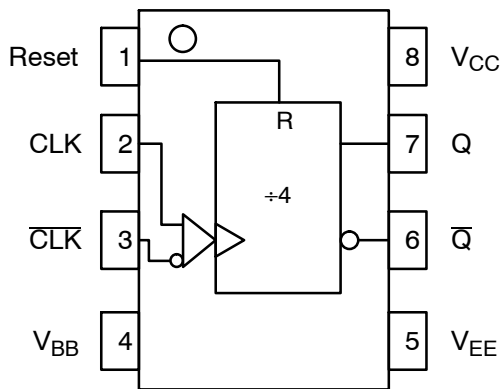


Table 1. PIN DESCRIPTION

| Pin | Function |
|------------------------------|--------------------------|
| CLK, $\overline{\text{CLK}}$ | ECL Clock Inputs* |
| Reset | ECL Asynch Reset* |
| Q, $\overline{\text{Q}}$ | ECL Data Outputs |
| V_{BB} | Reference Voltage Output |
| V_{CC} | Positive Supply |
| V_{EE} | Negative Supply |

*Pins will default low when left open.

Figure 1. Logic Diagram and Pinout Assignment

Table 2. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|----------------------|--|--|--|-------------|-----------------------------|
| V_{CC} | PECL Mode Power Supply | $V_{\text{EE}} = 0 \text{ V}$ | | 8 | V |
| V_{EE} | NECL Mode Power Supply | $V_{\text{CC}} = 0 \text{ V}$ | | -8 | V |
| V_{I} | PECL Mode Input Voltage NECL Mode Input Voltage | $V_{\text{EE}} = 0 \text{ V}$ $V_{\text{CC}} = 0 \text{ V}$ | $V_{\text{I}} \leq V_{\text{CC}}$ $V_{\text{I}} \geq V_{\text{EE}}$ | 6 -6 | V |
| I_{out} | Output Current | Continuous Surge | | 50 100 | mA |
| I_{BB} | V_{BB} Sink/Source | | | ± 0.5 | mA |
| T_{A} | Operating Temperature Range | | | -40 to +85 | $^{\circ}\text{C}$ |
| T_{stg} | Storage Temperature Range | | | -65 to +150 | $^{\circ}\text{C}$ |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | SOIC-8 NB SOIC-8 NB | 190 130 | $^{\circ}\text{C}/\text{W}$ |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | SOIC-8 NB | 41 to 44 | $^{\circ}\text{C}/\text{W}$ |
| T_{sol} | Wave Solder (Pb-Free) | < 2 to 3 sec @ 260 $^{\circ}\text{C}$ | | 265 | $^{\circ}\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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Table 3. 10EL SERIES PECL DC CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$; $V_{EE} = 0.0\text{ V}$ (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------|------|------|------|------|------|------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 27 | 33 | | 27 | 33 | | 27 | 33 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | 3920 | 4010 | 4110 | 4020 | 4105 | 4190 | 4090 | 4185 | 4280 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | 3050 | 3200 | 3350 | 3050 | 3210 | 3370 | 3050 | 3227 | 3405 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 3770 | | 4110 | 3870 | | 4190 | 3940 | | 4280 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 3050 | | 3500 | 3050 | | 3520 | 3050 | | 3555 | mV |
| V_{BB} | Output Voltage Reference | 3.57 | | 3.7 | 3.65 | | 3.75 | 3.69 | | 3.81 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 2.5 | | 4.6 | 2.5 | | 4.6 | 2.5 | | 4.6 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | | | 0.5 | | | 0.3 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.25 V / -0.5 V.
2. Outputs are terminated through a 50 Ω resistor to $V_{CC} - 2.0\text{ V}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1 V.

Table 4. 10EL SERIES NECL DC CHARACTERISTICS ($V_{CC} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 27 | 33 | | 27 | 33 | | 27 | 33 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | -1080 | -990 | -890 | -980 | -895 | -810 | -910 | -815 | -720 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | -1950 | -1800 | -1650 | -1950 | -1790 | -1630 | -1950 | -1773 | -1595 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1230 | | -890 | -1130 | | -810 | -1060 | | -720 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1950 | | -1500 | -1950 | | -1480 | -1950 | | -1445 | mV |
| V_{BB} | Output Voltage Reference | -1.43 | | -1.30 | -1.35 | | -1.25 | -1.31 | | -1.19 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | -2.5 | | -0.4 | -2.5 | | -0.4 | -2.5 | | -0.4 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | | | 0.5 | | | 0.3 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.25 V / -0.5 V.
2. Outputs are terminated through a 50 Ω resistor to $V_{CC} - 2.0\text{ V}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1 V.

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Table 5. 100EL SERIES PECL DC CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$; $V_{EE} = 0.0\text{ V}$ (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------|------|------|------|------|------|------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 27 | 33 | | 27 | 33 | | 31 | 37 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | 3915 | 3995 | 4120 | 3975 | 4045 | 4120 | 3975 | 4050 | 4120 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | 3170 | 3305 | 3445 | 3190 | 3295 | 3380 | 3190 | 3295 | 3380 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 3835 | | 4120 | 3835 | | 4120 | 3835 | | 4120 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 3190 | | 3525 | 3190 | | 3525 | 3190 | | 3525 | mV |
| V_{BB} | Output Voltage Reference | 3.62 | | 3.74 | 3.62 | | 3.74 | 3.62 | | 3.74 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 2.5 | | 4.6 | 2.5 | | 4.6 | 2.5 | | 4.6 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.8 V / -0.5 V.
2. Outputs are terminated through a 50 Ω resistor to $V_{CC} - 2.0\text{ V}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1 V.

Table 6. 100EL SERIES NECL DC CHARACTERISTICS ($V_{CC} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 27 | 33 | | 27 | 33 | | 31 | 37 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | -1085 | -1005 | -880 | -1025 | -955 | -880 | -1025 | -955 | -880 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | -1830 | -1695 | -1555 | -1810 | -1705 | -1620 | -1810 | -1705 | -1620 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1165 | | -880 | -1165 | | -880 | -1165 | | -880 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1810 | | -1475 | -1810 | | -1475 | -1810 | | -1475 | mV |
| V_{BB} | Output Voltage Reference | -1.38 | | -1.26 | -1.38 | | -1.26 | -1.38 | | -1.26 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | -2.5 | | -0.4 | -2.5 | | -0.4 | -2.5 | | -0.4 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.8 V / -0.5 V.
2. Outputs are terminated through a 50 Ω resistor to $V_{CC} - 2.0\text{ V}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1 V.

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Table 7. AC CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$; $V_{EE} = 0.0\text{ V}$ or $V_{CC} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------------------------------------|---|------------|------------|------------|------------|------------|------------|------------|------------|------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f _{max} | Maximum Toggle Frequency | 3.4 | 4.2 | | 3.8 | 4.2 | | 3.8 | 4.2 | | GHz |
| t _{PLH} t _{PHL} | Propagation Delay CLK to Q Reset to Q | 560 400 | 670 540 | 860 700 | 610 460 | 700 550 | 810 660 | 640 570 | 740 480 | 840 670 | ps |
| t _{RR} | Set/Reset Recovery | 400 | 200 | | 400 | 200 | | 400 | 200 | | ps |
| V _{PP} | Input Swing (Note 2) | 150 | | 1000 | 150 | | 1000 | 150 | | 1000 | mV |
| t _{JITTER} | Cycle-to-Cycle Jitter | | 1.0 | | | 1.0 | | | 1.0 | | ps |
| t _r t _f | Output Rise/Fall Times Q (20%–80%) | 100 | 225 | 350 | 100 | 225 | 350 | 100 | 225 | 350 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

- 10 Series: V_{EE} can vary +0.25 V / -0.5 V.
100 Series: V_{EE} can vary +0.8 V / -0.5 V.
- $V_{PP}(\text{min})$ is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈ 40 .

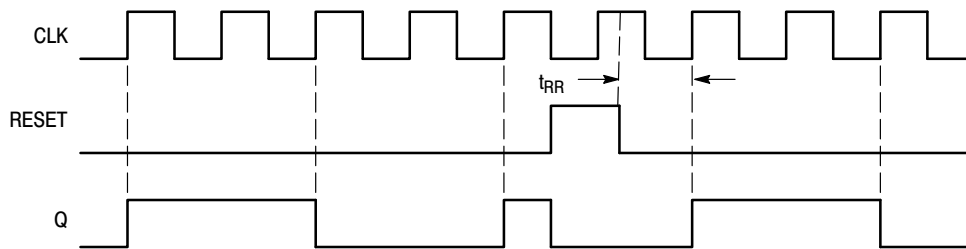


Figure 2. Timing Diagram

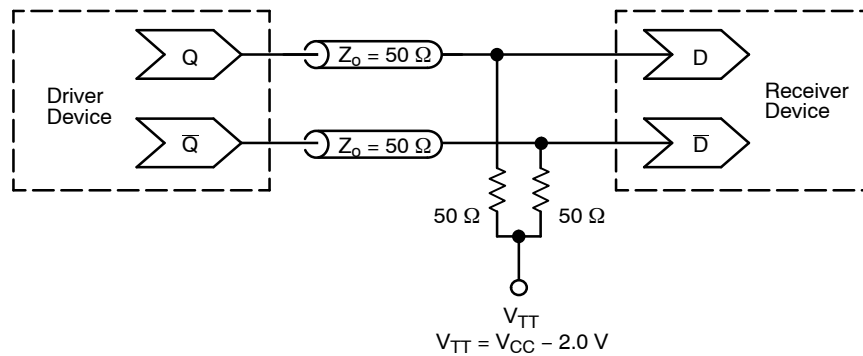


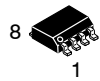
Figure 3. Typical Termination for Output Driver and Device Evaluation
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices)

MC10EL33, MC100EL33

Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

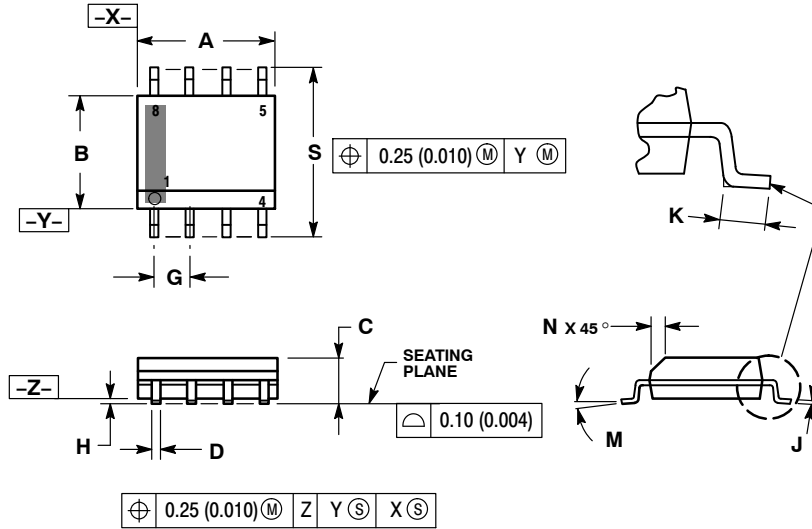
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

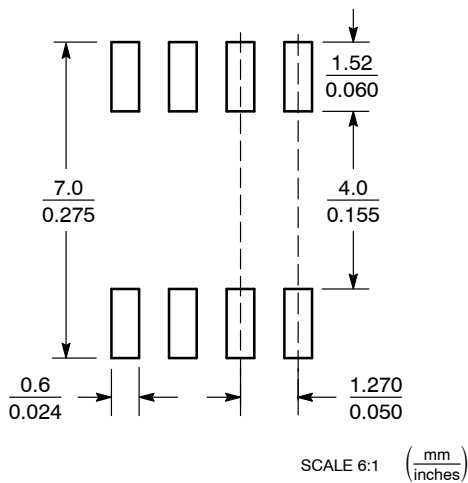
DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

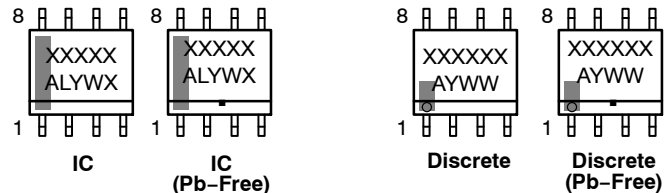
| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
■ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

| | | |
|------------------|-------------|--|
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| DESCRIPTION: | SOIC-8 NB | PAGE 1 OF 2 |

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CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER</p> | <p>STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1</p> | <p>STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1</p> | <p>STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE</p> |
| <p>STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE</p> | <p>STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE</p> | <p>STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd</p> | <p>STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1</p> |
| <p>STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON</p> | <p>STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND</p> | <p>STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1</p> | <p>STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> | <p>STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN</p> | <p>STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON</p> | <p>STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC</p> | <p>STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE</p> | <p>STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1</p> | <p>STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6</p> | <p>STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND</p> | <p>STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT</p> | <p>STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT</p> | <p>STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC</p> | <p>STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN</p> | <p>STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN</p> |
| <p>STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1</p> | <p>STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1</p> | | |

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