Low Skew 1:6 Clock Driver

Product Features:

- Six low skew outputs: 0.35 ns (typ.)
- XTAL oscillator interface: 35 MHz (max.)
- Clock input interface: 66 MHz (max.)
- 3.3V supply voltage
- High speed: 3.5 ns propagation delay
- 5.0V tolerant enable inputs
- Packages available:
  - 16-pin 150-mil wide SOIC (W16)

Product Description:

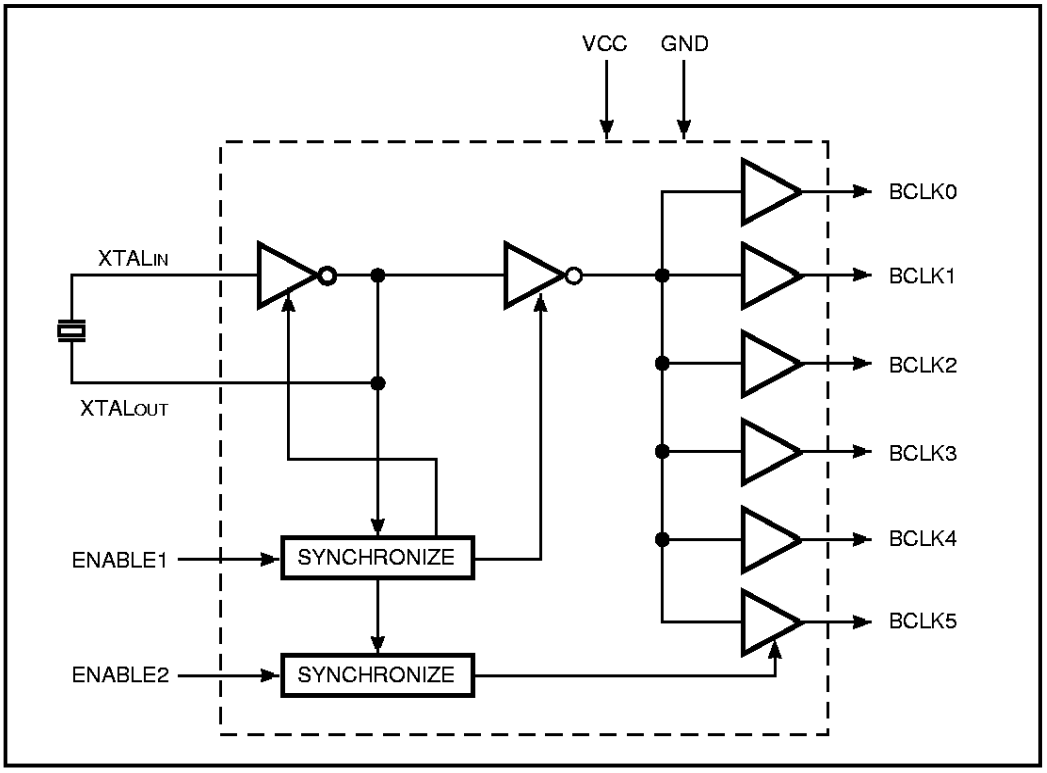
The PI6B3904 is a low skew 1:6 clock driver. It is designed to provide the requisite clocks for a PCI buses in either a 5V or 3.3V PCI signaling environment.

The PI6B3904 operates from a 3.3V supply and can interface to either a TTL clock input or an external crystal. The inputs can be driven with 5.0V when the Vcc is at 3.3V. The outputs meet all of the PCI standards specifications.

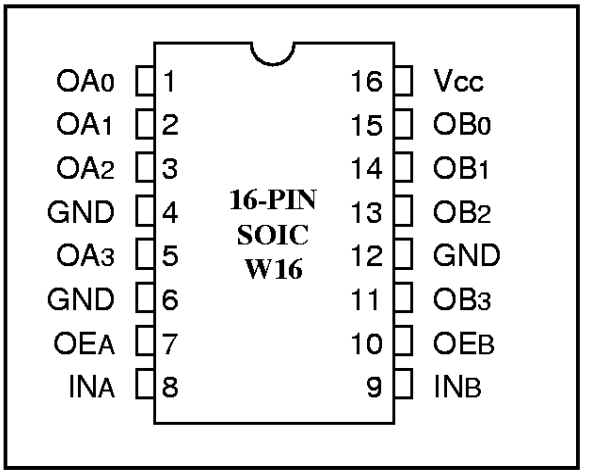
The PI6B3904 offers two synchronous enable inputs. Both enable signals are active HIGH. A logic "0" on the ENABLE1 input will disable the BCLK[4-0] outputs. A logic "0" on the ENABLE2 input will disable the BCLK5 output.

The enable signals can be used to disable the device for system power savings during periods of inactivity. Output disabling will happen only when the BCLK[4-0] outputs are already LOW. This feature guarantees that there will be no runt pulses during the enable and disable process.

Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
XTALIN	XTAL Input
XTALOUT	XTAL Output. 180° phase shift from XTAL pins.
ENABLE1 ENABLE2	Enable pins control BLCK5-BLCK0 outputs
BLCK5-0	Clock outputs. Same as input frequency
Vcc	Power supply
GND	Ground

Function Description

ENABLE1[1]	ENABLE2[1]	BLCK4-0 Output	BLCK5 Output	OSC (On/Off)
0	0	LOW	LOW	Off
0	1	LOW	XTALIN	On
1	0	XTALIN	LOW	On
1	1	XTALIN	XTALIN	On

Notes:
1. ENABLE1, ENABLE2 skew during logic switching from 10 to 01 should not cause the OSC to shut off.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Input Voltage	–0.5V to Vcc +0.5V
Supply Voltage	–0.5V to +4.6V
DC Output Current	120 mA
Power Dissipation (ENABLE1/2 = 1)	TBD mW
Power Dissipation (ENABLE1/2 = 0)	40 µW

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = 0°C to +70°C, V_{CC} = 3.3V ±0.3V)

Parameters	Description	Test Conditions[1]		Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –36.0 mA[2]	2.4	—	—	V
V_{OL}	Output LOW Current	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 36 mA	—	—	0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level[3]		2.0	—	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.		—	—	2.5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.		—	—	2.5	µA

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	$XTAL_{IN}$	—	9.0	pF
		Others	—	4.5	pF

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. The outputs can drive series terminated or parallel 50Ω (or 50Ω to Vcc/2) transmission lines on the incident edge.
3. $XTAL_{IN}$ input will sink up to 10 mA when driven to 5.5V. There are no reliability concerns associated with the condition. Note that the Enable1 input must be a logic HIGH. Do not take the Enable1 input to a logic LOW with >Vcc volts on the $XTAL_{IN}$ input.

Recommended Operating Conditions

Parameters	Description	Min.	Max.	Units
T_A	Ambient Temperature	0	70	°C
Vcc	Positive Supply Voltage (Functional Range)	3.0	3.6	V
SYNC	Input Frequency in $XTAL_{IN}$ (SYNC V_{IH} = 2.0V, V_{IL} = 0.8V	DC	66	MHz
t_R, t_F	Input Rise or Fall Time	3	—	ns
SYNC	t_{HIGH} (@ SYNC Input) when using external source for reference	0.44T	0.56T	(T is the time period)
SYNC	t_{LOW} (@ SYNC Input) when using external source for reference	0.44T	0.56T	(T is the time period)

Power Supply Characteristics

Parameters	Description	Test Conditions[1]	Min.	Typ.	Max.	Units
I_{CC}	Quiescent Power[2]	DC	—	20	—	µA
	Supply Current[3]	33 MHz	—	50	60	mA

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. PI6B3904 with no loading using a 33 MHz crystal. Enable1 = Enable2 = 0. Power supply current increases with output frequency and output load conditions.
3. PI6B3904 with no loading using a 33 MHz crystal. Enable1 = Enable2 = 1. Power supply current increases with output frequency and output load conditions.

Dynamic Operating Conditions (T_A = 0°C to +70°C, Vcc = 3.3V ± 0.3V)

Parameters	Description	Min.	Max.	Units
f	Frequency Range	DC	66	MHz
t_H	High Time (Time above 2.0V at the load end of transmission line)	0.4T	0.6T	T is the time period
t_L	Low Time (Time below 0.8V at the load end of transmission line)	0.4T	0.6T	T is the time period
Period (min.)	Time from 1.5V to next 1.5V at the end of transmission line	T – 400 ps		T is the average period
SK_R	Skew Rise Time	—	400	ps
SK_F	Skew Fall Time	—	500	ps
t_R	Rise Time: 0.4V to 2.4V (Unloaded Output)	1	4	V/ns
t_F	Fall Time: 2.4V to 0.4V (Unloaded Output)	1	4	V/ns
t_{ON}	Start-up Time. Time to start the oscillator on and Enable only CLK Output.	—	5	ms
t_{OFF}	Disable Time. Time to disable any CLK output and shut off the oscillator.	—	4	Cycles
t_{EN}	Enable CLK_{ON} Time. Time to enable any CLK output. (Oscillator is already ON)	—	4	Cycles
t_{DIS}	Disable CLK_{OFF} Time. Time to disable any CLK output. (Oscillator stays ON)	—	4	Cycles
C_{LOAD}	1 or 2 Series Terminated Lines Transmission Line Z_{OUT} Termination Matched Series Resistor Capacitance at Load Device	 60 Z_{OUT} 5	 100 Z_{OUT} 12	 Ω Ω pF
D_{RT}	Round Trip Delay Clock Lines. The lesser of or	— —	12 T/2 – 1	ns ns
O_{GAIN}	Oscillator Cell Gain. $XTAL_{IN}$ to $XTAL_{OUT}$ (Must oscillate with a XTAL of 70Ω (max) Series Resistance	6	—	dB
S_{LP}	Loop Phase Shift. Modulo 360° + (Oscillator Cell: Inverter and XTAL Network)	30	—	°C
R_F	XTAL Feedback Resistor, $XTAL_{IN}$ to $XTAL_{OUT}$	200K	1M	Ω
Rs	XTAL Source Impedance of $XTAL_{OUT}$	75	125	Ω
Ds	Driver Source Impedance of Clock Outputs	4	10	Ω

Notes:

1. Each Skew spec forms a window of specified time in which all output transitions must occur. Skew measurements should assume loading as described in notes 2 and 3.
2. **Cycle to Cycle Jitter.** The jitter is not defined separately from the High/Low time or the Period. The duty cycle and the Jitter must be such that the HIGH Time, LOW Time, and Minimum Period are met. In determining the effect of the jitter, it is requested that the 'peak' value be that level which occurs once in 10^{EXP15} events. If the Jitter were Gaussian, this would correspond to 8 sigma.
3. **Alignment Jitter:** Any dynamic Jitter terms that effect output to output skew shall be accounted for in the Skew spec. As with cycle to cycle Jitter, the level of Jitter that should be accounted for is one occurrence in 10^{EXP15} events.