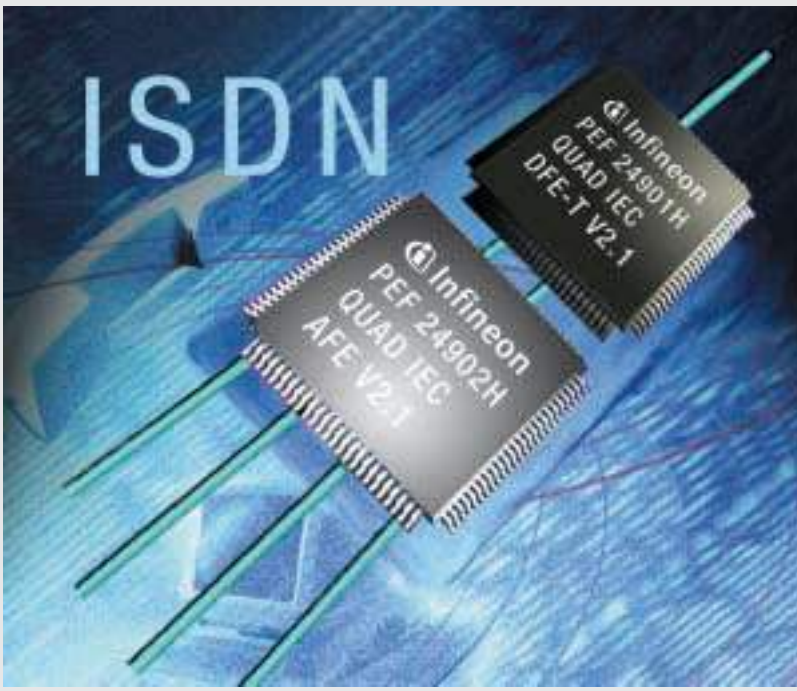
IEC4-T

PEF 24901 V2.1 (DFE-T)
PEF 24902 V2.1 (AFE)

ISDN Echocancellation Circuit 4-Channel for 4B3T Line Code

The widely used ISDN 4-channel chipset IEC4-T consisting of the analog frontend PEB/F 24902 (AFE) and the digital frontend PEB/F 24901 (DFE-T) has been optimized by a redesign of the digital part. The improvements of the DFE-T are a reduced supply-voltage due to its advanced low power 3.3V-CMOS-technology, the doubling of the IOM®-2 data-rate up to 4 Mbit/s and new features in terms of testability and analysis. The IEC4-T chipset fulfills all relevant FTZ, ETSI and ITU standards. Because of its multichannel-architecture it is extremely suitable for highly integrated ISDN linecards.



Applications

- Central office digital linecard
- Access network linecards
- PBX linecards

Features

- Two chip solution featuring full duplex data transmission and reception over two-wire metallic subscriber loops providing 4x ISDN basic rate access
- Fully compliant to:
  - FTZ Guideline 1TR220
  - ETSI TS 102 080 (1998)
  - Recommendation ITU-T I.430
- 4B3T block code at 120 kHz symbol rate
- Loop length without repeater:
  - up to 4.2 km on 0.4 mm wire
  - up to 8.0 km on 0.6 mm wire
- LT mode
- Low power consumption
- IOM®-2 interface for stand alone mode
- 1 kbit/s maintenance channel for transmission of data loopback commands and detected transmission errors
- Masterclock generated by PLL
- Activation and deactivation
- Adaptive echo cancellation and equalization
- Automatic gain control and polarity adaption
- 4 relay driver pins per channel to switch relays or power controller
- 2 status pins per channel
- Extended temperature range (40°C to +85°C)
- JTAG Boundary Scan
- P-MQFP-64 package
- Part of the Infineon System Solution

Add-On Features of the DFE-T PEF 24901 V2.1 compared to V1.x

- Max. IOM®-2 data rate 4 Mbit/s (DCL = 8 MHz)
- +3.3 V instead of +5 V power supply
- Dedicated pins for SSP and DT test modes
- DOUT configurable either as open drain or push-pull (tristate) output
- New MON-12 class features internal register access
- Additional digital local loops
- Bit Error Rate Measurement per port
- Optimized LT-state machine
- Backward compatibility to V1.x:
  - no software changes required
  - pinning-compatible

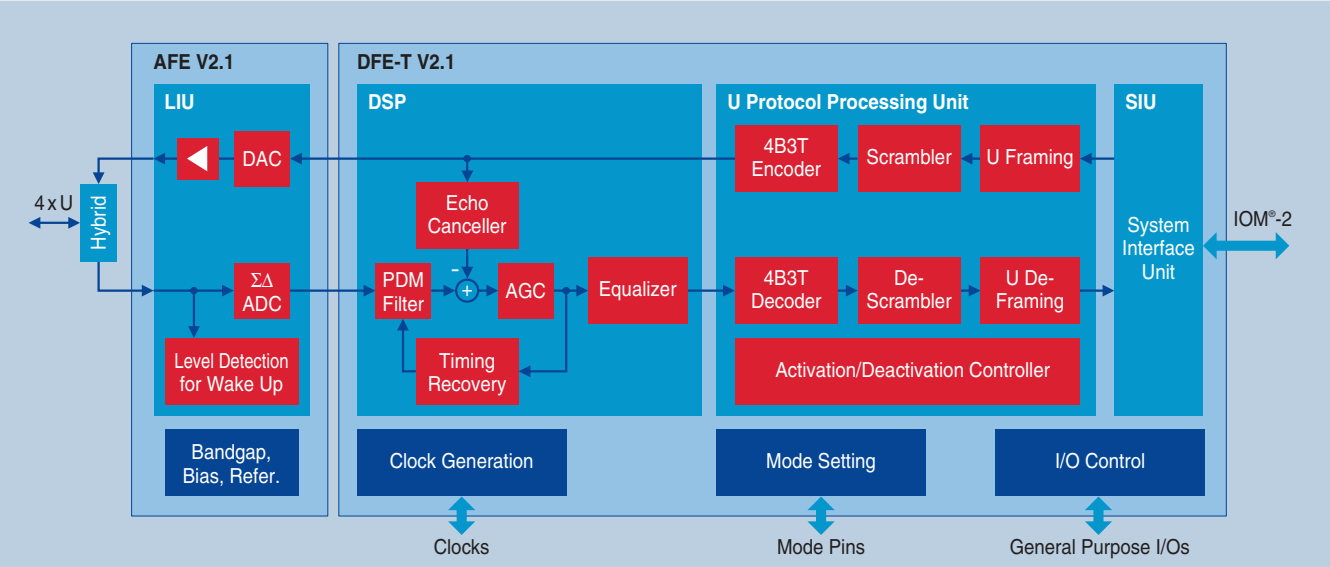
I S D N

4-Channel Chipset

Infineon technologies

Never stop thinking.

Block Diagram

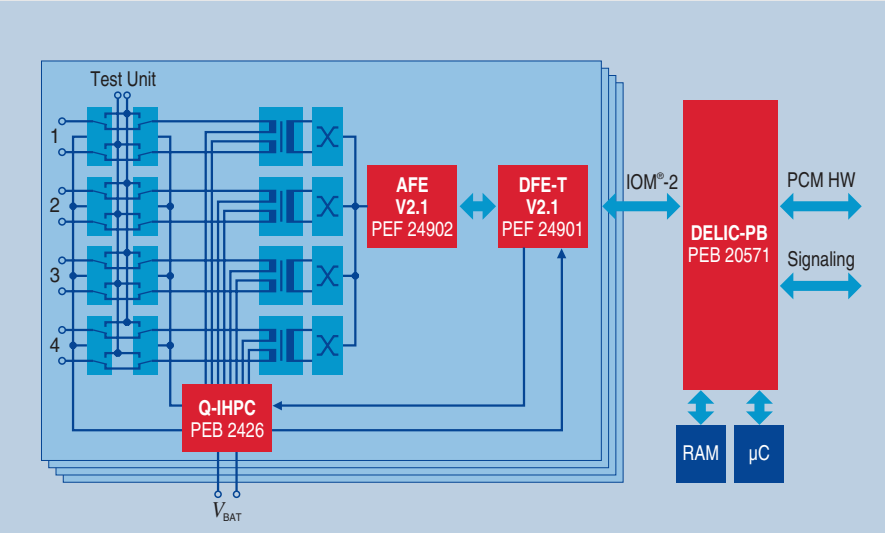


Type	Package	Availability
PEF 24901 H V2.1	P-MQFP-64	Development
PEB/F 24902 H V2.1	P-MQFP-64	Available

Tools and Documentation

Name	Status
Preliminary Data Sheet PEF 24901 V2.1	06.99
Delta Sheet PEF 24901 V2.1	03.99
Product Overview	04.99
Smart 24901 V2.0	Development

Application Examples
ISDN Linecard



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