



ON Semiconductor

High Brightness LED SEPIC Driver

Device	Application	Input Voltage	Output Power	Topology	I/O Isolation
NCP3065 NCV3065	Solid State, Automotive and Marine Lighting	8-25 V	<15 W	SEPIC	NONE

Other Specifications				
	Output 1	Output 2	Output 3	Output 4
Output Voltage	7.2-23 V	N/A	N/A	N/A
Current Ripple	<15%	N/A	N/A	N/A
Nominal Current	0.35, 0.7 A	N/A	N/A	N/A
Max Current	1 A	N/A	N/A	N/A
Min Current	N/A	N/A	N/A	N/A

Minimum Efficiency	70%
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Circuit Description

This circuit is intended for driving high power LEDs, such as the Cree XLAMP™ series, Lumileds Luxeon™ Rebel and K2 and OSRAM, Golden and Platinum Dragon™ as well as the OSTAR™. It is designed for such wide input nominal 12 Vdc applications as automotive and low voltage lighting (12 Vdc/12 Vac). An optional dimming PWM input is included. The circuit is based on NCP3065 operation at 250 kHz in a non-isolated configuration. The primary advantages of this circuit are in the wide input voltage range, wide output voltage range, and in its high efficiency.

A pulse feedback resistor (R8) is used to vary the slope of the oscillator ramp, achieving duty cycle control and steady switching frequency over a wide input voltage range.

Key Features

- Buck-Boost operation
- Wide input and output operation voltage
- Regulated output current
- Dimming
- High frequency operation
- Minimal input and output current ripple
- Open LED protection
- Output short circuit protection

Schematic

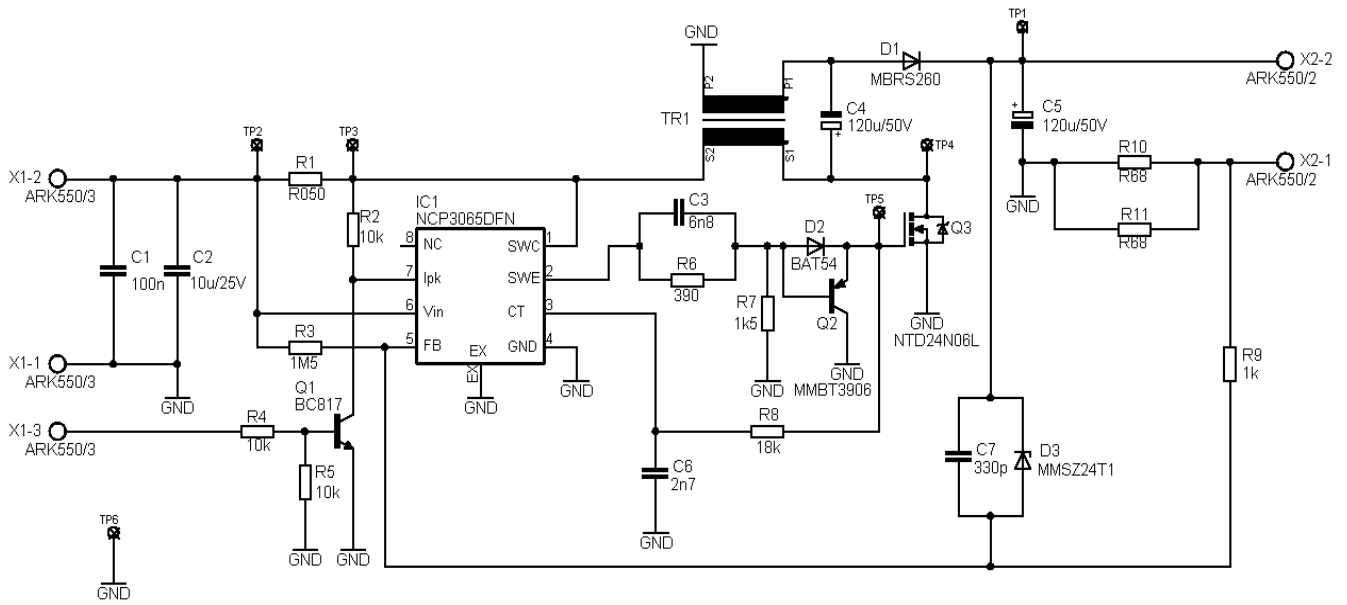


Figure 1 – SEPIC converter schematic

Design Notes

A SEPIC (single-ended primary inductance converter) is distinguished by the fact that its input voltage range can overlap the output voltage range. The basic schematic is shown in Figure 2.

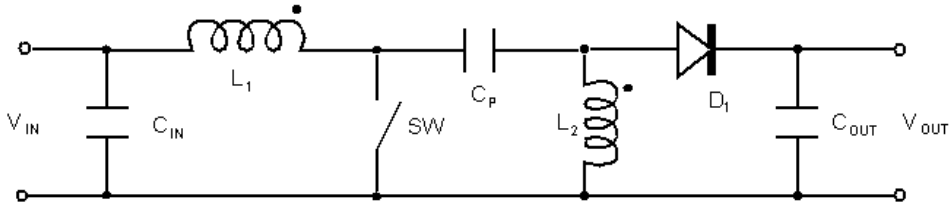


Figure 2 – Generalized SEPIC schematic

When switch SW is ON, energy from the input is stored in inductor L1. Capacitor C_P is connected in parallel to L₂, and energy from C_P is transferred to L₂. The voltage across L₂ is the same as the C_P voltage, which is the same as the input voltage. At this time, the diode is reverse biased and C_{OUT} supplies output current.

If the switch SW is OFF, current in L₁ flows through C_P and D₁ then continues to the load and C_{OUT}. This current recharges C_P for the next cycle. Current from L₂ also flows through D₁ to the load and C_{OUT} that is recharging for the next cycle.

Inductors L₁ and L₂ could be uncoupled, but then they must be twice as large as if they are coupled. Another advantage is that if coupled inductors are used there is very small input current ripple.

Values of coupled inductors are set by these equations:

$$D = \frac{V_{OUT \text{ min}}}{V_{OUT \text{ min}} + V_{IN \text{ min}}} = \frac{7.2}{7.2 + 8} = 0.47$$

$$\Delta I = r \cdot I_{OUT} \frac{D}{1 - D} = 0.8 \cdot 0.7 \cdot \frac{0.47}{1 - 0.47} = 0.51A$$

$$L_{1,2} = \frac{V_{IN \text{ min}} \cdot D}{2 \cdot f \cdot \Delta I} = \frac{8 \cdot 0.47}{2 \cdot 250 \cdot 10^3 \cdot 0.51} = 15.0 \mu H$$

where r is the maximum inductor current ripple factor.

DN06031/D

For a 0.35 A output current variant of this circuit, the values of inductors are

$$\Delta I = r \cdot I_{OUT} \frac{D}{1-D} = 0.95 \cdot 0.35 \cdot \frac{0.47}{1-0.47} = 0.3A$$

$$L_{1,2} = \frac{V_{IN \min} \cdot D}{2 \cdot f \cdot \Delta I} = \frac{8 \cdot 0.47}{2 \cdot 250 \cdot 10^3 \cdot 0.3} = 25.1 \mu H$$

The nearest coupled inductor value for the 0.7 A variant is 15 μH . A variant with 0.35 A output current needs to use inductors with value 22 μH .

The output current is set by R10 (R11). So this resistor can be calculated by the formula:

$$R10 = \frac{0.235}{I_{OUT}} = 350 m\Omega .$$

To protect the circuit against high output voltage under light loads or a fault condition, the output voltage is clamped by a Zener diode (D3) to approximately 24.5 V. Capacitor C7 is used to stabilize feedback, but it impacts line regulation. R3 fixes the line regulation error caused by C7.

External power MOSFET is driven by internal NPN Darlington transistor, external diode D2 and PNP transistor Q2. Compensated divider C3, R6 and R7 is used to reduce gate-source voltage, mainly for high input voltage and to keep sharp edges. Maximum gate-source voltage can be calculated by this formula:

$$V_{GS \max} = (V_{IN} - V_{CE} - V_{D2}) \cdot \frac{R7}{R6 + R7} = (27 - 1.4 - 0.4) \cdot \frac{1500}{390 + 1500} = 18.4V$$

Maximum MOSFET current can be calculated in this way:

$$I_{Q4 \max} = \left(1 + \frac{r}{2}\right) \cdot I_{OUT} \frac{V_{OUT \max}}{V_{IN \min}} = \left(1 + \frac{0.8}{2}\right) \cdot 0.7 \cdot \frac{23}{8} = 2.5A$$

To minimize power MOSFET conductance losses, it is recommended to select a transistor with small $R_{DS(ON)}$. To minimize switching losses, it is recommended to select a transistor with small gate charge. Power MOSFET must also have a breakdown voltage higher than:

$$V_{FETPK} = V_{IN} + V_{OUT} = 18 + 23 = 41V$$

Cycle by cycle switch current protection is set by R1 at

$$I_{PKset} = \frac{0.2}{R1}$$

A suitable value is higher than maximum switch current.

$$R1 < \frac{0.2}{I_{Q1 \max}} = \frac{0.2}{2.5} = 80 m\Omega$$

Diode D1 maximum voltage is determined by this equation:

DN06031/D

$$V_{D1\max} = V_{IN} + V_{OUT} = 18 + 23 = 41V$$

and with current

$$I_{D1} = I_{OUT} = 0.7A$$

The C4 coupling capacitor is selected based on input voltage and on current

$$D_{\max} = \frac{V_{OUT\max}}{V_{OUT\max} + V_{IN\min}} = \frac{23}{23 + 8} = 0.74$$

$$I_{C4RMS} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN}} \sqrt{\frac{1 - D_{\max}}{D_{\max}}} = \frac{23 \cdot 0.7}{8} \sqrt{\frac{1 - 0.74}{0.74}} = 1.2A$$

and its minimal value is

$$C4 > \frac{I_{OUT} \cdot D_{\min}}{0.05 \cdot V_{IN\min} \cdot f} = \frac{0.7 \cdot 0.47}{0.05 \cdot 8 \cdot 250 \cdot 10^3} = 2\mu F$$

The output capacitor's current is

$$I_{C5} = I_{OUT} \cdot \sqrt{\frac{D_{\max}}{1 - D_{\max}}} = 0.7 \sqrt{\frac{0.74}{1 - 0.74}} = 1.2A$$

$$C5 > \frac{\frac{V_{OUT\min}}{V_{IN\min}} \cdot I_{OUT} \cdot D_{\min}}{f \cdot r \cdot V_{OUT\min}} = \frac{\frac{7.3}{8} \cdot 0.7 \cdot 0.47}{250 \cdot 10^3 \cdot 0.1 \cdot 7.3} = 1.7\mu F$$

The value could be much larger for higher stability, but a higher value impacts the dimming function at low duty cycle.

The resistor R8 is used to stabilize feedback loop. Used value is compromise for whole input and output voltage range. If this circuit is used for specified load only, it should be tuned by this resistor to better efficiency and line regulation.

X1-3 input is used for dimming. The dimming signal level is 2-10 V. The recommended dimming frequency is about 200 Hz. For frequencies below 100 Hz the human eye will see the flicker. The dimming function utilizes the NCP3065's peak current protection input. The second way to achieve this is to use the FB pin. See figure 10.

Conclusion

This circuit is ideal in applications with strings of two to six LED chips powered from a power supply with wide input range (8-20V). The advantages of this circuit include its small size, low price, wide input and output voltage ranges, and very small input current ripple.

PC Board

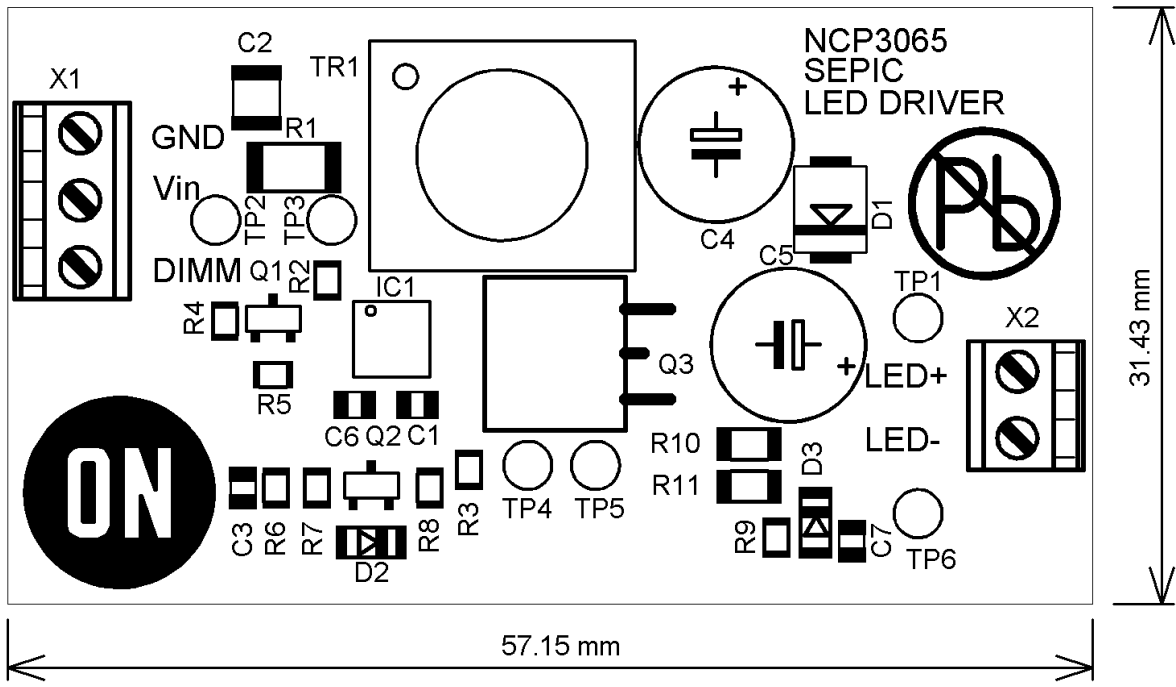


Figure 3 – components position on PCB

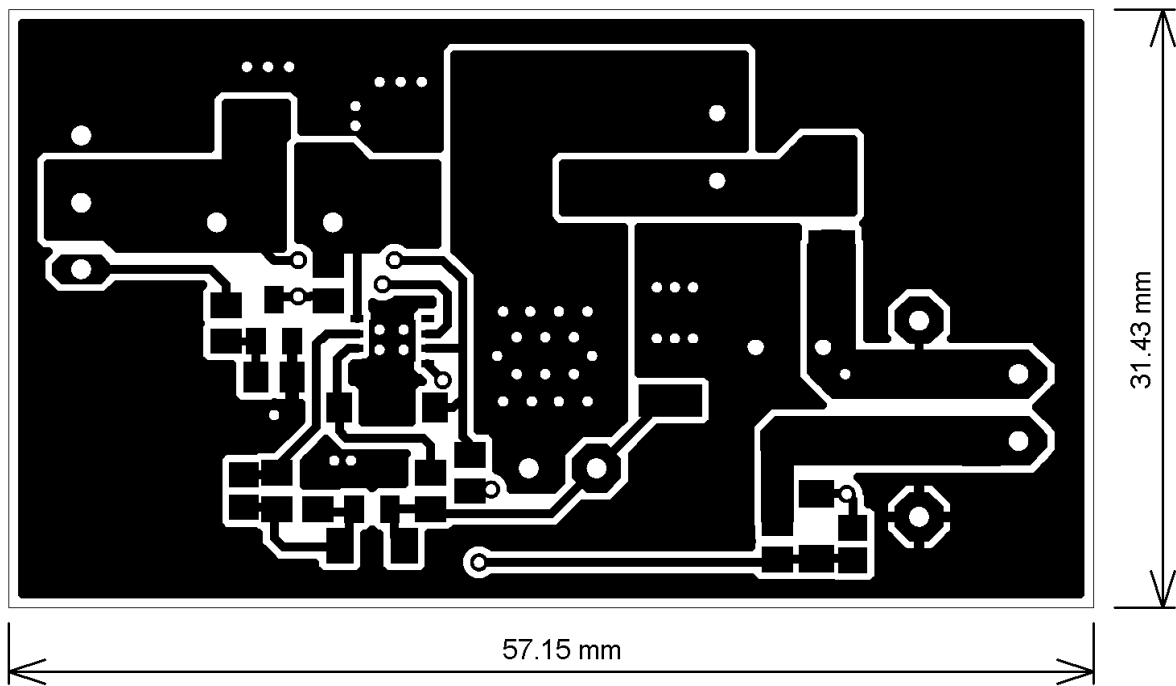


Figure 4 – PCB's top side

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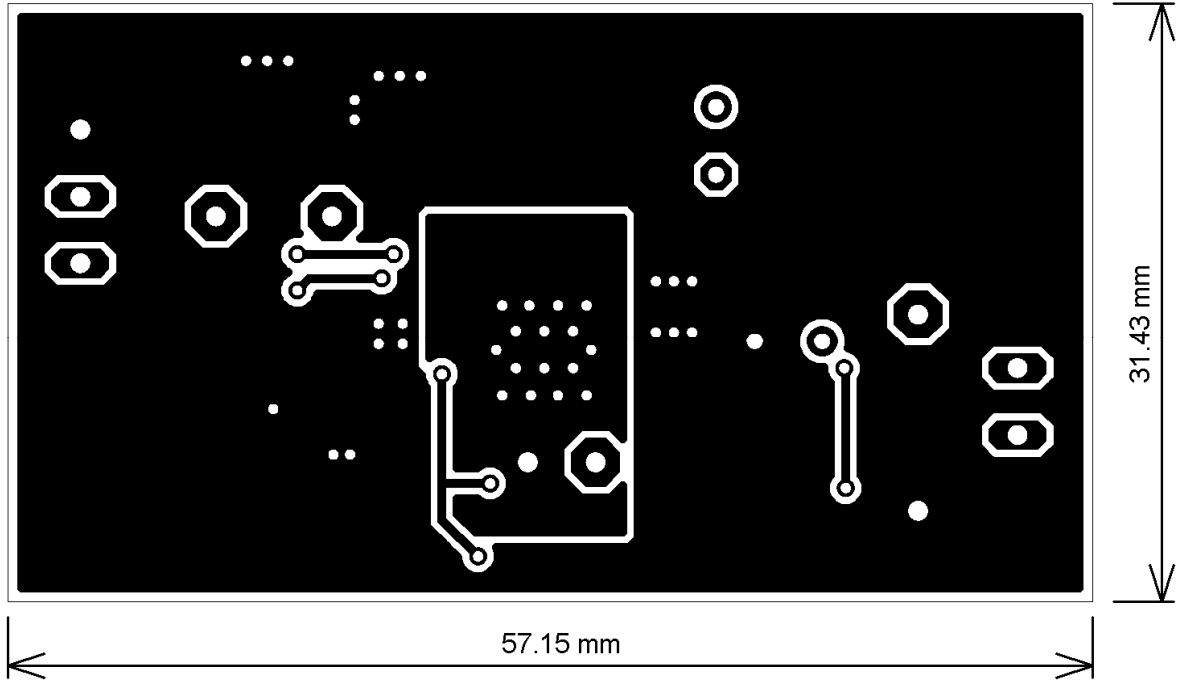


Figure 5 – PCB's bottom side

Bill of Materials for the NPC3065 SEPIC Demoboard

Designator	Quantity	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Lead Free	Comments
R3	1	Resistor SMD	1M5	1%	0805	Vishay	CRCW08051M50FKEA	Yes	Yes	
R9	1	Resistor SMD	1k	1%	0805	Vishay	CRCW08051K00FKEA	Yes	Yes	
R7	1	Resistor SMD	1k5	1%	0805	Vishay	CRCW08051K50FKEA	Yes	Yes	
C6	1	Ceramic Capacitor SMD	2n7	5%	0805	Murata	GM2165C1H272JA16D	Yes	Yes	
C3	1	Ceramic Capacitor SMD	6n8	10%	0805	Kemet	C0805C688K5RAC	Yes	Yes	
R2, R4, R5	3	Resistor SMD	10k	1%	0805	Vishay	CRCW080510K0FKEA	Yes	Yes	
C2	1	Ceramic Capacitor SMD	10uF/25V	+80%/-20%	1210	Murata	GRM32NF51E106ZA01L	Yes	Yes	
R8	1	Resistor SMD	27k	1%	0805	Vishay	CRCW080527K0FKEA	Yes	Yes	
C1	1	Ceramic Capacitor SMD	100nF	5%	0805	Kemet	C0805C104J5RAC	Yes	Yes	
C4, C5	2	Capacitor	120uF/50V	20%	8x15	Koshin	KZH-50V121MIG4	Yes	Yes	
C7	1	Ceramic Capacitor SMD	330pF	5%	0805	Kemet	C0805C33J5GAC-TU	Yes	Yes	
R6	1	Resistor SMD	390R	1%	0805	Vishay	CRCW0805390RFKEA	Yes	Yes	
X2	1	Inlet Terminal Block	DG350-3.50-02	-	-	Dejson	DG350-3.50-02	Yes	Yes	
X1	1	Outlet Terminal Block	DG350-3.50-03	-	-	Dejson	DG350-3.50-03	Yes	Yes	
D2	1	Schottky Diode 30V	BAT54HTTIG	-	SOD-323	ON Semiconductor	BAT54HTTIG	Yes	Yes	
O1	1	General Purpose Transistor NPN	BC817-40LT1G	-	SOT-23	ON Semiconductor	BC817-40LT1G	No	Yes	
D1	1	Surface Mount Schottky Power Rectifier	MBR5260T3G	-	SMB	ON Semiconductor	MBR5260T3G	No	Yes	
Q2	1	PNP General Purpose Transistor	MMBT3906TTIG	-	SOT-23	ON Semiconductor	MMBT3906TTIG	No	Yes	
D3	1	Zener Diode 500 mW 24 V	MMSZ24TTG	5%	SOT-123	ON Semiconductor	MMSZ24TTG	No	Yes	
IC1	1	Constant Current Switching Regulator	NCV3065MNTXG	-	DFN	ON Semiconductor	NCV3065MNTXG	No	Yes	
Q3	1	Power MOSFET 24 Amps, 60 Volts, Logic Level, N-Channel	NTD24N06LT4G	-	DPAK	ON Semiconductor	NTD24N06LT4G	No	Yes	
R1	1	Resistor SMD	0R050	1%	2010	Weilwyn	LR2010-R05FW	Yes	Yes	
R10, R11	2	Resistor SMD	0F68	5%	1206	Tyco Electronics	RL73K2BR68JTD	Yes	Yes	
TP1, TP2, TP3, TP4, TP5, TP6	6	Test Point	Terminal, PCB Black PK100	-	1.02mm	Verob	20-2137	Yes	Yes	
TR1	1	Transformer for 0.35A version	PF0553.223	-	-	Pulse	PF0553.223	No	Yes	
TR1	1	Transformer for 0.7A version	PF0553.153	-	-	Pulse	PF0553.153	No	Yes	

Measurements

NCP3065 SEPIC Converter - Line regulation, $I_{OUT} = 350 \text{ mA}$

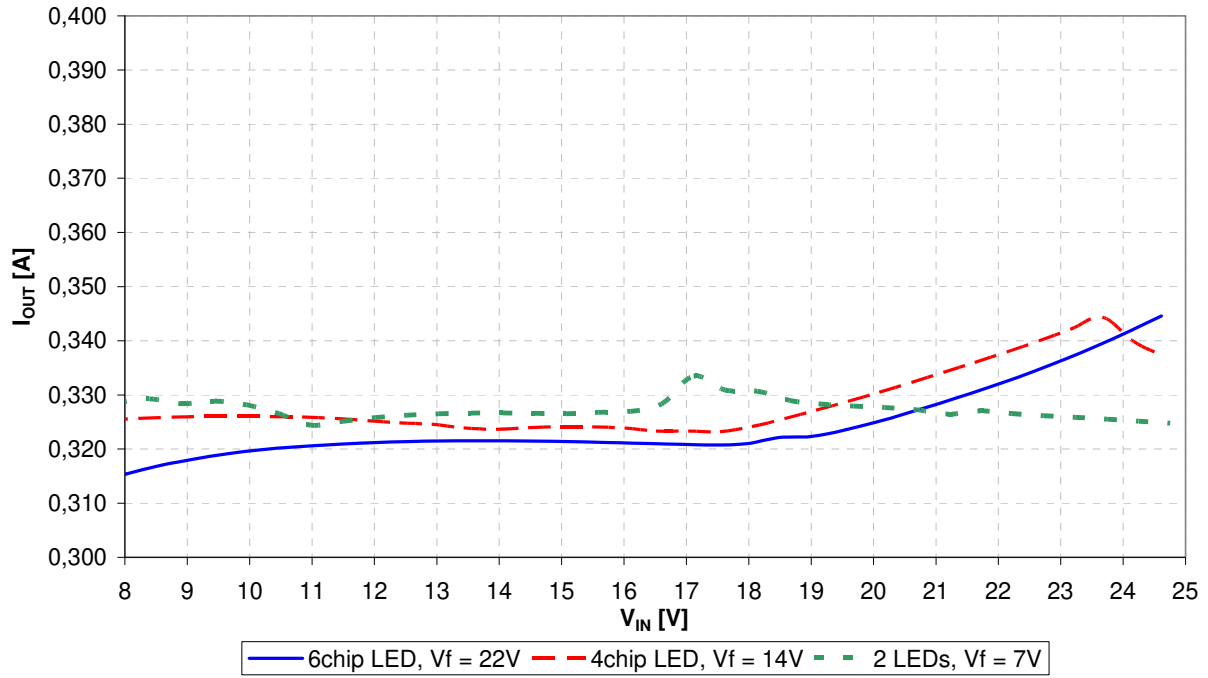


Figure 6 – Line regulation for $I_{OUT} = 350 \text{ mA}$

NCP3065 SEPIC Converter - Efficiency, $I_{OUT} = 350 \text{ mA}$

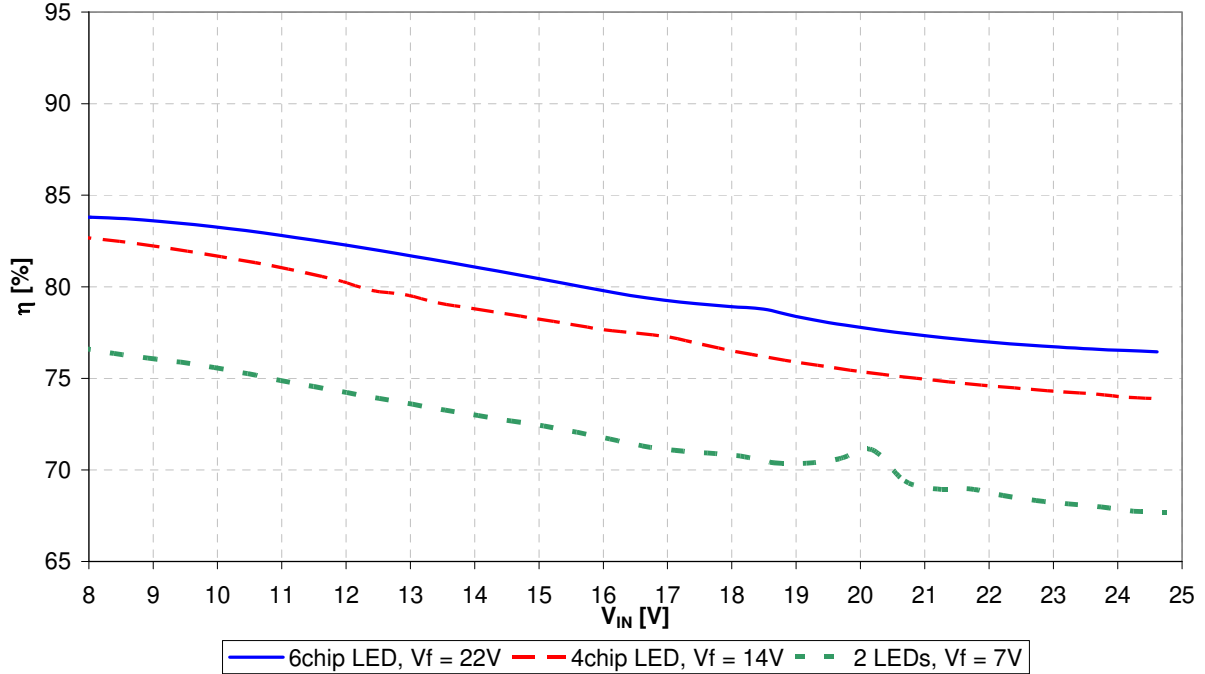


Figure 7 – Efficiency for $I_{OUT} = 350 \text{ mA}$

NCP3065 SEPIC Converter - Line regulation, $I_{OUT} = 700\text{ mA}$

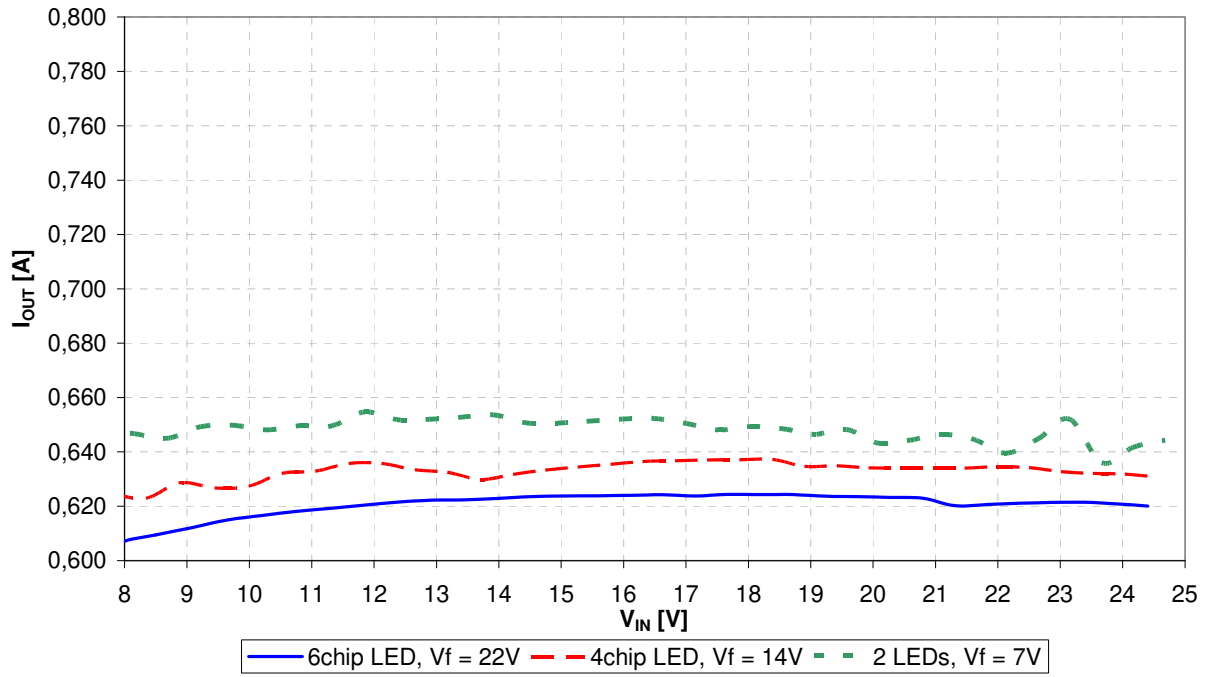


Figure 8 – Line regulation for $I_{OUT} = 700\text{ mA}$

NCP3065 SEPIC Converter - Efficiency, $I_{OUT} = 700\text{ mA}$

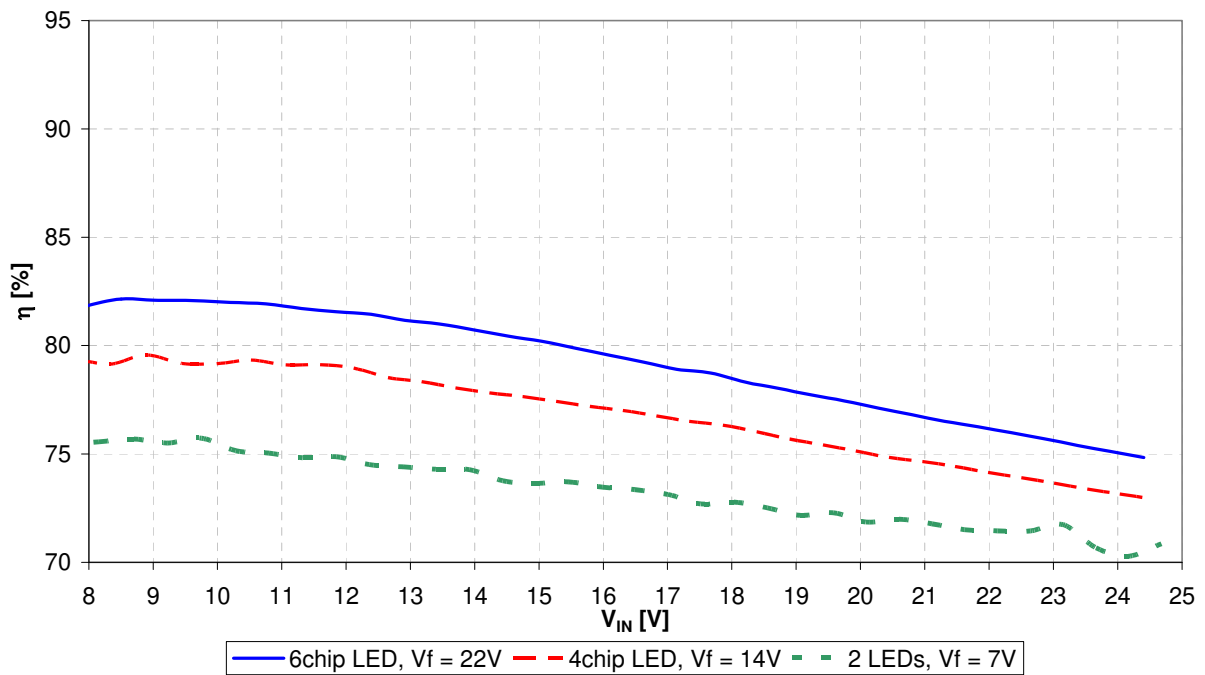


Figure 9 – Efficiency for $I_{OUT} = 700\text{ mA}$

NCP3065 SEPIC Converter - Dimming Linearity

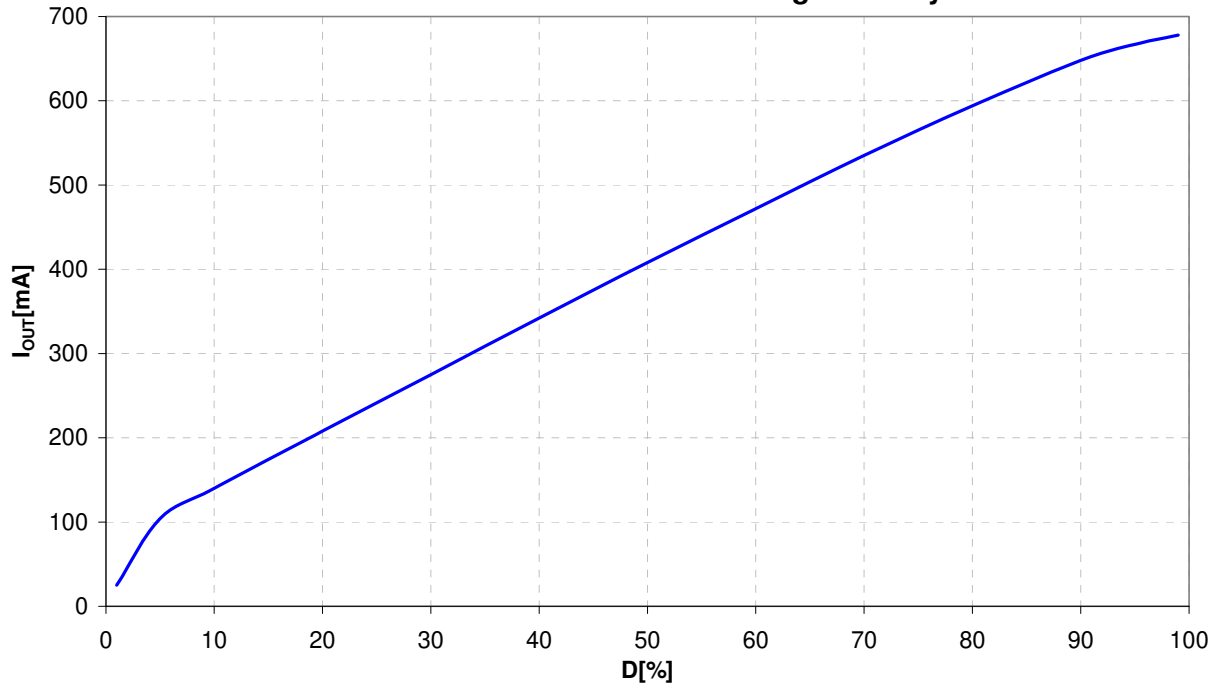


Figure 10 – Dimming linearity, dimming frequency 200Hz

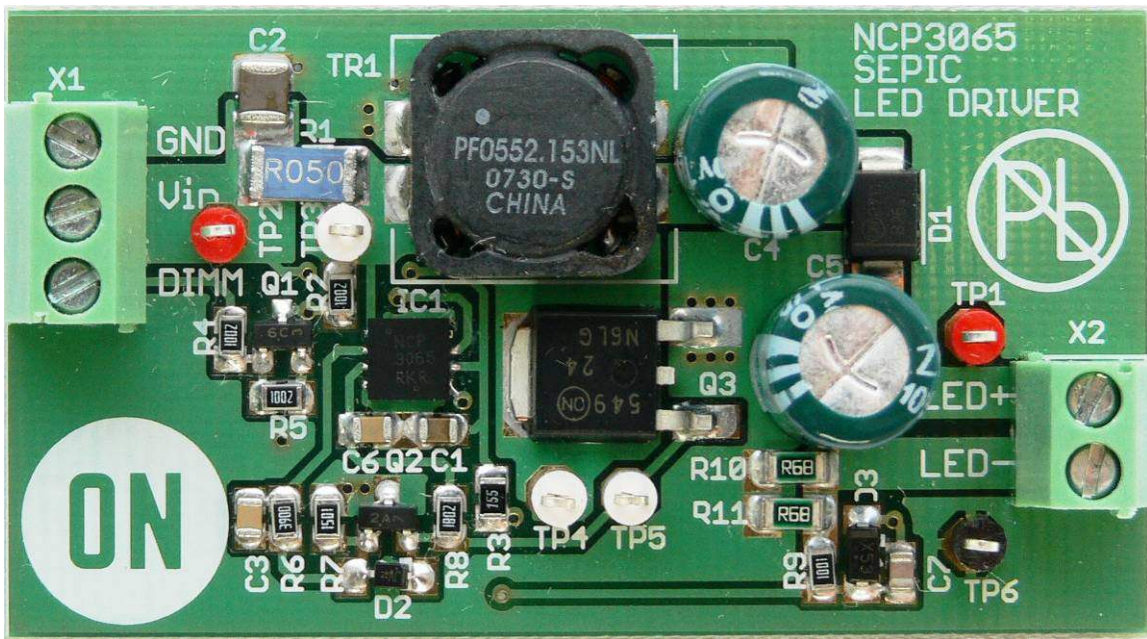


Figure 11 – PCB's top side

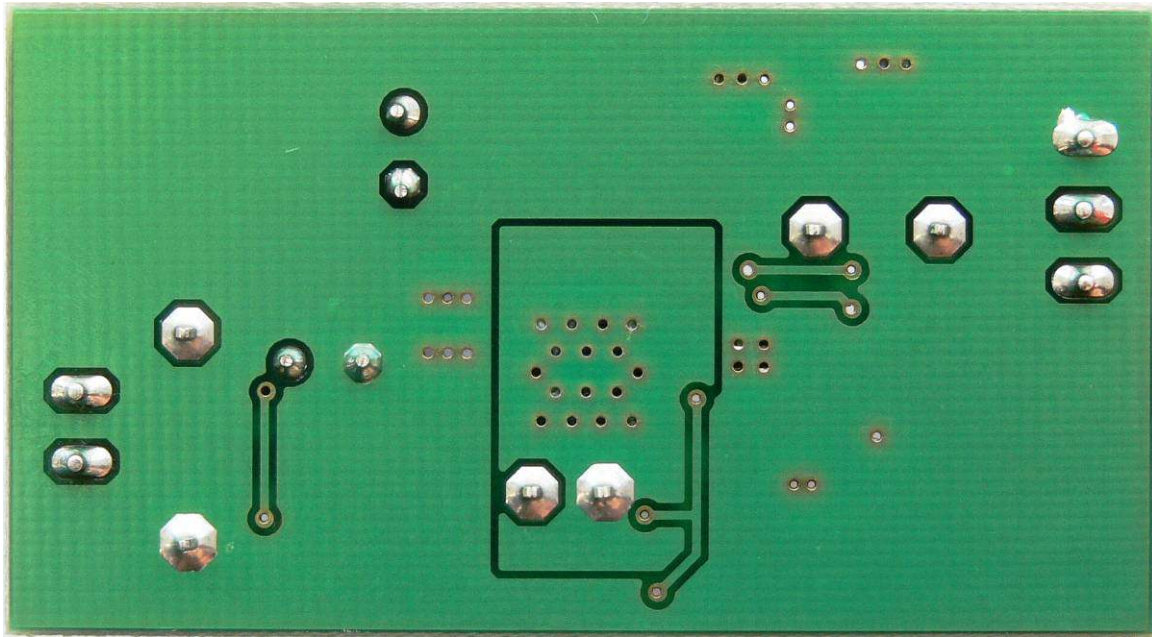


Figure 12 – PCB's bottom side

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Design note created by Petr Konvičný, Tomáš Tichý, e-mail: Petr.Konvicny@onsemi.com, Tomas.Tichy@onsemi.com