

**54S/74S257**  
**54LS/74LS257**

**QUAD 2-INPUT MULTIPLEXER**  
(With 3-State Outputs)

**DESCRIPTION** — The '257 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ( $\overline{OE}$ ) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed.

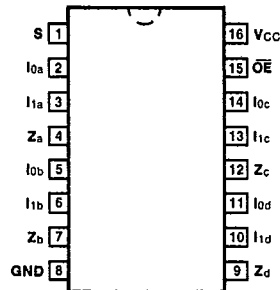
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER
- NON-INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

**ORDERING CODE:** See Section 9

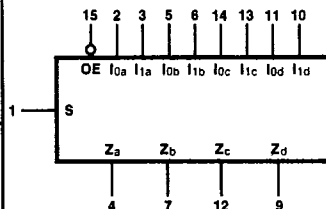
PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0 V \pm 5\%$ , $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = +5.0 V \pm 10\%$ , $T_A = -55^\circ C$ to $+125^\circ C$	
Plastic DIP (P)	A	74S257PC, 74LS257PC		9B
Ceramic DIP (D)	A	74S257DC, 74LS257DC	54S257DM, 54LS257DM	6B
Flatpak (F)	A	74S257FC, 74LS257FC	54S257FM, 54LS257FM	4L

**CONNECTION DIAGRAM**  
PINOUT A

T-66-21-51



**LOGIC SYMBOL**



$V_{CC}$  = Pin 16  
Gnd = Pin 8

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
S	Common Data Select Input	2.5/2.5	1.0/0.5
$\overline{OE}$	3-State Output Enable Input (Active LOW)	1.25/1.25	0.5/0.25
$I_{0a} - I_{0d}$	Data Inputs from Source 0	1.25/1.25	0.5/0.25
$I_{1a} - I_{1d}$	Data Inputs from Source 1	1.25/1.25	0.5/0.25
$Z_a - Z_d$	Multiplexer Outputs	162/12.5 (50)	65/5.0 (25)/(2.5)

**FUNCTIONAL DESCRIPTION** — This device is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the  $I_{0x}$  inputs are selected and when Select is HIGH, the  $I_{1x}$  inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\begin{aligned} Z_a &= \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) & Z_b &= \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S}) \\ Z_c &= \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) & Z_d &= \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S}) \end{aligned}$$

When the Output Enable input ( $\overline{OE}$ ) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

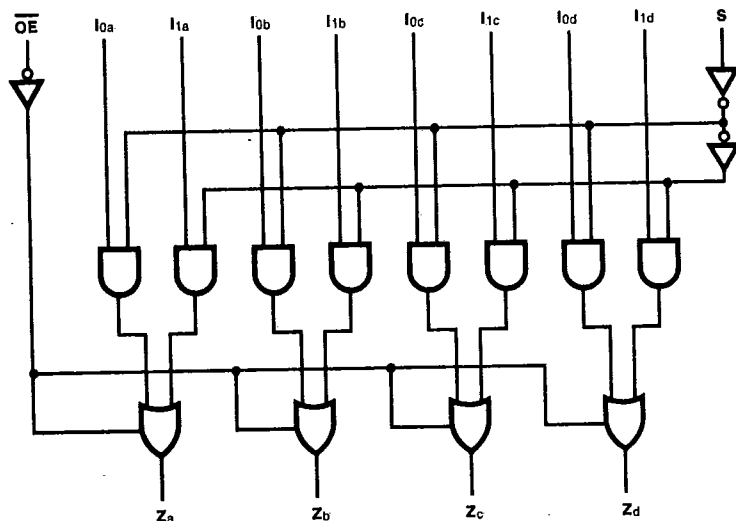
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**TRUTH TABLE**

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	$I_0$	$I_1$	Z
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 (Z) = High Impedance

**LOGIC DIAGRAM**



**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

SYMBOL	PARAMETER		54/74S		54/74LS		UNITS	CONDITIONS
			Min	Max	Min	Max		
I <sub>CC</sub>	Power Supply Current	Outputs HIGH	68		10		mA	V <sub>CC</sub> = Max; S, I <sub>1x</sub> = 4.5 V; OE, I <sub>0x</sub> = Gnd
		Outputs LOW	93		16			V <sub>CC</sub> = Max; I <sub>1x</sub> = 4.5 V; OE, I <sub>0x</sub> , S = Gnd
		Outputs OFF	99		19			V <sub>CC</sub> = Max; S, I <sub>0x</sub> = Gnd OE, I <sub>1x</sub> = 4.5 V

**AC CHARACTERISTICS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER		54/74S		54/74LS		UNITS	CONDITIONS
			C <sub>L</sub> = 15 pF R <sub>L</sub> = 280 Ω		C <sub>L</sub> = 15 pF			
			Min	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to Z <sub>n</sub>		7.5	18	18	18	ns	Figs. 3-1, 3-5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S to Z <sub>n</sub>		15	21	15	21	ns	Figs. 3-1, 3-20
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time		19.5	30	21	30	ns	Figs. 3-3, 3-11, 3-12 R <sub>L</sub> = 2 kΩ ('LS257)
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time		8.5	30	14	25	ns	Figs. 3-3, 3-11, 3-12 R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 5 pF ( 'LS257)