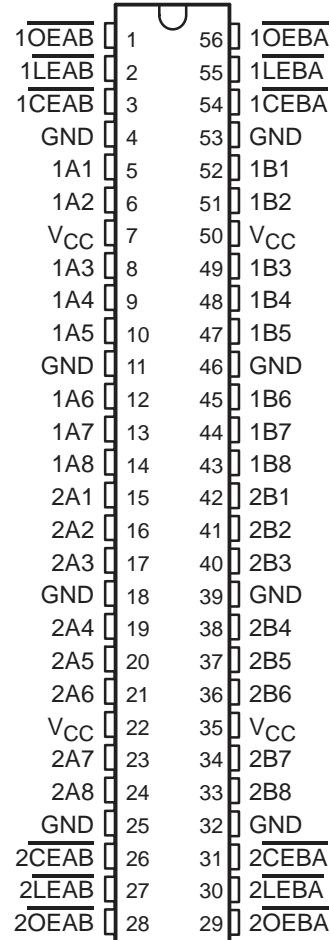


# SN74LVC16543 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS317A – NOVEMBER 1993 – REVISED OCTOBER 1995

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

DGG OR DL PACKAGE  
(TOP VIEW)



## description

This 16-bit registered transceiver is designed for low-voltage (3.3-V)  $V_{CC}$  operation.

The SN74LVC16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ( $\overline{LEAB}$  or  $\overline{LEBA}$ ) and output-enable ( $\overline{OEAB}$  or  $\overline{OEBA}$ ) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ( $\overline{CEAB}$ ) input must be low in order to enter data from A or to output data from B. If  $\overline{CEAB}$  is low and  $\overline{LEAB}$  is low, the A-to-B latches are transparent; a subsequent low-to-high transition of  $\overline{LEAB}$  puts the A latches in the storage mode. With  $\overline{CEAB}$  and  $\overline{OEAB}$  both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{OEBA}$  inputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16543 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



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**FUNCTION TABLE†**  
**(each 8-bit section)**

INPUTS				OUTPUT B
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	$B_0^\ddagger$
L	L	L	L	L
L	L	L	H	H

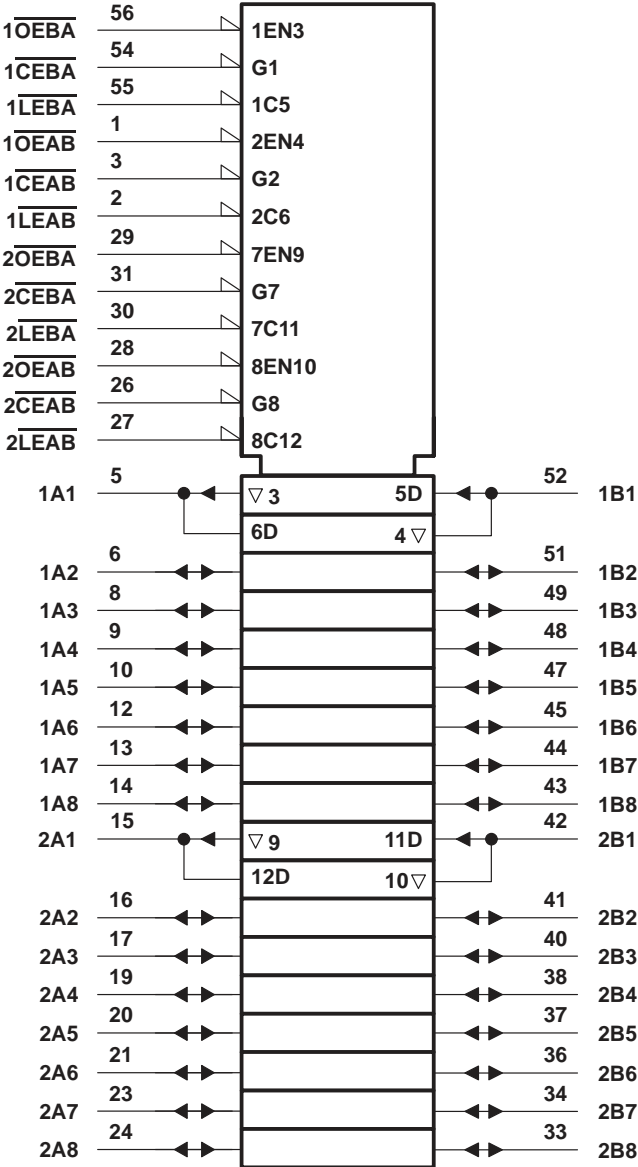
† A-to-B data flow is shown; B-to-A flow control is the same except that it uses  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{OEBA}$ .

‡ Output level before the indicated steady-state input conditions were established

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logic symbol†



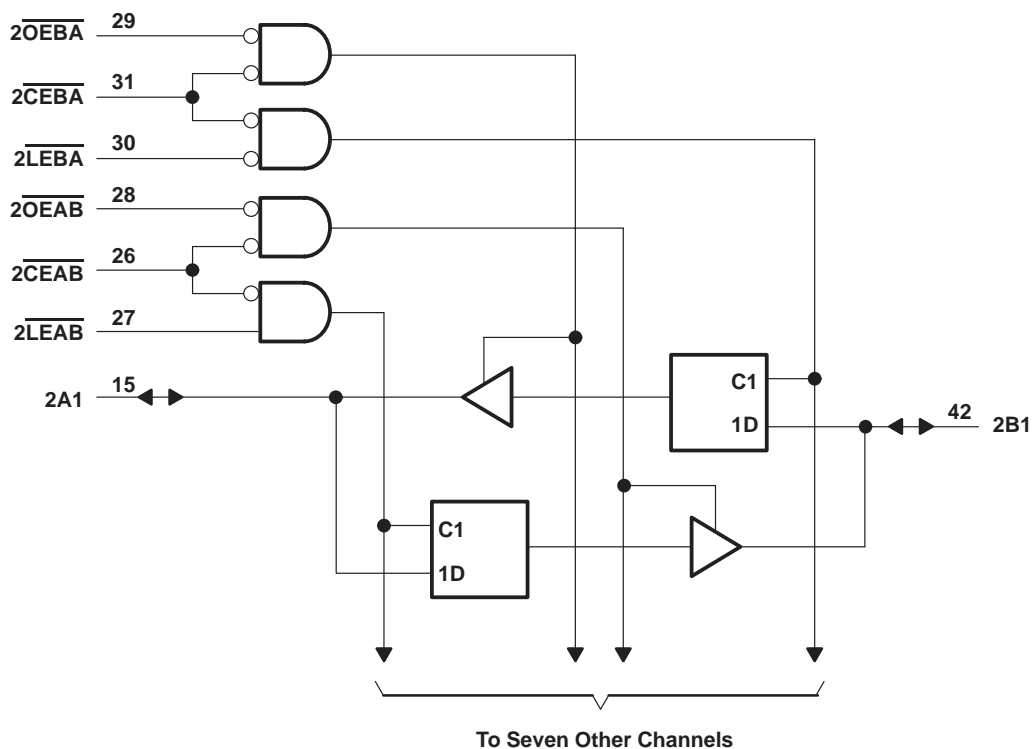
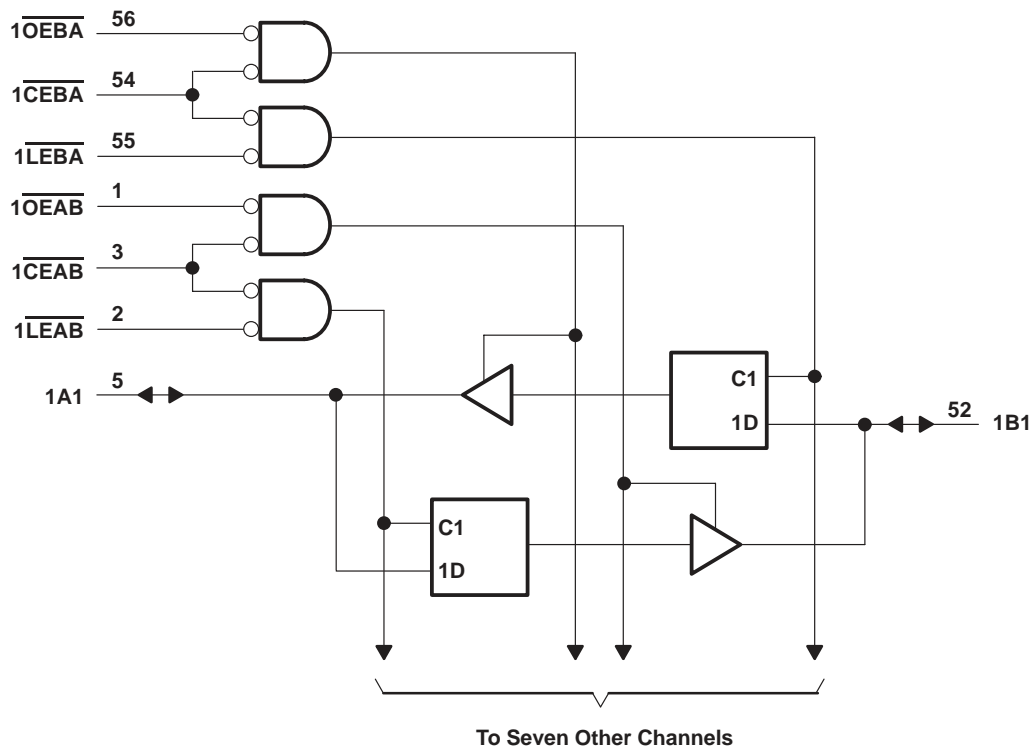
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



# SN74LVC16543 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

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## logic diagram (positive logic)



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	–0.5 V to 4.6 V
Input voltage range, $V_I$ : Except I/O ports (see Note 1) .....	–0.5 V to 4.6 V
I/O ports (see Notes 1 and 2) .....	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±50 mA
Continuous current through $V_{CC}$ or GND .....	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package .....	1 W
DL package .....	1.4 W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. This value is limited to 4.6 V maximum.  
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

**recommended operating conditions (see Note 4)**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.7	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
$I_{OL}$	Low-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> <sup>†</sup>	MIN	TYP <sup>‡</sup>	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = -100 μA	MIN to MAX	V <sub>CC</sub> -0.2			V
		I <sub>OH</sub> = -12 mA	2.7 V	2.2			
		I <sub>OH</sub> = -24 mA	3 V	2.4			
V <sub>OL</sub>		I <sub>OL</sub> = 100 μA	MIN to MAX			0.2	V
		I <sub>OL</sub> = 12 mA	2.7 V			0.4	
		I <sub>OL</sub> = 24 mA	3 V			0.55	
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V			±5	μA
I <sub>I</sub> (hold)	A or B ports	V <sub>I</sub> = 0.8 V	3 V	75			μA
		V <sub>I</sub> = 2 V		-75			
I <sub>OZ</sub> <sup>§</sup>		V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V			±10	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			40	μA
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			500	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			3	pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V			7	pF

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

<sup>§</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		UNIT
		MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, $\overline{LE}$ or $\overline{CE}$ low	4		4		ns
t <sub>su</sub>	Setup time, Data before $\overline{LE}$ , $\overline{CE}$	2		2		ns
t <sub>h</sub>	Hold time, Data after $\overline{LE}$ , $\overline{CE}$	2		2		ns

**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)**

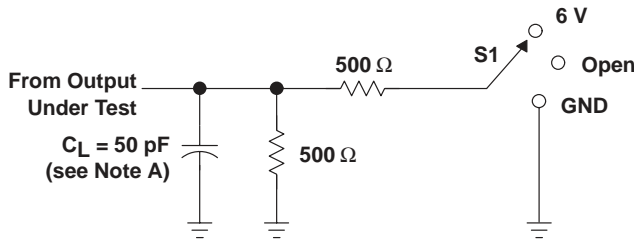
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A	1.5	8	1.5	9	ns
t <sub>pd</sub>	$\overline{LE}$	A or B	1.5	9	1.5	10	ns
t <sub>en</sub>	$\overline{CE}$	A or B	1.5	9	1.5	10	ns
t <sub>dis</sub>	$\overline{CE}$	A or B	1.5	9	1.5	10	ns
t <sub>en</sub>	$\overline{OE}$	A or B	1.5	8.5	1.5	9.5	ns
t <sub>dis</sub>	$\overline{OE}$	A or B	1.5	8.5	1.5	9.5	ns



operating characteristics,  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$

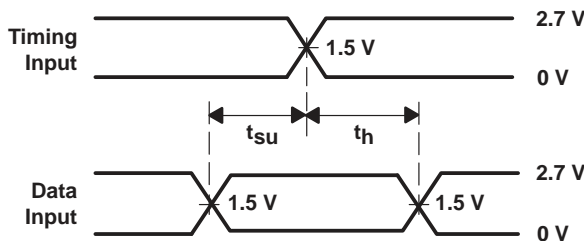
PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per transceiver	Outputs enabled	21	pF
		Outputs disabled	3.5	

**PARAMETER MEASUREMENT INFORMATION**

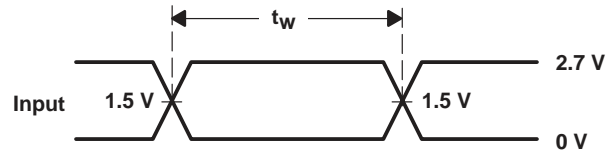


LOAD CIRCUIT

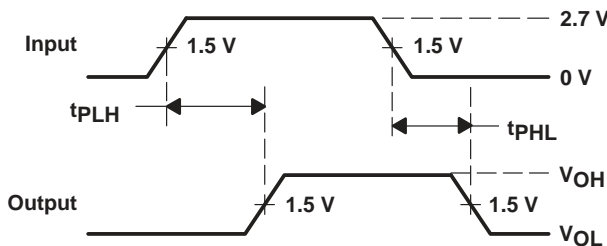
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



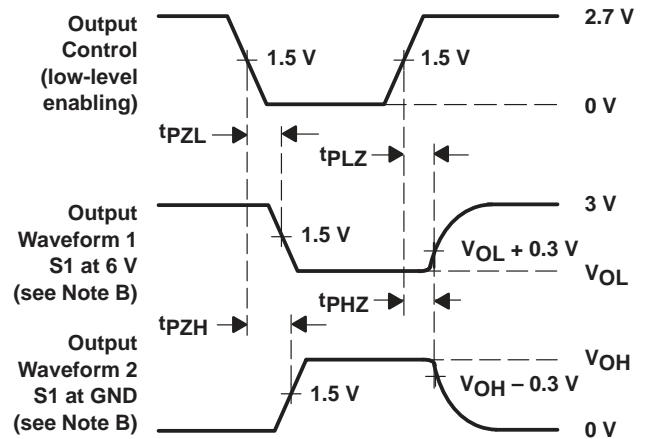
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

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