AOZ6762DI

EZBuck™ 2A 1.25MHz Synchronous Buck Regulator

General Description

The AOZ6762DI is a high efficiency, easy to use, 2A synchronous buck regulator at high switching frequency for small form factor solution. The AOZ6762DI works from 4.5V to 18V input voltage range, and provides up to 2A of continuous output current with an output voltage adjustable down to 0.6V.

The AOZ6762DI features fixed frequency operation at heavy load and Pulse Energy Mode (PEM) at light load, providing best efficiency across whole load range.

The AOZ6762DI comes in a DFN 3mm x 3mm 8-lead package and is rated over a -40°C to +85°C operating ambient temperature range.

Features

- 4.5V to 18V operating input voltage range
- Synchronous Buck: 145mΩ internal high-side switch and 90mΩ Internal low-side switch
- Up to 95% efficiency
- 30ns controllable minimum on-time enabling this part to operate at Vo=0.9V with 12V power rail
- Pulse Energy Mode for light load efficiency (V_{IN}=12V, V_{OUT}=5V, 87%@10mA)
- Output voltage adjustable to 0.6V
- 2A continuous output current
- Fixed frequency 1.25MHz PWM operation
- External compensation for flexible LC design
- Internal Soft Start
- Cycle-by-cycle current limit
- Pre-bias start-up
- Short-circuit protection
- Thermal shutdown

Applications

- High performance wireless AP/router
- High reliable DC/DC converters
- High performance LCD TV
- High performance cable modems

Green Product

Typical Application

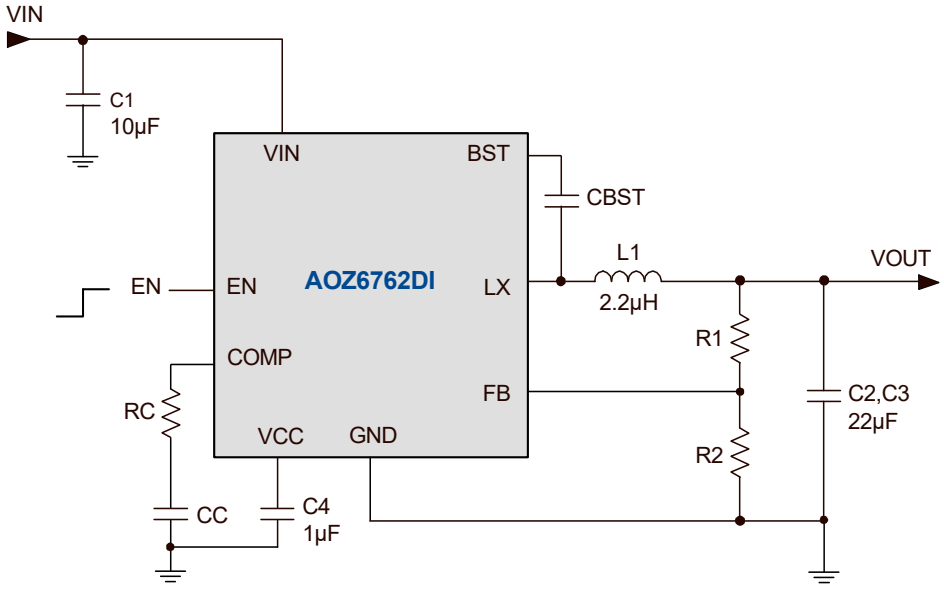


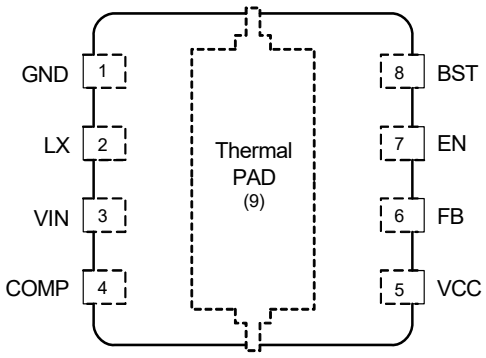
Figure 1. 2A Synchronous Buck Regulator, Fs = 1.25 MHz

Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ6762DI	-40°C to +85°C	DFN3X3-8L	RoHS

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



8-Pin 3mm x 3mm DFN
Top Transparent View

Pin Description

Pin Number	Pin Name	Pin Function
1	GND	System ground.
2	LX	Switching output.
3	VIN	Supply voltage input. When VIN rises above the UVLO threshold and EN is logic high, the device starts up.
4	COMP	External Loop Compensation Pin. Connect a RC network between COMP and GND to compensate the control loop.
5	VCC	The output of LDO. 1µF decoupling capacitor needs added.
6	FB	Feedback input. The FB pin is used to set the output voltage via a resistor voltage divider between the output and GND.
7	EN	Enable input. Pull up EN to logic high will enable the device. Pull EN to logic low will disable the device. If no enable control signal is available, this pin can be connected directly to VIN to enable the part. Do not leave it open.
8	BST	Bootstrap input for High-Side driver. Connect a capacitor to LX. Typical value is 0.1µF.
9	Thermal PAD	This thermal pad must be connected to GND for normal operation.

Absolute Maximum Ratings[1]

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
Supply Voltage (V_{IN})	20V
EN to GND	-0.3V to V_{IN}+0.3V
LX to GND	-0.3V to V_{IN}+0.3V
LX to GND Transient (20ns)	-5V to 22V
VCC, FB to GND	-0.3V to 6V
BST TO LX	6V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating[2]	2kV

Notes:

1. Exceeding the Absolute Maximum ratings may damage the device.
2. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Maximum Operating Ratings[3]

The device is not guaranteed to operate beyond the Maximum Operating ratings.

Parameter	Rating
Supply Voltage (V_{IN})	4.5V to 18V
Output Voltage Range	0.6V to 6V
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance DFN 3x3 (θ_{JA})[4]	50°C/W

Notes:

3. The device is not guaranteed to operate beyond the Maximum Operating ratings.
4. The value of θ_{JA} is measured with the device mounted on a 1-in^2 FR-4 four layer board with 2oz copper and Vias, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specification board design.

Electrical Characteristics

T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V, unless otherwise specified. Specifications in **Bold** indicate an ambient temperature range of -40°C to +85°C. These specifications are guaranteed by design.

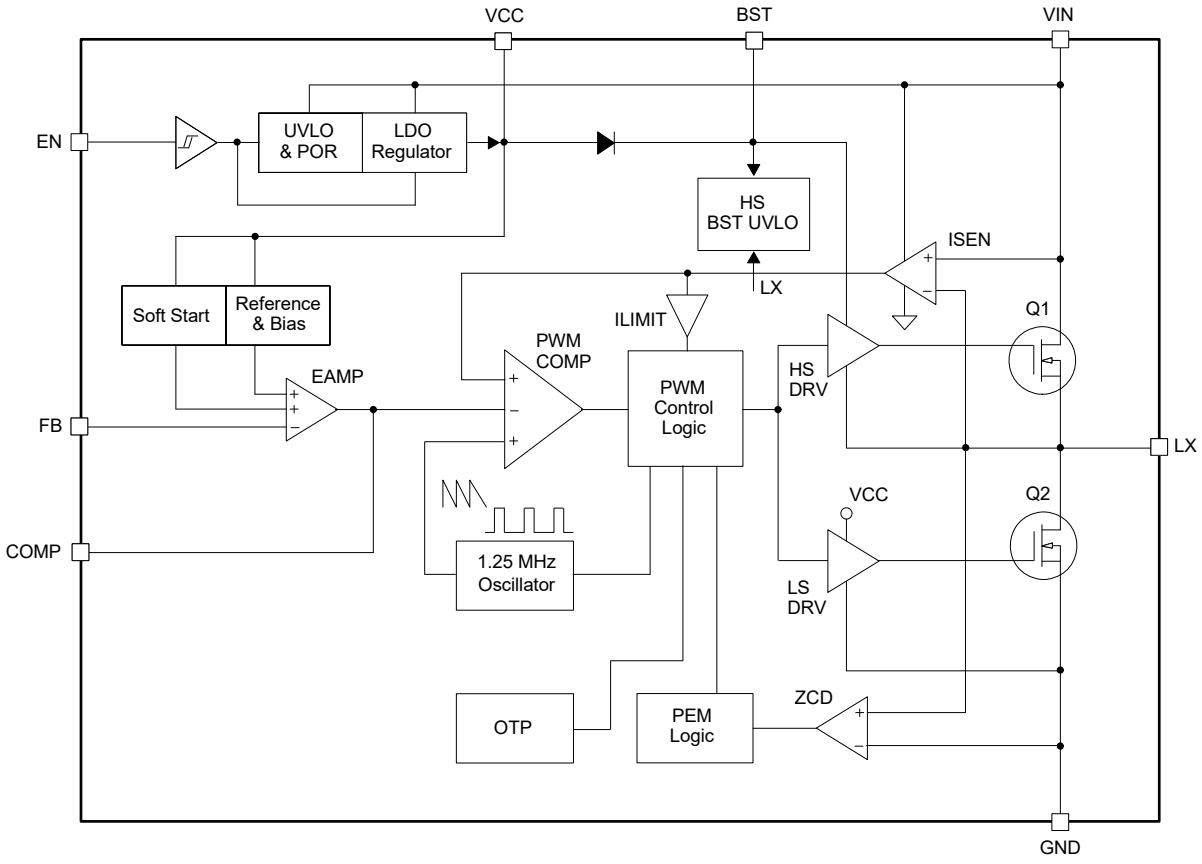
Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{IN}	Supply Voltage		**4.5**		**18**	V
V_{UVLO}	Input Under-Voltage Lockout Threshold	V_{IN} rising V_{IN} falling	 **3.2**	4.1 3.7	**4.49**	V V
I_{IN}	Supply Current (Quiescent)	I_{OUT} = 0V, VFB = 1.2V, V_{EN} > 2V		260		µA
I_{OFF}	Shutdown Supply Current	V_{EN} = 0V		0.1	1	µA
V_{FB}	Feedback Voltage	T_A = 25°C	0.591	0.6	0.609	V
R_O	Load Regulation	PWM mode 0.5A < ILoad < 2A		0.5		%
S_V	Line Regulation	4.5V < V_{IN} < 18V		1		%
I_{FB}	Feedback Voltage Input Current				200	nA
V_{EN}	EN Input Threshold	Off threshold On threshold	 **2**		**0.6**	V V
V_{HYS}	EN Input Hysteresis			300		mV
I_{EN}	EN Input Current	V_{EN} = 5V		2.5	4	µA
t_{SS}	SS Time			3.5		ms
Modulator						
f_O	Frequency		1100	1250	1400	kHz
D_{MAX}	Maximum Duty Cycle		65	70		%
t_{MIN}	Controllable Minimum Duty Cycle			30		ns
Protection						
I_{LIM}	Current Limit		3.0	4.0		A
T_{OTP}	Over Temperature Shutdown Limit	T_J rising T_J falling		150 120		°C °C

Electrical Characteristics

T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V, unless otherwise specified. Specifications in **Bold** indicate an ambient temperature range of -40°C to +85°C. These specifications are guaranteed by design.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
Output Stage						
R_{HS}	High-Side Switch On-Resistance	BST - LX = 5V		145		mΩ
R_{LS}	Low-Side Switch On-Resistance			90		mΩ

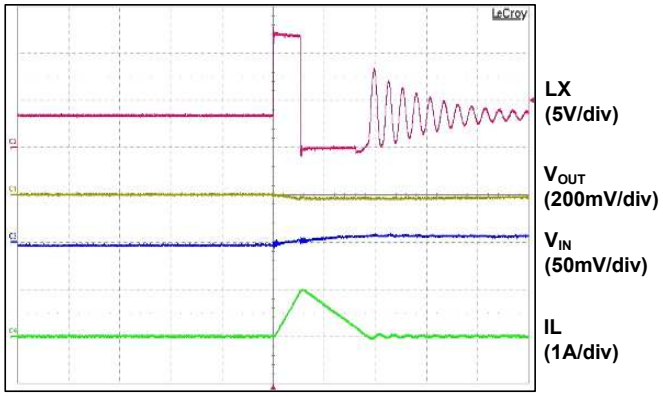
Functional Block Diagram



Typical Characteristics

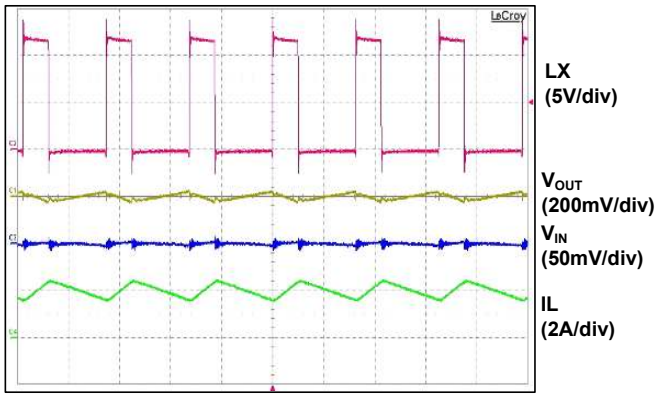
T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V, unless otherwise specified.

Light Load Operation



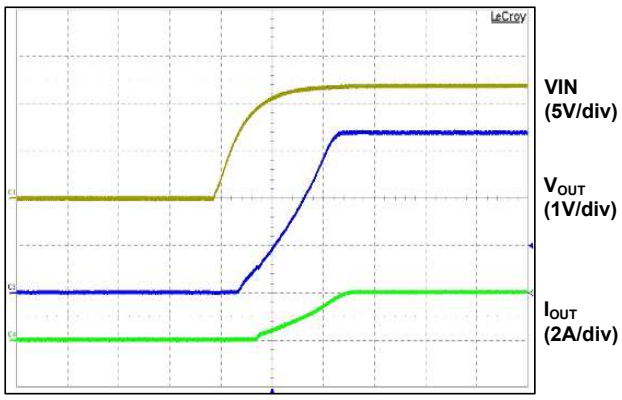
1µs/div

Full Load Operation



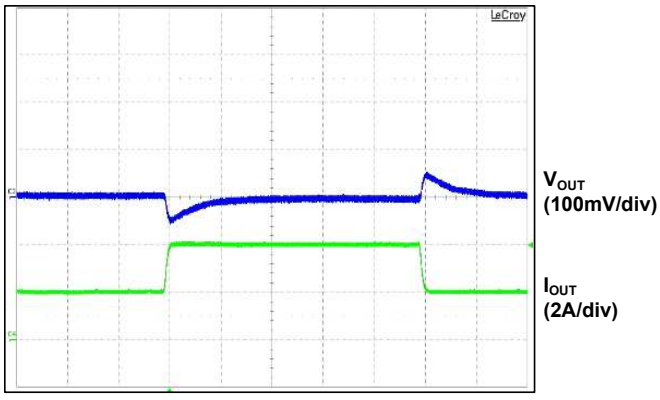
0.5µs/div

Start-up to Full Load



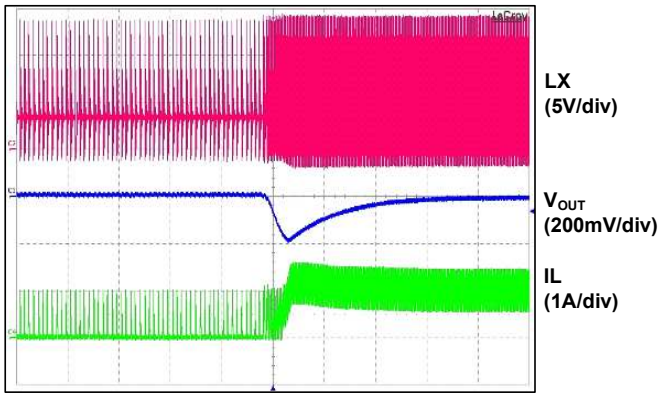
1ms/div

50% to 100% Load Transient



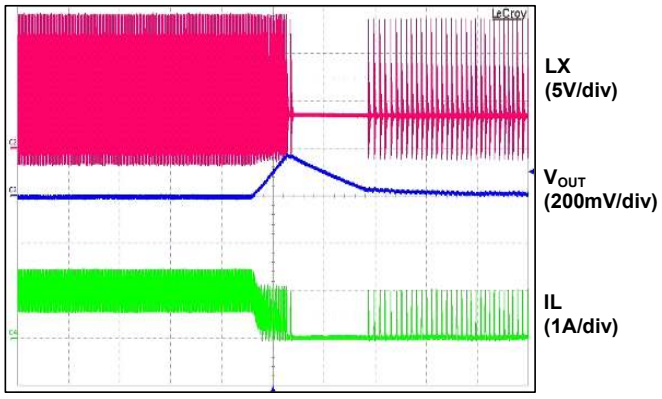
200µs/div

PEM to PWM Transition



0.5ms/div

PWM to PEM Transition

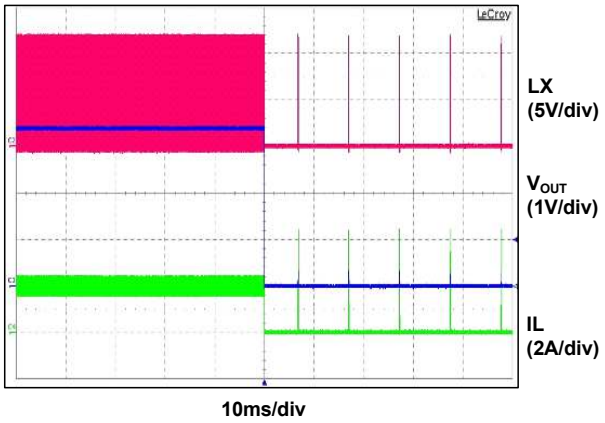


0.5ms/div

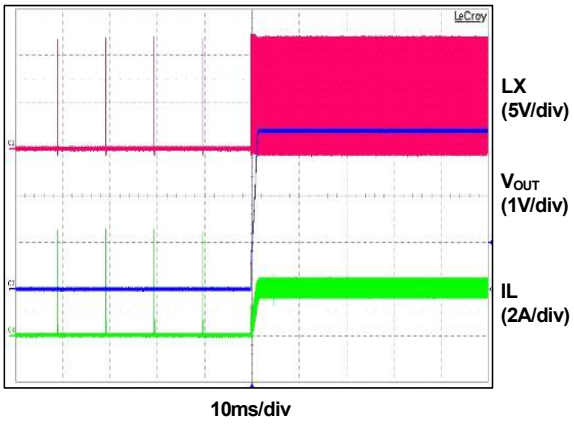
Typical Characteristics *(continued)*

T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V, unless otherwise specified.

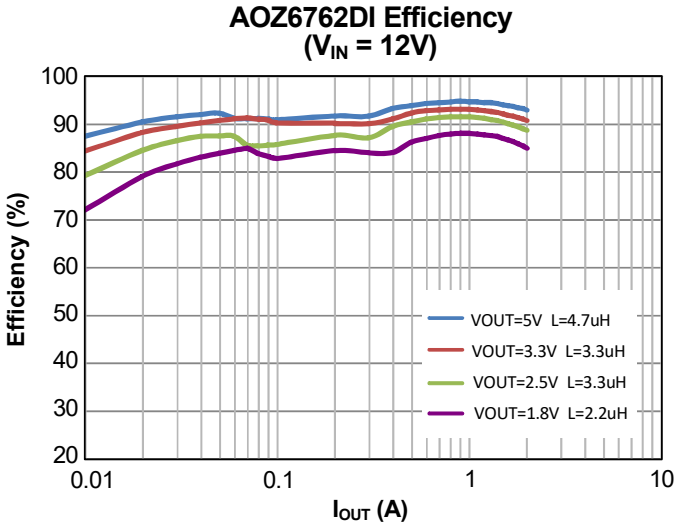
Short Protection



Short Circuit Recovery



Efficiency



Detailed Description

The AOZ6762DI is a current-mode step down regulator with integrated High-Side and Low-Side power switches. The regulator operates from 4.5V to 18V input voltage range and supplies up to 2A of load current. Functional features such as enable control rated up to VIN, Power-On Reset (POR), input Under-Voltage Lockout (UVLO), output Over Voltage Protection (OVP), internal soft-start, cycle-by-cycle current limit, and Over-temperature Protection (OTP) are built in. AOZ6762DI is available in DFN3x3-8L package.

Enable and Soft Start

The AOZ6762DI has internal soft start feature to limit the in-rush current and ensure the output voltage ramps up smoothly to regulation voltage during start up. A soft start process begins when the input voltage rises above 4.1V and voltage on EN pin is higher than 2V. The soft start time is pre-programmed to 3.5ms typical.

The EN pin of the regulator is active high. The voltage at EN pin must be above 2V to enable the device. When the voltage at EN pin falls below 0.6V, the device is disabled. To ensure proper operation, EN pin must be biased to solid voltage level in either enable or disable state. EN pin is rated up to VIN voltage. This feature allows for simple design with EN pin directly tied to VIN to minimize component count and system complexity, if no enable control signal is available.

Steady-State Operation

Under heavy load steady-state conditions, the converter operates in fixed frequency and Continuous-Conduction Mode (CCM).

The AOZ6762DI is using current mode control for regulation. Inductor current is sensed through the current being conducted by the power MOSFET. Output voltage is determined by the external voltage divider between VOUT, FB, and GND. The difference of the FB voltage and internal reference voltage is amplified by the transconductance error amplifier. The error voltage is compared against the current signal (sum of inductor current signal and input ramp compensation signal) at PWM comparator stage. If the current signal is less than the error voltage, the high-side switch is turned on. The inductor current flows from the VIN through the inductor to the VOUT. When the current signal exceeds the error voltage, the High-Side switch is turned off. The inductor current is freewheeling through the Low-Side switch from GND to VOUT.

The internal adaptive gate drivers guarantee no turn on overlap between High-Side and Low-Side switches to prevent any shoot-through condition.

Comparing with non-synchronous converters using freewheeling Schottky diodes, the AOZ6762DI use synchronous power switch to greatly improve the converter efficiency by reducing power loss in the Low-Side switch.

Light Load Operation

Under low output current settings, the AOZ6762DI will operate with pulse energy mode (PEM) to obtain high efficiency. The main goal of PEM is to reduce the switching loss as it is the main source of energy loss at low load. Under this mode, the High-Side switch will not turn off until its on-time reaches a controlled duration which is determined by input voltage (VIN), output voltage (VOUT), and switching frequency (f_O). The Low-Side switch will be turned off eventually when inductor current is close to 0A. Both switches are off and LX is in high impedance state until VOUT drops to a pre-determined level and more energy is needed to bring the VOUT back to regulated voltage. The High-Side switch will then be turned on at the beginning of the clock cycle.

Bootstrap Supply for High-Side Switch

This converter uses a N-Channel MOSFET as the High-Side switch. Since the N-Channel MOSFET requires a gate voltage higher than the input voltage to turn on, a bootstrap capacitor is needed between LX pin (Pin 2) and BST pin (Pin 8) to drive the gate of the MOSFET. The boost capacitor is being charged while LX is low. Typical 0.1µF capacitor is recommended for most applications.

Output Voltage Programming

Output voltage (VOUT) can be set by feeding back the VOUT to the FB pin through a resistor divider network as shown in Figure 1. Design starts by selecting a fixed R2 value and then calculates the required R1 using the equation below:

$$V_{OUT} = FB \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Combination of R1 and R2 should be large enough to avoid drawing excessive current from the output, which will cause power loss.

Some standard value of R_1, R_2 and most used output voltage values are listed in Table 1.

Table 1: Typical Resistor Divider Values for FB Input

VO (V)	R1 (kΩ)	R2 (kΩ)
0.6	10	OPEN
0.8	3.4	10.2
0.9	7.5	15
1.0	10	15
1.2	10	10
1.5	15	10
1.8	20	10
2.5	31.6	10
3.3	68.1	15
5.0	110	15
6.0	180	20

Protection Features

The AOZ6762DI has multiple protection features to prevent system circuit damage under abnormal conditions.

Over Current Protection (OCP)

The output current from LX pin is being monitored cycle by cycle. If the output current exceeds the preset limit, the switch will be turned off to prevent excessive power being dissipated by the converter. If output drops to certain level during OC condition, the part will shut down and auto restart with hiccup mode.

Power-On Reset (POR)

A power-on reset circuit monitors the VIN voltage. When the VIN voltage exceeds 4.1V, the converter starts to operate if EN > 2V. When VIN voltage falls below 3.7V, the converter will be shut down.

Thermal Protection

An internal temperature sensor monitors the junction temperature. It shuts down the internal control circuit and both High-Side and Low-Side switches if the junction temperature exceeds 150ºC. The regulator will restart automatically under the control of soft-start circuit when the junction temperature decreases to 120ºC.

Application Information

Operating Range

For any output voltage setting, minimum input voltage supported by AOZ6762DI is governed by maximum duty cycle allowed by the regulator. Maximum duty cycle is input voltage dependent, where it decreases as VIN goes lower. The minimum input voltage required for certain output voltage setting is shown in Figure 2.

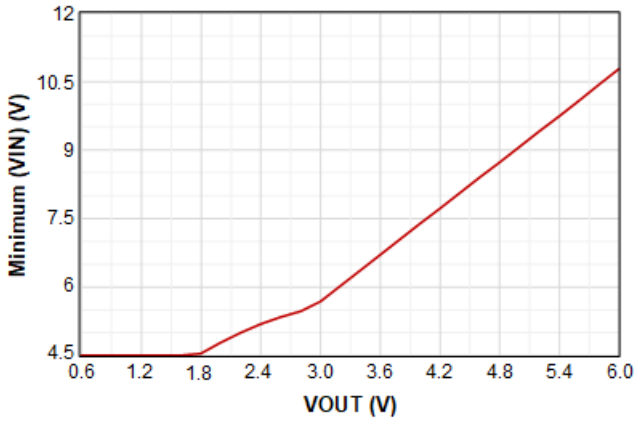


Figure 2. Minimum Input Voltage Required vs. Output Voltage Setting

Input Capacitor

The input capacitor must be connected to the VIN pin and GND pin to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_o \times C_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \frac{V_{OUT}}{V_{IN}} \quad (2)$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

if let *m* equal the conversion ratio:

$$\frac{V_{OUT}}{V_{IN}} = m \quad (4)$$

The relation between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure 3 below. It can be seen that when V_{OUT} is half of

V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is $0.5 \cdot I_{OUT}$.

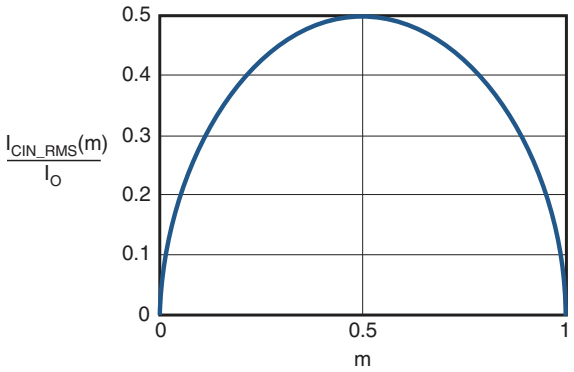


Figure 3. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than $I_{CIN-RMS}$ at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high current rating. Depending on the application circuits, other low ESR tantalum capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors should be used for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures are based on certain amount of life time. Further de-rating may be necessary in practical design.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is:

$$\Delta I_L = \frac{V_{OUT}}{f_o \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

The peak inductor current is:

$$I_{Lpeak} = I_{OUT} + \frac{\Delta I_L}{2} \quad (6)$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 20% to 40% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor need to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR_{C2} + \frac{1}{8 \times f_o \times C_2}\right) \quad (7)$$

where C2 is output capacitor value and ESR_{C2} is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_{OUT} = \Delta I_L \times \frac{1}{8 \times f_o \times C_2} \quad (8)$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{C2} \quad (9)$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}} \quad (10)$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

Loop Compensation

AOZ6762DI employs peak current mode control for easy use and fast transient response. Peak current mode control eliminates the double pole effect of the output L&C filter. It greatly simplifies the compensation loop design.

With peak current mode control, the buck power stage can be simplified to be a one-pole and one-zero system in frequency domain. The pole is dominant pole can be calculated by:

$$f_{p1} = \frac{1}{2\pi \times C2 \times R_L} \quad (11)$$

The zero is a ESR zero due to output capacitor and its ESR. It is can be calculated by:

$$f_{z1} = \frac{1}{2\pi \times C2 \times ESR_{C2}} \quad (12)$$

Where C2 is the output filter capacitor;

R_L is load resistor value;

ESR_{C2} is the equivalent series resistance of output capacitor;

The compensation design is actually to shape the converter control loop transfer function to get desired gain and phase. Several different types of compensation network can be used. For most cases, a series capacitor and resistor network connected to the COMP pin sets the pole and zero and it is adequate for a stable high bandwidth control loop.

Using the series R and C compensation network connected to COMP provides one pole and one zero. The pole is:

$$f_{p2} = \frac{G_{EA}}{2\pi \times C_C \times G_{VEA}} \quad (13)$$

Where G_{EA} is the error amplifier transconductance, (260μA/V);

G_{VEA} is the error amplifier voltage gain, (40V/mV);

C_c is compensation capacitor in Figure1;

The zero given by the external compensation network, capacitor Cc and resistor Rc, is located at:

$$f_{z2} = \frac{1}{2\pi \times C_C \times R_C} \quad (14)$$

To design the compensation circuit, a target crossover frequency f_C for close loop must be selected. The system crossover frequency is where control loop has unity gain. The crossover is the also called the converter bandwidth. Generally, a higher bandwidth means faster response to load transient. However, the bandwidth should not be too high because of system stability concern. When designing the compensation loop, converter stability under all line and load condition must be considered.

Usually, it is recommended to set the bandwidth to be equal or less than 1/10 of switching frequency.

The strategy for choosing R_C and C_C is to set the cross over frequency with R_C and set the compensator zero with C_C. Using selected crossover frequency, f_C, to calculate R_C:

$$R_C = f_C \times \frac{V_{OUT}}{FB} \times \frac{2\pi \times C2}{G_{EA} \times G_{cs}} \quad (15)$$

where f_C is desired crossover frequency. For best performance, fc is set to be about 1/10 of switching frequency;

FB is 0.6V;

G_{EA} is the error amplifier transconductance; (260μA/V),

G_{CS} is the current sense circuit transconductance, which is (4.45A/V);

The compensation capacitor C_c and resistor R_c together make a zero. This zero is put somewhere

close to the dominate pole f_{P1} but lower than 1/5 of selected crossover frequency. C_C can is selected by:

Equation above can also be simplified to:

$$C_C = \frac{C_O \times R_L}{R_C} \quad (16)$$

An easy-to-use application software which helps to design and simulate the compensation loop can be found at www.aosmd.com.

Thermal Management and Layout Consideration

In the AOZ6762DI buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the VIN pin, to the LX pad, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the High-Side switch is on. The second loop starts from inductor, to the output capacitors and load, to the Low-Side switch. Current flows in the second loop when the Low-Side switch is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is strongly recommended to connect input capacitor, output capacitor, and GND pin of the regulator.

In the buck regulator application, the major power dissipating components are the AOZ6762DI and the output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total\_loss} = V_{IN} \times I_{IN} - V_{OUT} \times I_{OUT} \quad (17)$$

The power dissipation of inductor can be approximately calculated by output current and DCR of inductor.

$$P_{inductor\_loss} = I_{OUT}^2 \times R_{inductor} \times 1.1 \quad (18)$$

The actual junction temperature can be calculated with power dissipation in the AOZ6762DI and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total\_loss} - P_{inductor\_loss}) \times \Theta_{JA} + T_A \quad (19)$$

The thermal performance of the AOZ6762DI is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

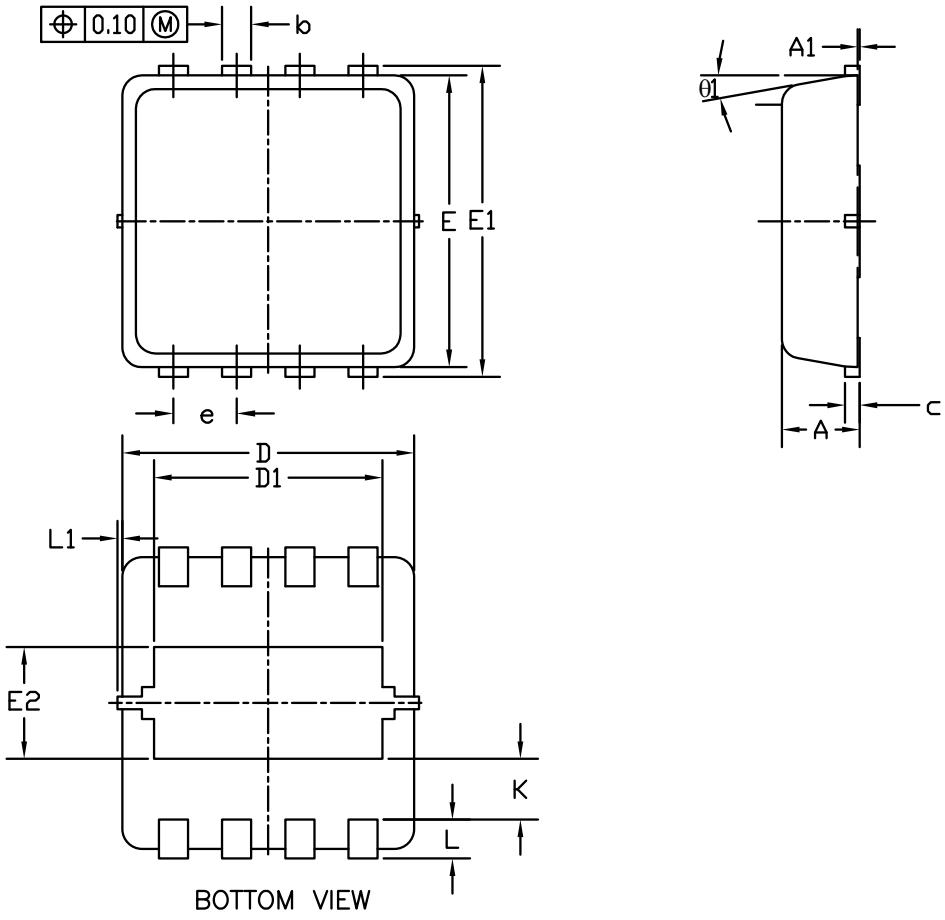
The maximum junction temperature of the regulator is 150ºC, which limits the maximum load current capability.

Layout Consideration

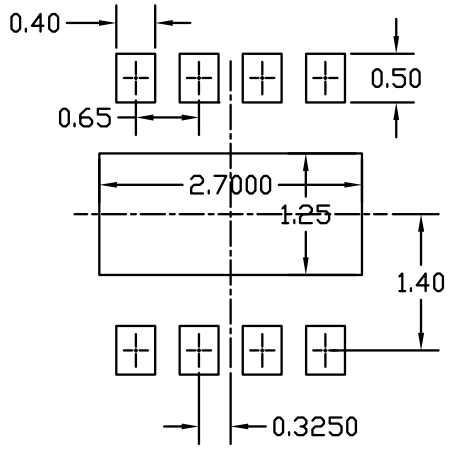
AOZ6762DI is using exposed pad DFN3x3 package. Several layout tips are listed below for the best electric and thermal performance.

1. The exposed thermal pad has to connect to ground by PCB externally. Connect a large copper plane to exposed thermal pad to help thermal dissipation.
2. Do not use thermal relief connection to the VIN and the GND pin. Pour a maximized copper area to the GND pin and the VIN pin to help thermal dissipation.
3. Input capacitor should be connected to the VIN pin and the GND pin as close as possible.
4. Make the current trace from LX pins to L1 to C2 to the GND as short as possible.
5. Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, GND or VOUT.
6. Keep sensitive signal trace far away from the LX pad.

Package Dimensions, DFN3x3B-8L



RECOMMENDED LAND PATTERN

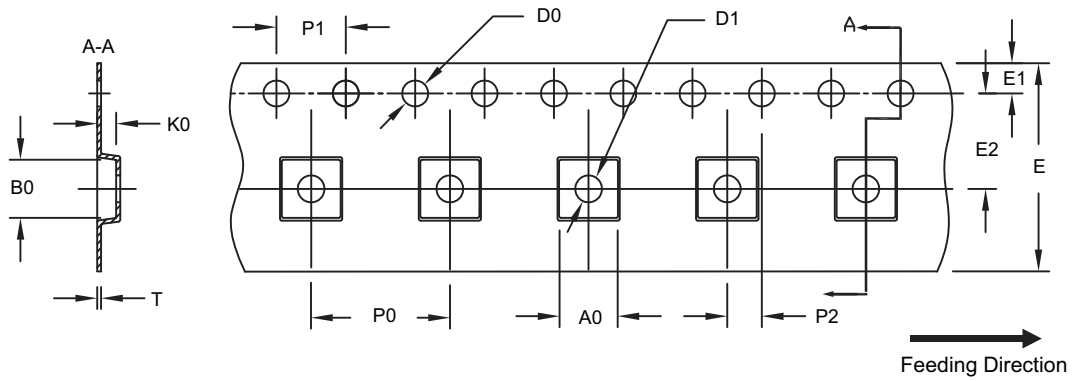


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.80	0.90	0.028	0.031	0.035
A1	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.10	0.15	0.25	0.004	0.006	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	2.15	2.35	2.55	0.085	0.093	0.100
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	3.05	3.20	3.35	0.120	0.126	0.132
E2	1.10	1.15	1.20	0.043	0.045	0.047
e	0.60	0.65	0.70	0.024	0.026	0.028
K	0.575	0.625	0.675	0.023	0.025	0.027
L	0.30	0.40	0.50	0.012	0.016	0.020
L1	0	---	0.10	0	---	0.004
θ1	0	10	12	0	10	12

NOTE
1. PAKCAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
   MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
2. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, DFN3x3-8L

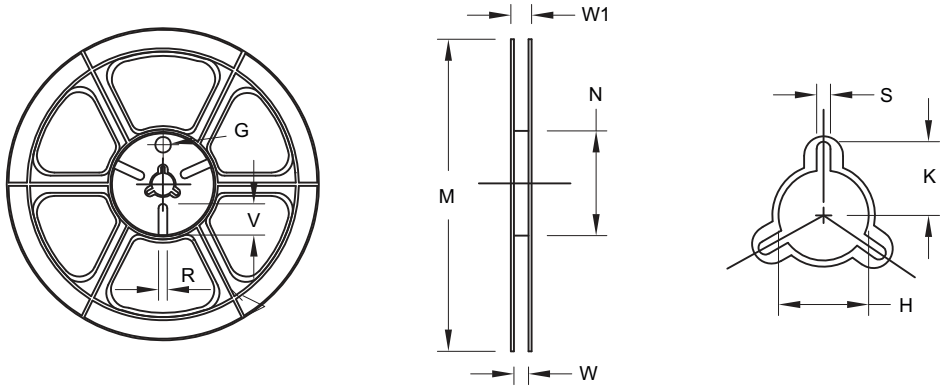
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN 3x3 EP	3.40 ±0.10	3.35 ±0.10	1.10 ±0.10	1.50 +0.10/-0	1.50 +0.10/-0	12.00 ±0.30	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

Reel

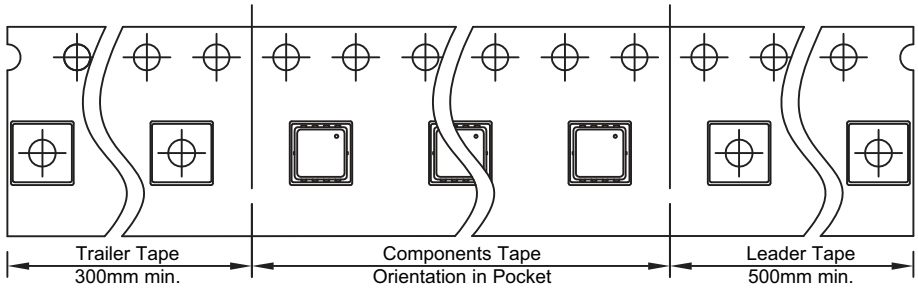


UNIT: mm

Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ø330	ø330.0 ±0.50	ø97.0 ±1.0	13.0 ±0.30	17.4 ±1.0	ø13.0 +0.5/-0.2	10.6	2.0 ±0.5	—	—	—

Leader/Trailer and Orientation

Unit Per Reel:
5000pcs



Part Marking