Revision History List

512K x 16 bit -AS6C8016-55TIN - 48-pin TSOP I PACKAGE

Revision	Details	Date
Rev. 1.0	Initial Issue	November12.2015

ALLIANCE MEMORY

AS6C8016-55TIN

FEATURES

- Fast access time : 55ns
- Low power consumption:
  Operating current : 30/20mA (TYP.)
  Standby current : 1.5μA (TYP.) SL-version
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)
  UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.2V(MIN.)

- Package : 48-pin 12mm x 20mm TSOP-I
- Green & ROHS Compliant

GENERAL DESCRIPTION

The AS6C8016-55TIN is a 8,388,608-bit low power CMOS static random access memory organized as 524,288 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS6C8016-55TIN is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The AS6C8016-55TIN operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible
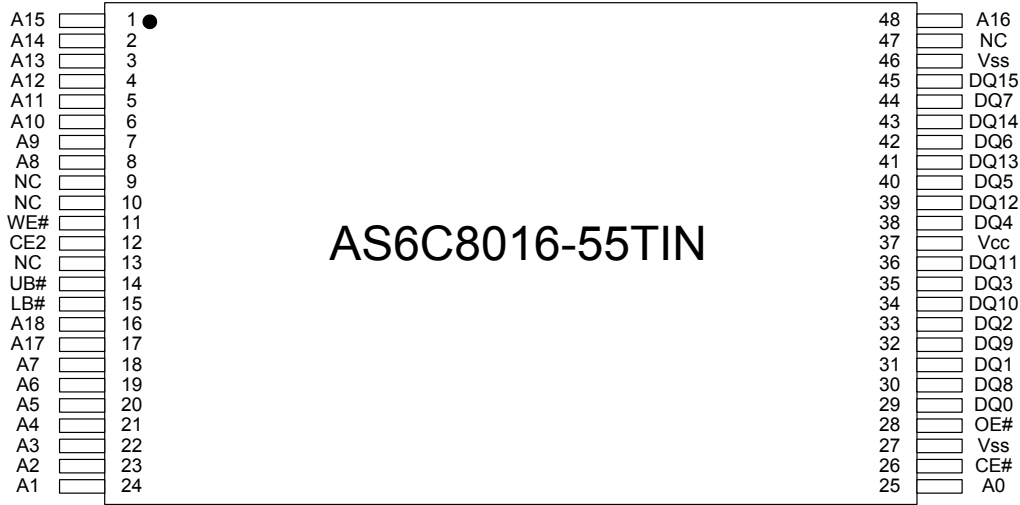
FUNCTIONAL BLOCK DIAGRAM
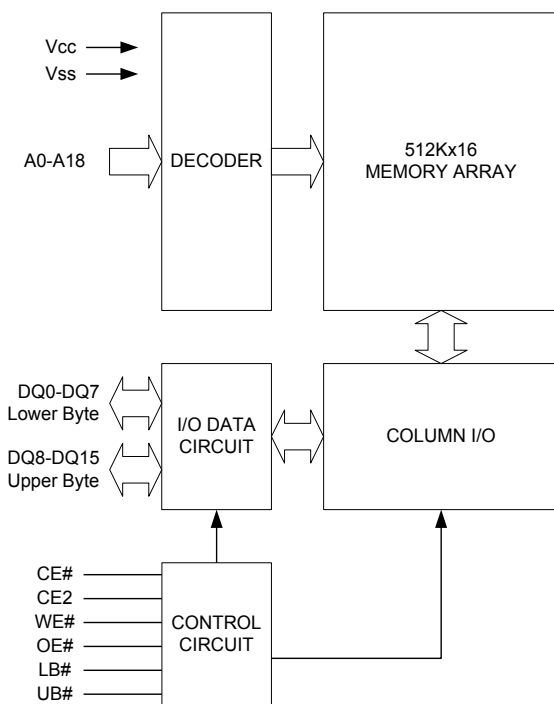
PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
DQ0 – DQ15	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
V_{CC}	Power Supply
V_{SS}	Ground

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I_{SB1},TYP.)	Operating(Icc,TYP.)
AS6C8016-55TIN	-40°C ~ 85°C	2.7 ~ 3.6V	55ns	1.5μA(SL)	30/20mA

PIN CONFIGURATION

```
         A15 ┌ 1●          48 ┐ A16
         A14 ┌ 2           47 ┐ NC
         A13 ┌ 3           46 ┐ Vss
         A12 ┌ 4           45 ┐ DQ15
         A11 ┌ 5           44 ┐ DQ7
         A10 ┌ 6           43 ┐ DQ14
          A9 ┌ 7           42 ┐ DQ6
          A8 ┌ 8           41 ┐ DQ13
          NC ┌ 9           40 ┐ DQ5
          NC ┌ 10          39 ┐ DQ12
         WE# ┌ 11          38 ┐ DQ4
         CE2 ┌ 12          37 ┐ Vcc
          NC ┌ 13          36 ┐ DQ11
         UB# ┌ 14          35 ┐ DQ3
         LB# ┌ 15          34 ┐ DQ10
         A18 ┌ 16          33 ┐ DQ2
         A17 ┌ 17          32 ┐ DQ9
          A7 ┌ 18          31 ┐ DQ1
          A6 ┌ 19          30 ┐ DQ8
          A5 ┌ 20          29 ┐ DQ0
          A4 ┌ 21          28 ┐ OE#
          A3 ┌ 22          27 ┐ Vss
          A2 ┌ 23          26 ┐ CE#
          A1 ┌ 24          25 ┐ A0

              AS6C8016-55TIN
```

TSOP-I

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to V_{CC}+0.5	V
Operating Temperature	T_A	0 to 70(C grade)	℃
		-40 to 85(I grade)	
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
							DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	X	High – Z	High – Z	I_{SB}, I_{SB1}
	X	L	X	X	X	X	High – Z	High – Z	
	X	X	X	X	H	H	High – Z	High – Z	
Output Disable	L	H	H	H	L	X	High – Z	High – Z	I_{CC}, I_{CC1}
	L	H	H	H	X	L	High – Z	High – Z	
Read	L	H	L	H	L	H	D_{OUT}	High – Z	I_{CC}, I_{CC1}
	L	H	L	H	H	L	High – Z	D_{OUT}	
	L	H	L	H	L	L	D_{OUT}	D_{OUT}	
Write	L	H	X	L	L	H	D_{IN}	High – Z	I_{CC}, I_{CC1}
	L	H	X	L	H	L	High – Z	D_{IN}	
	L	H	X	L	L	L	D_{IN}	D_{IN}	

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP. [4]	MAX.	UNIT
Supply Voltage	V_{CC}				2.7	3.0	3.6	V
Input High Voltage	V_{IH} [1]				2.2	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL} [2]				- 0.2	-	0.6	V
Input Leakage Current	I_{LI}	V_{CC} V_{IN} V_{SS}			- 1	-	1	µA
Output Leakage Current	I_{LO}	V_{CC} V_{OUT} V_{SS}, Output Disabled			- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -1mA			2.2	2.7	-	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA			-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = Min. CE# = V_{IL} and CE2 = V_{IH} $I_{I/O}$ = 0mA Other pins at V_{IL} or V_{IH}	- 55		-	30	40	mA
			- 70		-	20	30	mA
	I_{CC1}	Cycle time = 1µs CE#≦0.2V and CE2≧V_{CC}-0.2V $I_{I/O}$ = 0mA Other pins at 0.2V or V_{CC}-0.2V			-	4	8	mA
Standby Power Supply Current	I_{SB}	CE# = V_{IH} or CE2 = V_{IL} Other pins at V_{IL} or V_{IH}			-	0.15	1	mA
	I_{SB1}	CE# V_{CC}-0.2V or CE2≦0.2V Other pins at 0.2V or V_{CC}-0.2V	*SLI [5]	25℃	-	1.5	5	µA
				40℃	-	1.5	5	µA
					-			
			SLI		-	1.5	20	µA

Notes:
1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
   Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25℃
5. This parameter is measured at V_{CC} = 3.0V

CAPACITANCE (T$_A$ = 25 , f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C$_{IN}$	-	6	pF
Input/Output Capacitance	C$_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V$_{CC}$ - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C$_L$ = 30pF + 1TTL, I$_{OH}$/I$_{OL}$ = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	AS6C8016-55TIN		UNIT
		MIN.	MAX.	
Read Cycle Time	t$_{RC}$	55	-	ns
Address Access Time	t$_{AA}$	-	55	ns
Chip Enable Access Time	t$_{ACE}$	-	55	ns
Output Enable Access Time	t$_{OE}$	-	30	ns
Chip Enable to Output in Low-Z	t$_{CLZ}$*	10	-	ns
Output Enable to Output in Low-Z	t$_{OLZ}$*	5	-	ns
Chip Disable to Output in High-Z	t$_{CHZ}$*	-	20	ns
Output Disable to Output in High-Z	t$_{OHZ}$*	-	20	ns
Output Hold from Address Change	t$_{OH}$	10	-	ns
LB#, UB# Access Time	t$_{BA}$	-	55	ns
LB#, UB# to High-Z Output	t$_{BHZ}$*	-	25	ns
LB#, UB# to Low-Z Output	t$_{BLZ}$*	10	-	ns

(2) WRITE CYCLE

PARAMETER	SYM.	AS6C8016-55TIN		UNIT
		MIN.	MAX.	
Write Cycle Time	t$_{WC}$	55	-	ns
Address Valid to End of Write	t$_{AW}$	50	-	ns
Chip Enable to End of Write	t$_{CW}$	50	-	ns
Address Set-up Time	t$_{AS}$	0	-	ns
Write Pulse Width	t$_{WP}$	45	-	ns
Write Recovery Time	t$_{WR}$	0	-	ns
Data to Write Time Overlap	t$_{DW}$	25	-	ns
Data Hold from End of Write Time	t$_{DH}$	0	-	ns
Output Active from End of Write	t$_{OW}$*	5	-	ns
Write to Output in High-Z	t$_{WHZ}$*	-	20	ns
LB#, UB# Valid to End of Write	t$_{BW}$	45	-	ns

*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

**READ CYCLE 1** (Address Controlled) (1,2)

Address

t_{RC}

t_{AA}

t_{OH}

Dout — Previous Data Valid — Data Valid
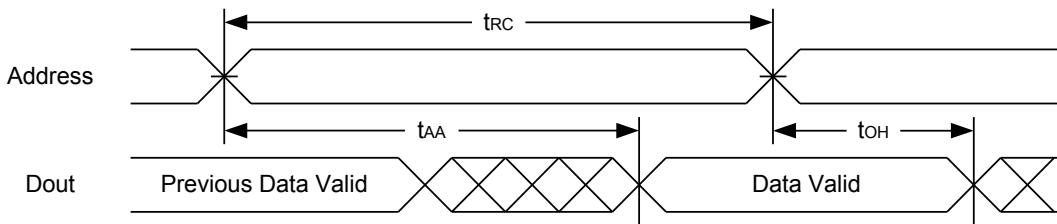
READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

Address

t_{RC}

t_{AA}

CE#

t_{ACE}

CE2

LB#,UB#

t_{BA}

OE#

t_{OE}

t_{OLZ}

t_{BLZ}

t_{CLZ}

t_{OH}

t_{OHZ}

t_{BHZ}

t_{CHZ}

Dout — High-Z — Data Valid — High-Z
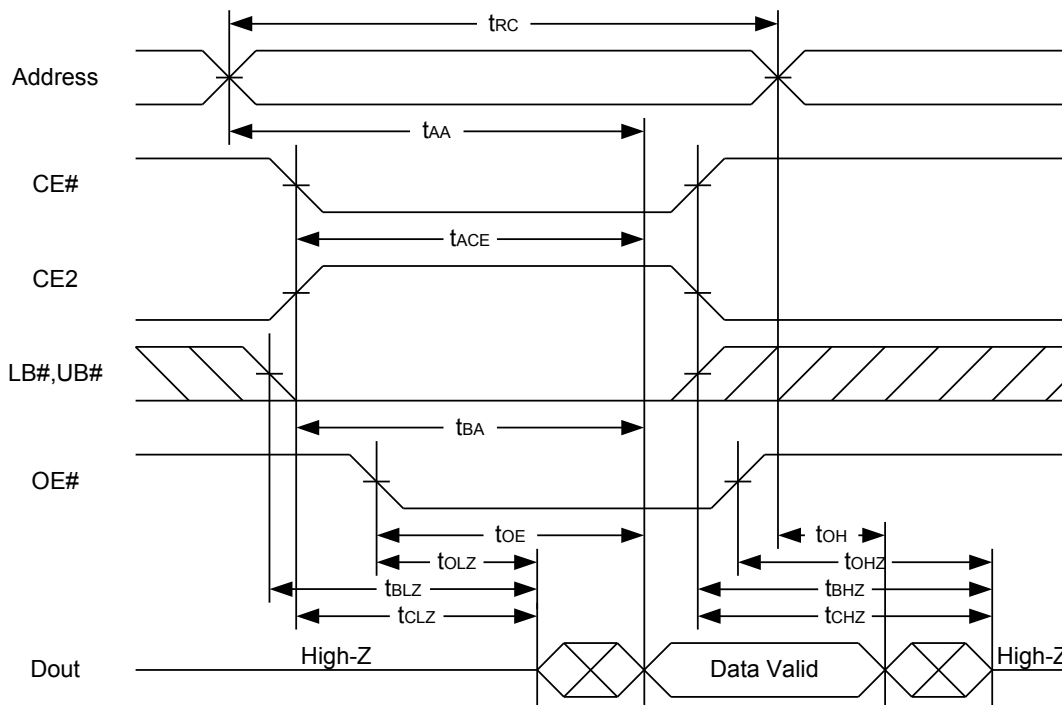
Notes :
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ}, t_{BLZ}, t_{OLZ}, t_{CHZ}, t_{BHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ}, t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)
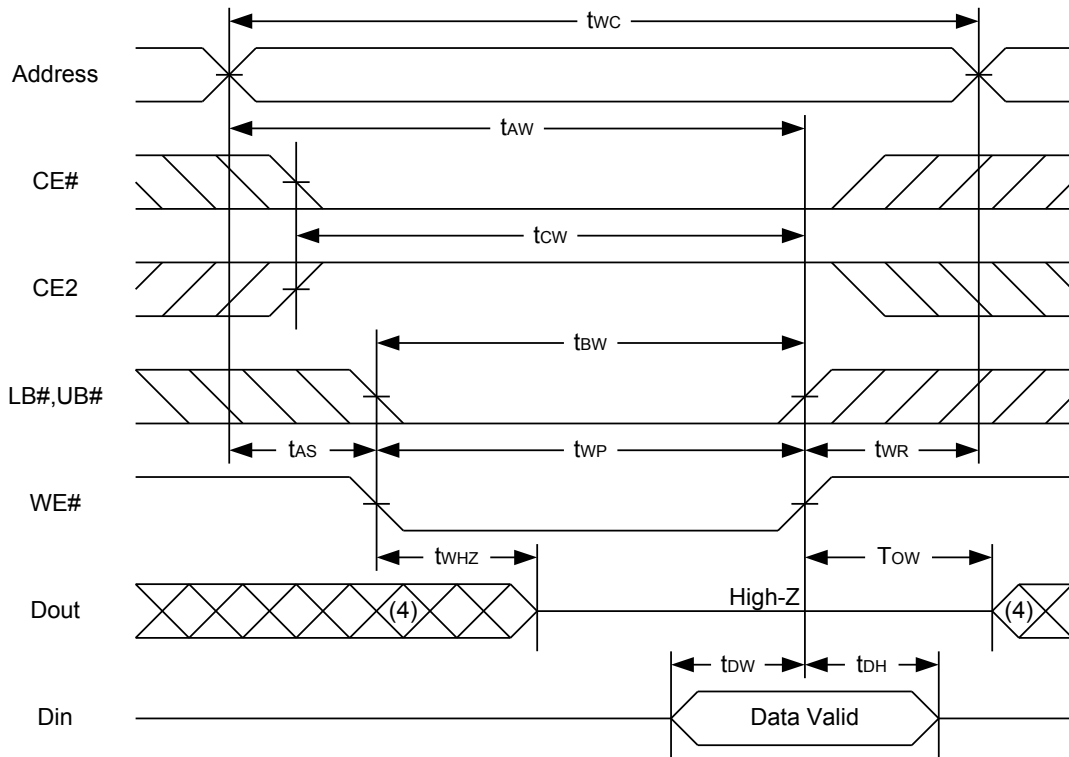
WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)
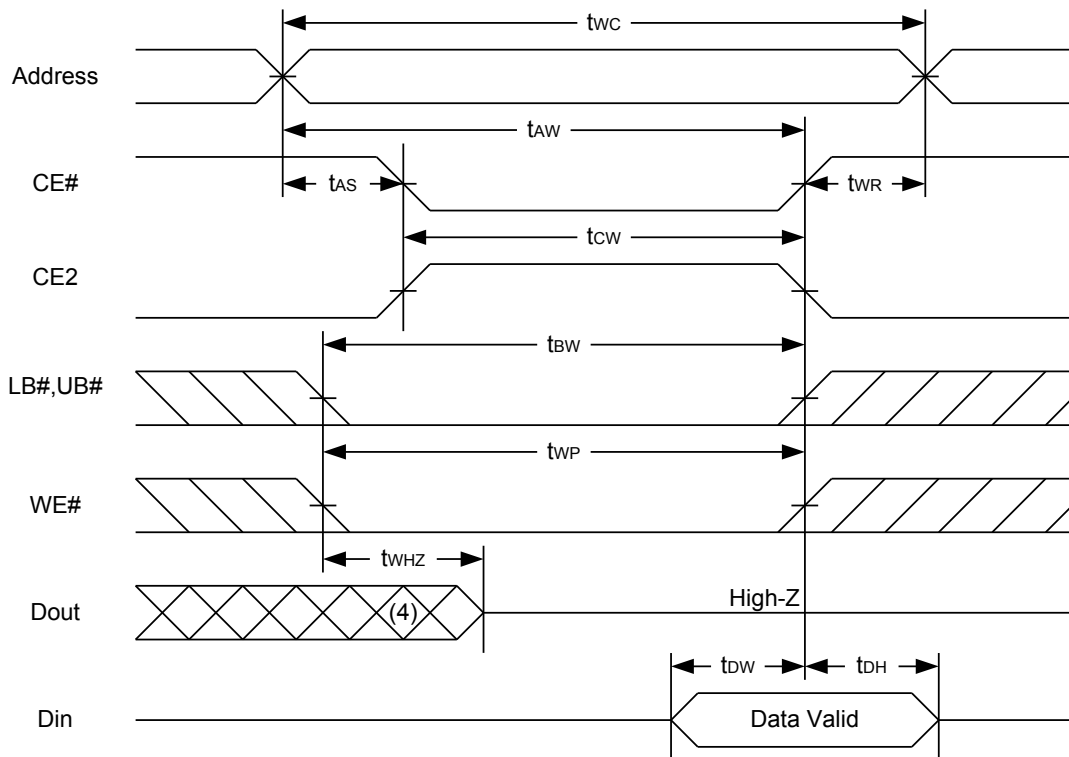
WRITE CYCLE 3 (LB#,UB# Controlled) (1,2,5,6)
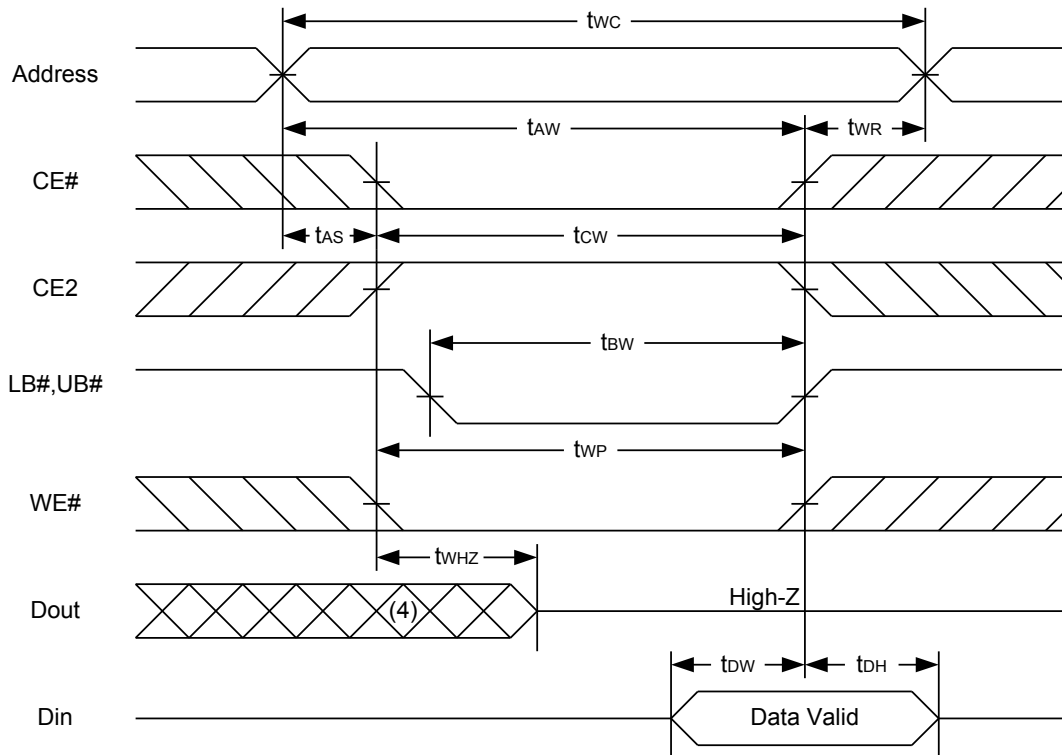
Notes :
1. WE#,CE#, LB#, UB# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.
3. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than t_{WHZ} + t_{DW} to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE#　V_{CC} - 0.2V or CE2$\leq$0.2V			1.2	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 1.2V CE#　V_{CC}-0.2V or CE2$\leq$0.2V Other pins at 0.2V or V_{CC}-0.2V	SLI	25℃	-	1	3	μA
				40℃	-	1	3	μA
					-			
			SLI		-	1	20	μA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)			0	-	-	ns
Recovery Time	t_R				t_{RC*}	-	-	ns

t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) (CE# controlled)
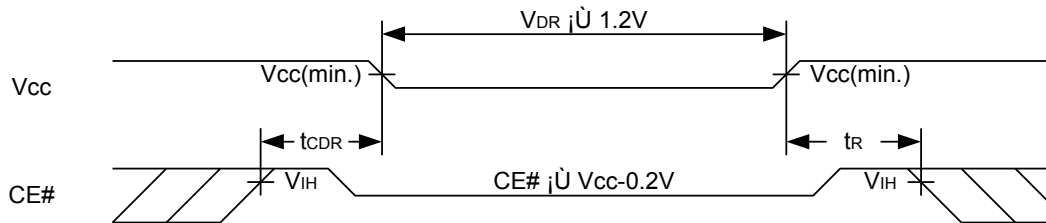
Low Vcc Data Retention Waveform (2) (CE2 controlled)
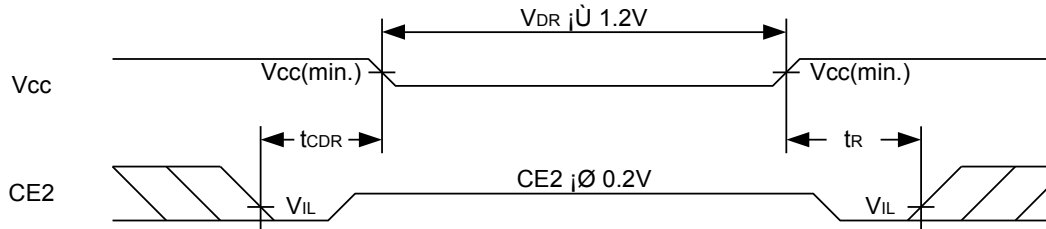
Low Vcc Data Retention Waveform (3) (LB#, UB# controlled)
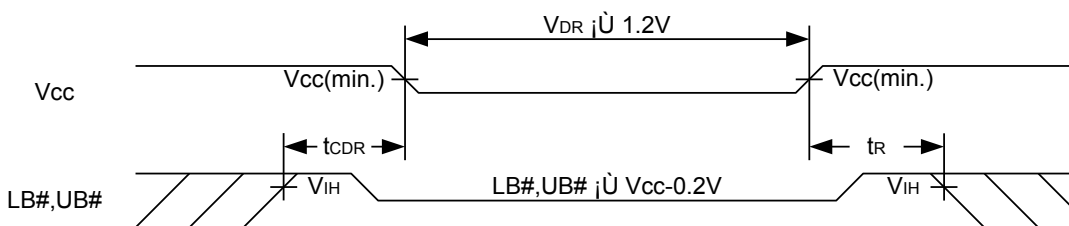
PACKAGE OUTLINE DIMENSION

48-pin 12mm x 20mm TSOP-I Package Outline Dimension
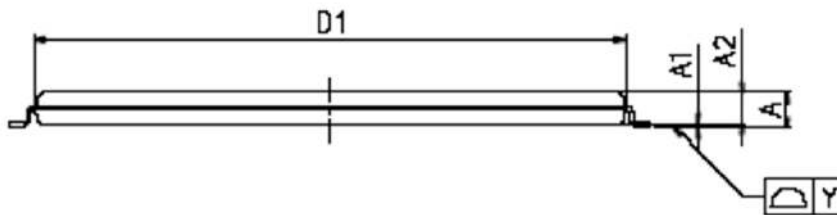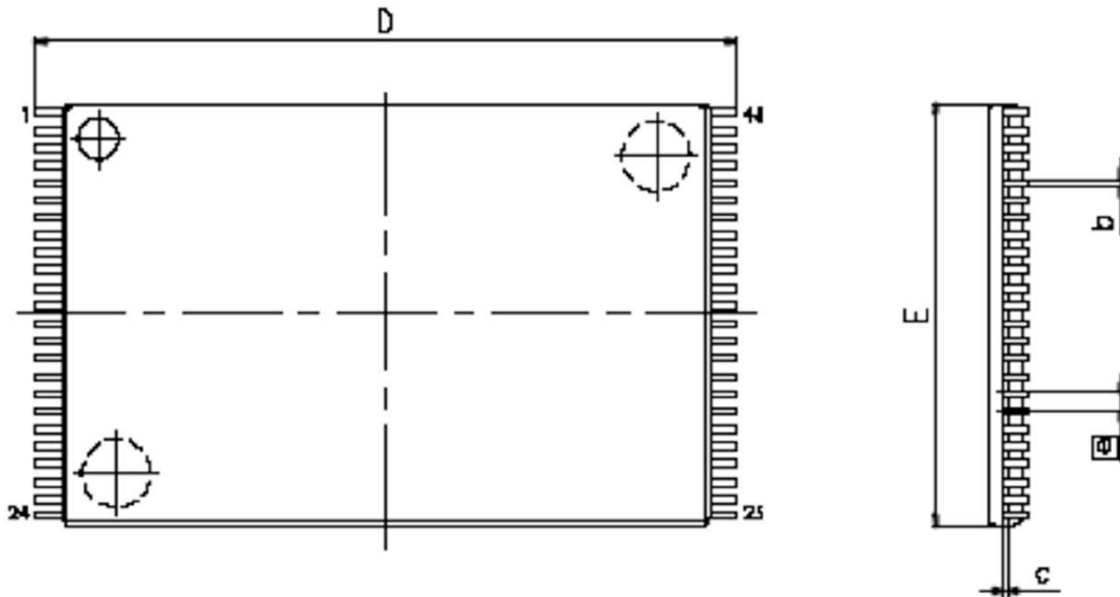
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.10	–	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
L1	–	0.80	–
Y	–	–	0.10
θ	0°	–	5°
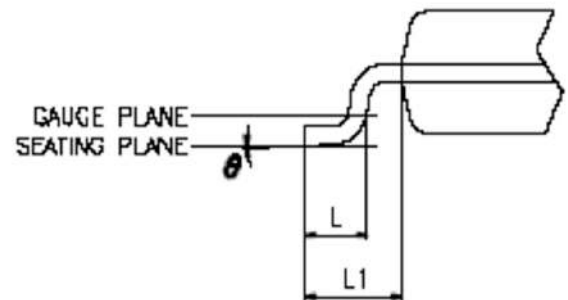
NOTES:
1. JEDEC OUTLINE : MO-142 DD
2. PROFILE TOLERANCE ZONES FOR D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

PART NUMBERING SYSTEM

AS6C	8016	55	T	I	N
SRAM	8M=512K x 16	Speed=55 ns	T = 48pin TSOP I	I=Industrial (-40°C～85°C)	Indicates Pb and Halogen Free

Alliance Memory, Inc.
511 Taylor Way,
San Carlos, CA 94070
Tel: 650-610-6800
Fax: 650-620-9211
www.alliancememory.com