



ALPHA & OMEGA
SEMICONDUCTOR

AOT11N60L/AOTF11N60L/AOTF11N60
600V, 11A N-Channel MOSFET

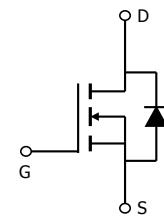
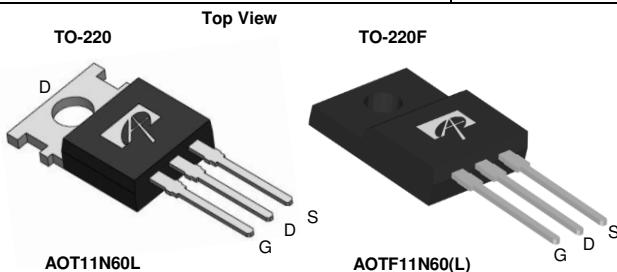
General Description

The AOT11N60L & AOTF11N60L & AOTF11N60 have been fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications. By providing low $R_{DS(on)}$, C_{iss} and C_{rss} along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.

Product Summary

V_{DS}	700V@150°C
I_D (at $V_{GS}=10V$)	11A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 0.65Ω

100% UIS Tested
100% R_g Tested



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	AOT11N60L	AOTF11N60	AOTF11N60L	Units
Drain-Source Voltage	V_{DS}		600		V
Gate-Source Voltage	V_{GS}		± 30		V
Continuous Drain Current	I_D	11	11*	11*	A
		8	8*	8*	
Pulsed Drain Current ^c	I_{DM}		39		
Avalanche Current ^c	I_{AR}		4.8		A
Repetitive avalanche energy ^c	E_{AR}		345		mJ
Single plused avalanche energy ^g	E_{AS}		690		mJ
Peak diode recovery dv/dt	dv/dt		5		V/ns
Power Dissipation ^b	P_D	272	50	37.9	W
		2.2	0.4	0.3	W/ °C
Junction and Storage Temperature Range	T_J, T_{STG}		-55 to 150		°C
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	T_L		300		°C

Thermal Characteristics

Parameter	Symbol	AOT11N60L	AOTF11N60	AOTF11N60L	Units
Maximum Junction-to-Ambient ^{a,d}	$R_{\theta JA}$	65	65	65	°C/W
Maximum Case-to-sink ^a	$R_{\theta CS}$	0.5	--	--	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	0.46	2.5	3.3	°C/W

* Drain current limited by maximum junction temperature.

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V, T _J =25°C	600			V
		I _D =250μA, V _{GS} =0V, T _J =150°C		700		
BV _{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I _D =250μA, V _{GS} =0V		0.67		V/ $^\circ\text{C}$
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =600V, V _{GS} =0V		1		μA
		V _{DS} =480V, T _J =125°C		10		
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±30V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =5V I _D =250μA	3.3	3.9	4.5	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =5.5A		0.56	0.65	Ω
g _{FS}	Forward Transconductance	V _{DS} =40V, I _D =5.5A		12		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.73	1	V
I _S	Maximum Body-Diode Continuous Current				11	A
I _{SM}	Maximum Body-Diode Pulsed Current				39	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =25V, f=1MHz	1320	1656	1990	pF
C _{oss}	Output Capacitance		100	146	195	pF
C _{rss}	Reverse Transfer Capacitance		6.5	11.2	16	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	1.7	3.5	5.3	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =480V, I _D =11A	24	30.6	37	nC
Q _{gs}	Gate Source Charge			9.6		nC
Q _{gd}	Gate Drain Charge			9.6		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =300V, I _D =11A, R _G =25Ω		39		ns
t _r	Turn-On Rise Time			58		ns
t _{D(off)}	Turn-Off DelayTime			92		ns
t _f	Turn-Off Fall Time			42		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =11A, dI/dt=100A/μs, V _{DS} =100V	400	500	600	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =11A, dI/dt=100A/μs, V _{DS} =100V	4.7	5.9	7.1	μC

A. The value of R_{WA} is measured with the device in a still air environment with T_A=25° C.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{WA} is the sum of the thermal impedance from junction to case R_{WC} and case to ambient.

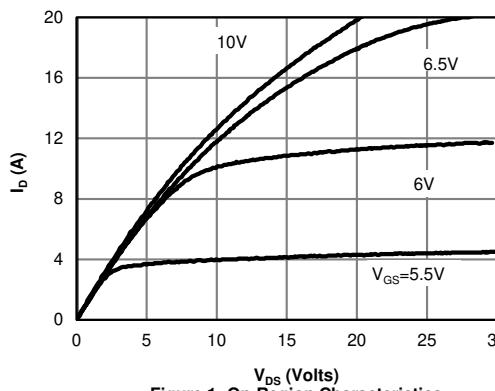
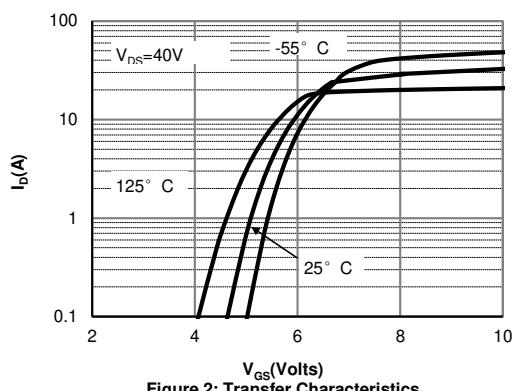
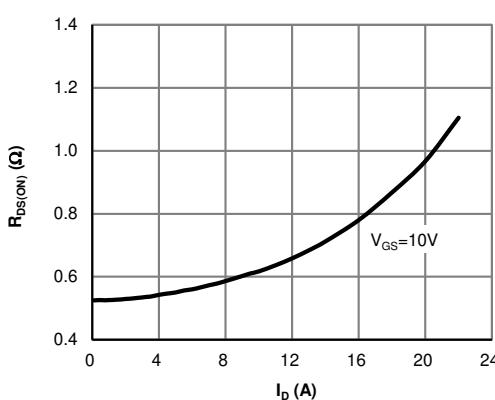
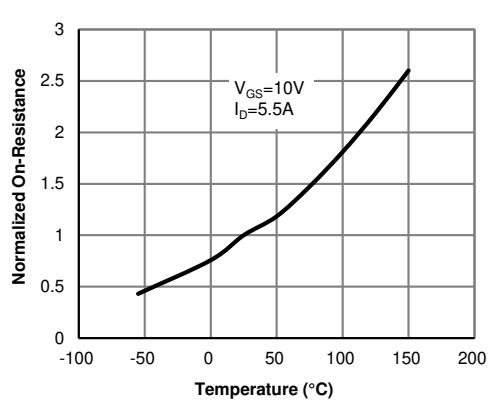
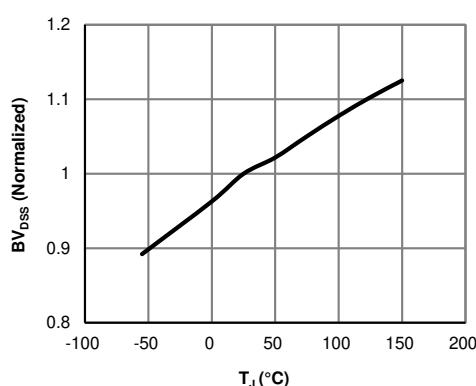
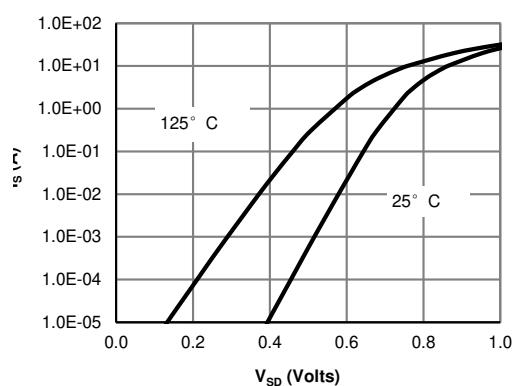
E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

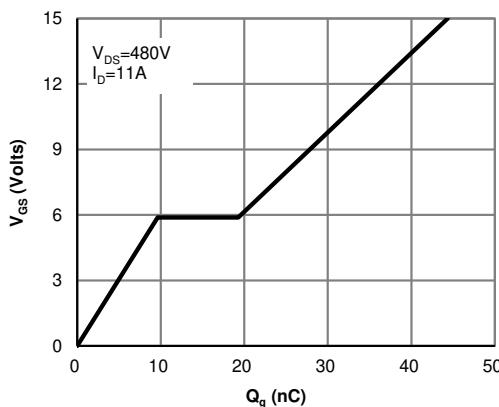
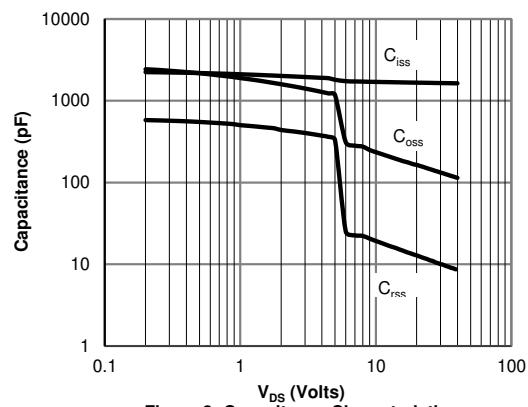
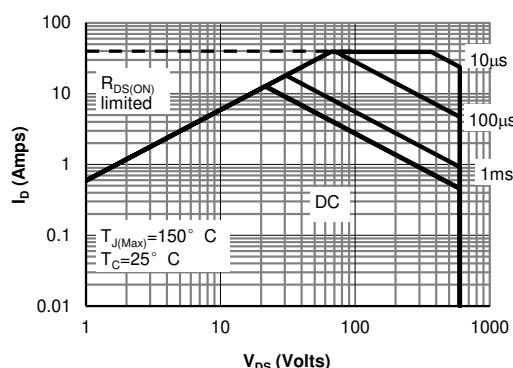
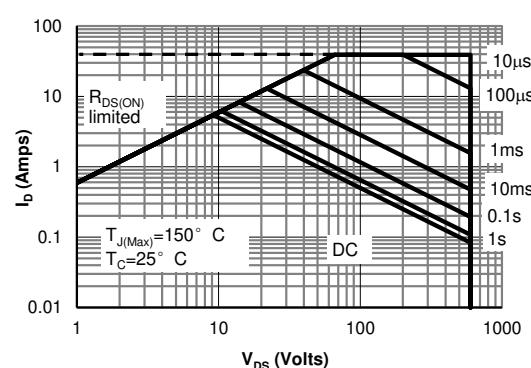
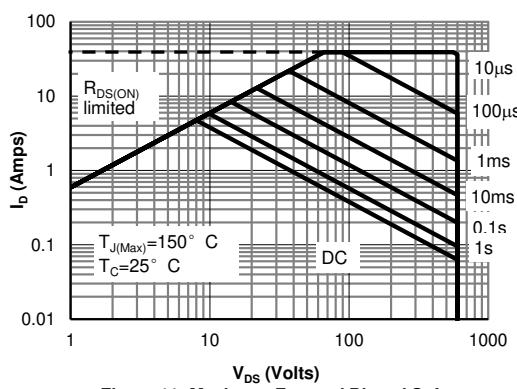
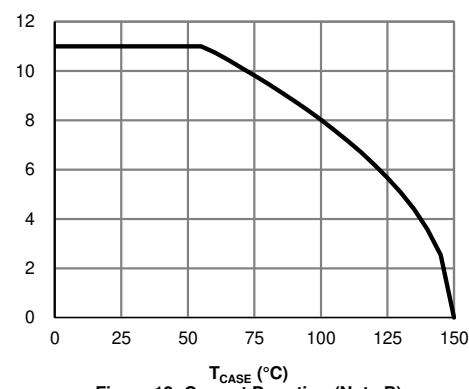
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. L=60mH, I_{AS}=4.8A, V_{DD}=150V, R_G=25Ω, Starting T_J=25° C

APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO MAKE CHANGES TO PRODUCT SPECIFICATIONS WITHOUT NOTICE. IT IS THE RESPONSIBILITY OF THE CUSTOMER TO EVALUATE SUITABILITY OF THE PRODUCT FOR THEIR INTENDED APPLICATION. CUSTOMER SHALL COMPLY WITH APPLICABLE LEGAL REQUIREMENTS, INCLUDING ALL APPLICABLE EXPORT CONTROL RULES, REGULATIONS AND LIMITATIONS.

AOS' products are provided subject to AOS' terms and conditions of sale which are set forth at:
http://www.aosmd.com/terms_and_conditions_of_sale

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 1: On-Region Characteristics

Figure 2: Transfer Characteristics

Figure 3: On-Resistance vs. Drain Current and Gate Voltage

Figure 4: On-Resistance vs. Junction Temperature

Figure 5: Break Down vs. Junction Temperature

Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 7: Gate-Charge Characteristics

Figure 8: Capacitance Characteristics

Figure 9: Maximum Forward Biased Safe Operating Area for AOT11N60 (Note F)

Figure 10: Maximum Forward Biased Safe Operating Area for AOTF11N60 (Note F)

Figure 11: Maximum Forward Biased Safe Operating Area for AOTF11N60L (Note F)

Figure 12: Current De-rating (Note B)

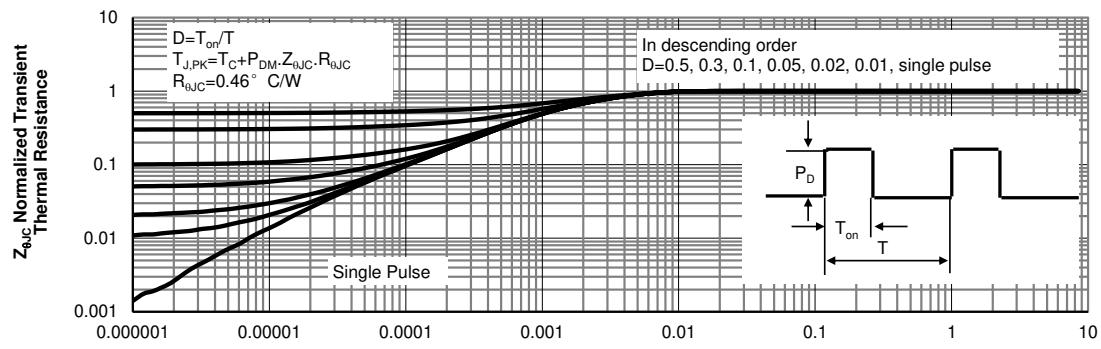
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS


Figure 13: Normalized Maximum Transient Thermal Impedance for AOT11N60 (Note F)

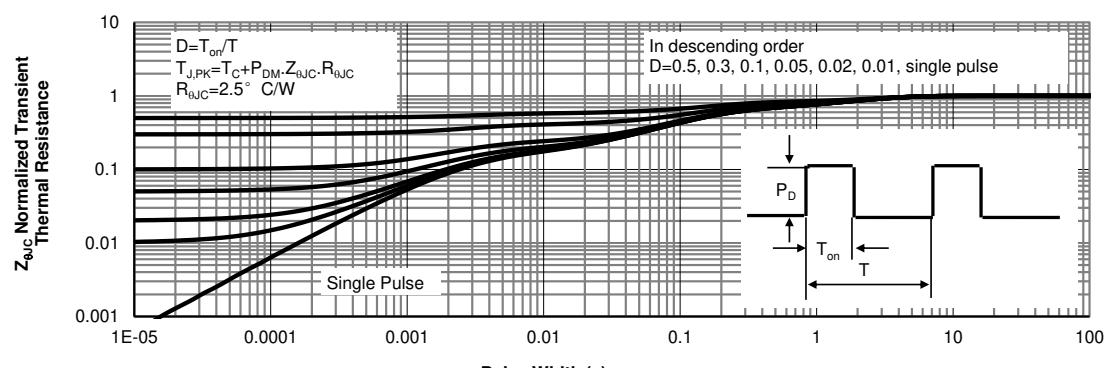


Figure 14: Normalized Maximum Transient Thermal Impedance for AOTF11N60 (Note F)

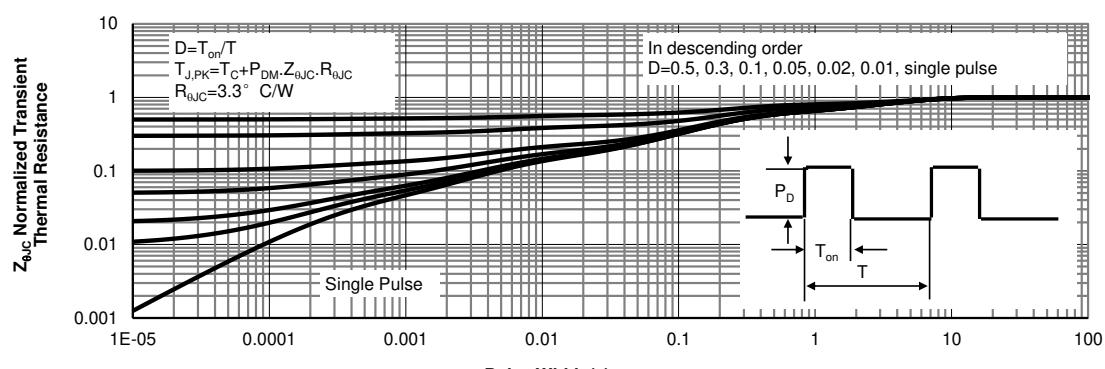
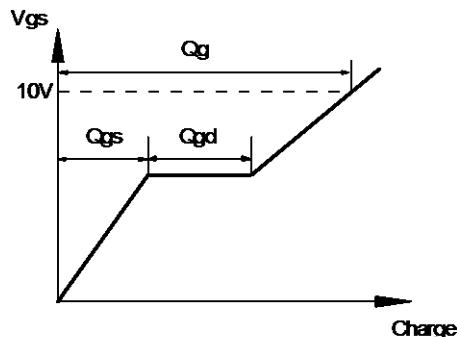
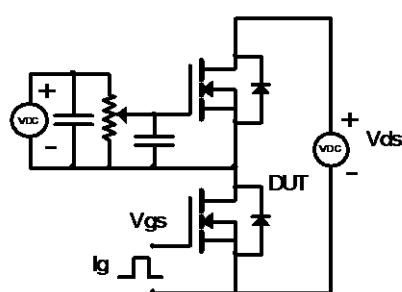
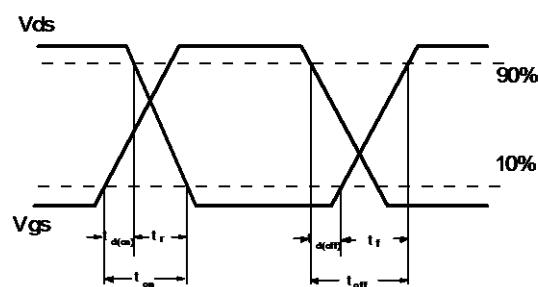
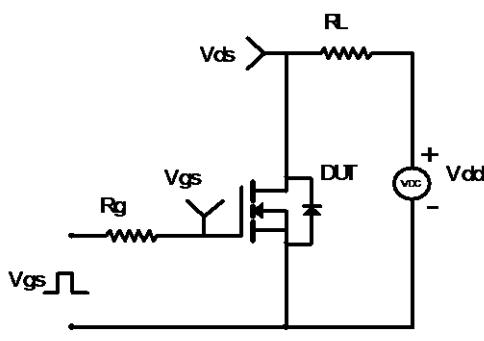
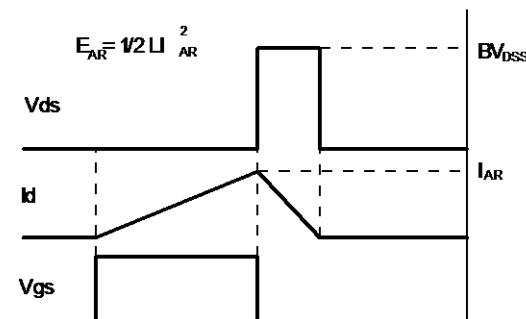
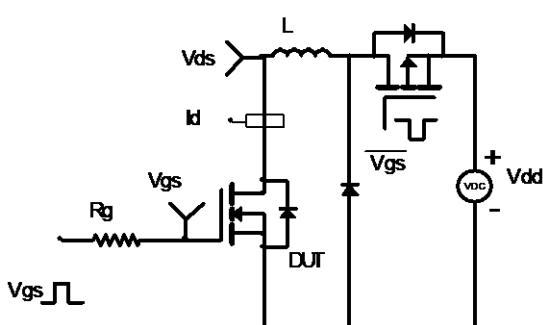


Figure 15: Normalized Maximum Transient Thermal Impedance for AOTF11N60L (Note F)

Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

Diode Recovery Test Circuit & Waveforms
