THS789 Quad-Channel Time Measurement Unit (TMU)

1 Features

- Four Event Channels + Sync Channel
- Single-Shot Accuracy: 800 ps
- Precision: 100 ps
- Result Interface Range: –7 to 7 s
- Event Input Rate: 200 MHz
- High-Speed Serial Host-Processor Bus Interface: 50 MHz
- High-Speed LVDS-Compatible Serial-Result Bus per Channel
- Temperature Sensor
- Single 3.3-V Supply

2 Applications

- Automatic Test Equipment
- Benchtop Time-Measurement Equipment
- Radar and Sonar
- Medical Imaging
- Mass Spectroscopy
- Nuclear and Particle Physics
- Laser Distance Measurement
- Ultrasonic Flow Measurement

3 Description

The THS789 device is a version of the THS788 with a reduced number of features.

The THS789 is a four-channel timing measurement unit (TMU) that incorporates a time-to-digital converter (TDC) architecture for fast and accurate measurements. The TMU can provide less than 800 ps of single-shot accuracy. The TDC has 13 ps resolution (LSB), which is derived from an external master clock of 200 MHz. It uses fast LVDS-compatible interfaces for all of its event inputs and serial result outputs, which allows for fast and reliable data transfer. Each channel can process timestamps at a maximum speed of 200 MSPS.

The THS789 has a 40-bit serial-result interface that is operated at 300 MHz using single data rate clocking. The event channels can be programmed to take timestamps on rising edges or falling edges. Host programming is achieved through a 50-MHz LVCMOS interface.

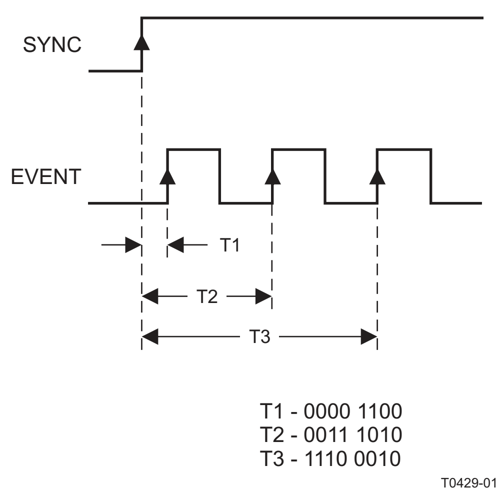
The THS789 is available in a HTQFP-100 with a heat slug on top for easy heat-sink access. The device is built using TI's RF SiGe process technology, which allows for maximum timing accuracy with low power.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THS789	HTQFP (100)	14.00 mm × 14.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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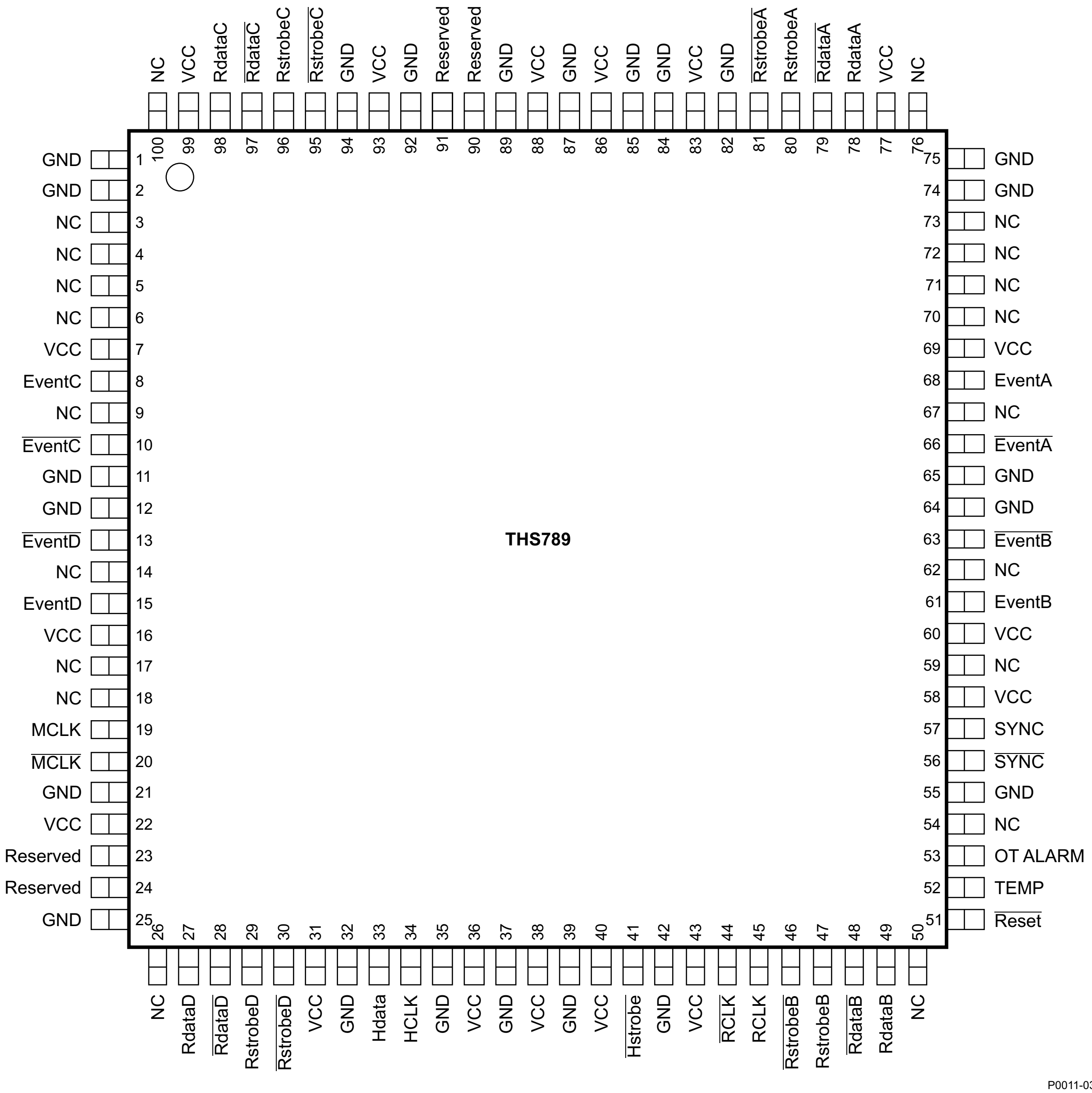
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2012) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed *Thermal Information* table	5
• Updated decoupling capacitor values in Figure 16	32

5 Pin Configuration and Functions

**PFD Package
100-Pin HTQFP
(Top View)**



Note: Pin 1 indicator is symbolized with a white dot, and is located near pin 1 corner.

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EventA	68	LVDS-compatible input	Positive event input for channel A
$\overline{\text{EventA}}$	66	LVDS-compatible input	Negative event input for channel A
EventB	61	LVDS-compatible input	Positive event input for channel B
$\overline{\text{EventB}}$	63	LVDS-compatible input	Negative event input for channel B
EventC	8	LVDS-compatible input	Positive event input for channel C
$\overline{\text{EventC}}$	10	LVDS-compatible input	Negative event input for channel C
EventD	15	LVDS-compatible input	Positive event input for channel D
$\overline{\text{EventD}}$	13	LVDS-compatible input	Negative event input for channel D
GND	1, 2, 11, 12, 21, 25, 32, 35, 37, 39, 42, 55, 64, 65, 74, 75, 82, 84, 85, 87, 89, 92, 94	Ground	Chip ground
HCLK	34	LVCMOS input	Host serial-interface clock
Hdata	33	LVCMOS I/O	Host serial-interface data I/O
$\overline{\text{Hstrobe}}$	41	LVCMOS input	Host serial-interface chip select
MCLK	19	LVDS-compatible input	Positive master-clock input
$\overline{\text{MCLK}}$	20	LVDS-compatible input	Negative master-clock input
NC	3–6, 9, 14, 17, 18, 26, 50, 54, 59, 62, 67, 70–73, 76, 100	No connect	Physically not connected to silicon
OT_ALARM	53	Open-drain output	Overtemperature alarm
RCLK	45	LVDS-compatible output	Positive result-interface clock
$\overline{\text{RCLK}}$	44	LVDS-compatible output	Negative result-interface clock
RdataA	78	LVDS-compatible output	Positive result-data output for channel A
$\overline{\text{RdataA}}$	79	LVDS-compatible output	Negative result-data output for channel A
RdataB	49	LVDS-compatible output	Positive result-data output for channel B
$\overline{\text{RdataB}}$	48	LVDS-compatible output	Negative result-data output for channel B
RdataC	98	LVDS-compatible output	Positive result-data output for channel C
$\overline{\text{RdataC}}$	97	LVDS-compatible output	Negative result-data output for channel C
RdataD	27	LVDS-compatible output	Positive result-data output for channel D
$\overline{\text{RdataD}}$	28	LVDS-compatible output	Negative result-data output for channel D
Reserved	23, 24, 90, 91	Engineering or test pins	Connect to VCC
$\overline{\text{Reset}}$	51	LVCMOS input	Chip reset, active-low
RstrobeA	80	LVDS-compatible output	Positive strobe signal for channel A
$\overline{\text{RstrobeA}}$	81	LVDS-compatible output	Negative strobe signal for channel A
RstrobeB	47	LVDS-compatible output	Positive strobe signal for channel B
$\overline{\text{RstrobeB}}$	46	LVDS-compatible output	Negative strobe signal for channel B
RstrobeC	96	LVDS-compatible output	Positive strobe signal for channel C
$\overline{\text{RstrobeC}}$	95	LVDS-compatible output	Negative strobe signal for channel C
RstrobeD	29	LVDS-compatible output	Positive strobe signal for channel D
$\overline{\text{RstrobeD}}$	30	LVDS-compatible output	Negative strobe signal for channel D
SYNC	57	LVDS-compatible input	Positive input for sync channel
$\overline{\text{SYNC}}$	56	LVDS-compatible input	Negative input for sync channel
TEMP	52	Analog output	Die temperature
VCC	7, 16, 22, 31, 36, 38, 40, 43, 58, 60, 69, 77, 83, 86, 88, 93, 99	Power supply	Positive supply, nominal 3.3 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}		4		V
	Analog I/O to GND[1]	–0.3	V_{CC} + 0.3	V
	Digital I/O to GND	–0.3	V_{CC} + 0.3	V
T_J	Maximum junction temperature[2]		150	°C
T_{stg}	Storage temperature		150	°C

(1) LVDS outputs are not short-circuit-proof to GND.
(2) The THS789 device has an automatic power shutdown at 140°C, typical.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3.135		3.465	V
T_J	Junction temperature	0		105	°C
	MCLOCK frequency		200		MHz

6.4 Thermal Information

THERMAL METRIC[1]		THS789	UNIT
		PFD (HTQFP)	
		100 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Typical conditions are at T_J = 55°C and V_{CC} = 3.3 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TDC CHARACTERISTICS					
Time-measurement precision (LSB)			13.02		ps
Measurement accuracy after calibration, mean		–800		800	ps
Single-event accuracy, one sigma			800		ps
Time-measurement temperature coefficient			0.1		ps/°C
Time-measurement voltage coefficient			±30		ps/V
Event input rate				200	MHz
Minimum event pulse duration		250			ps
Turnon time (ready to take timestamp)				250	µs
MASTER CLOCK CHARACTERISTICS					
Frequency			200		MHz
Duty cycle		0.4		0.6	
Jitter				3	ps RMS
HIGH-SPEED LVDS INPUTS: MCLK, EVENT, SYNC					
Differential input voltage	100-Ω termination, line-to-line	200	350	500	mV
Common-mode voltage			1.25		V
Peak voltage, either input		0.6		1.7	V
Input capacitance			1		pF
HIGH-SPEED LVDS OUTPUTS: Rdata, Rstrobe, RCLK					
Differential output voltage	100-Ω termination, line-to-line	250	325	400	mV
Common-mode voltage		1.125	1.28	1.375	V
Rise time/fall time	20%/80%		250		ps
Output resistance			40		Ω
TEMPERATURE SENSOR DC CHARACTERISTICS					
Output voltage	T_J = 65°C		1.69		V
Output voltage temperature slope			5		mV/°C
Max capacitive load		30			pF
Max resistive load				10	kΩ
OVERTEMPERATURE ALARM DC CHARACTERISTICS					
Trip point	Active-low pulldown		141		°C
Leakage current	Temperature < trip point		1		µA
Output voltage, low	I_{sink} = 1 ma			0.2	V
OUTPUT INTERFACE TIMING					
RCLK duty cycle		45%	50%	55%	
Rdata/Rstrobe to RCLK setup time	300 MHz	1.4			ns
Rdata/Rstrobe to RCLK hold time	300 MHz	1.5			ns
OPERATING PARAMETERS					
Coarse counter range		34			bit
Coarse counter max time range				14.31	s
Result-interface clock				300	MHz
Result-interface transfer format			40		bit
Result-interface time range		–7.158		7.158	s

6.6 Host Serial Interface DC Characteristics

over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		0.7 × V_{CC}		V_{CC} + 0.5	V
V_{IL}	Low-level input voltage		GND – 0.3		0.3 × V_{CC}	V
V_{OH}	High-level output voltage		V_{CC} – 0.5		V_{CC} + 0.3	V
V_{OL}	Low-level output voltage		0		0.4	V
I_{lkg}	Leakage current				1	µA

6.7 Host Serial Interface AC Characteristics

over operating junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
HCLK frequency				50	MHz
Rise and fall times				3.5	ns
HCLK duty cycle		40%	50%	60%	
Hstrobe high period between two consecutive transactions		40			ns
Hstrobe low to HCLK high setup		5			ns
HCLK high to Hstrobe high hold time		5			ns
Hdata in to HCLK high setup		5			ns
Hdata in to HCLK high hold time		5			ns
HCLK falling edge to Hdata out (L or H)	C_L = 20 pF	3.25			ns
HCLK falling edge to Hdata out (H or L)	C_L = 20 pF	3.25			ns

6.8 Power Consumption

Typical conditions are at 55°C junction temperature, V_{CC} = 3.3 V.

CONDITION	TYP	MAX	UNIT
Four channel current	925	1236	mA

6.9 Typical Characteristics

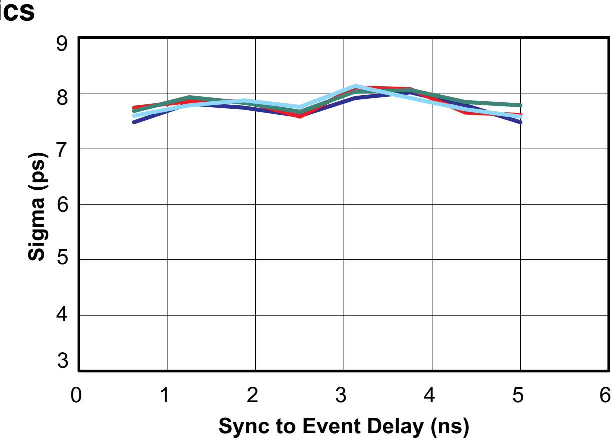


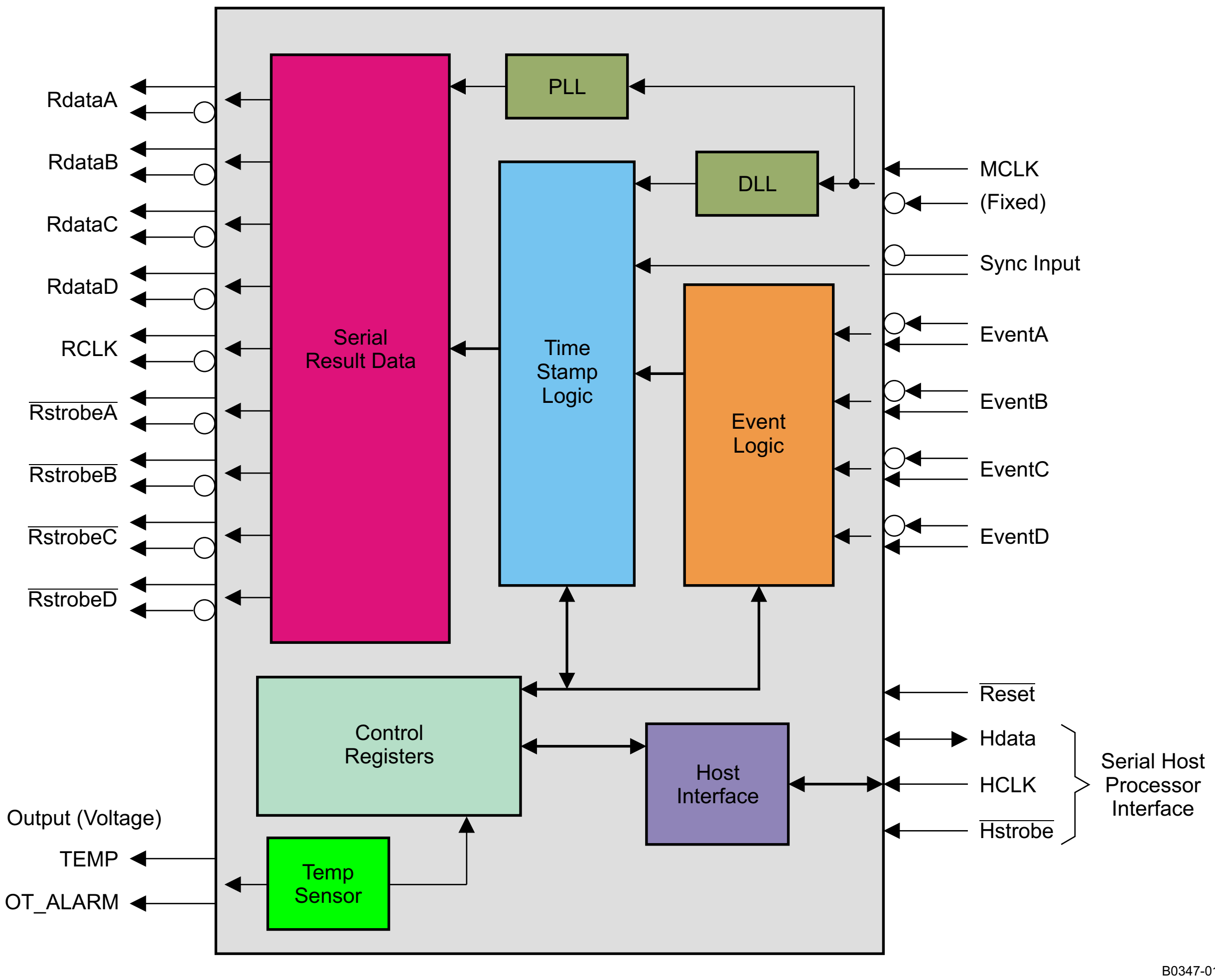
Figure 1. Typical Per Channel Sigmas vs 5-ns (200-MHz) Window

7 Detailed Description

7.1 Overview

The THS789 TMU includes four measurement channels plus a synchronization channel optimized to make high-accuracy time-interval measurements. The following is a brief description of the various circuit blocks and how they interact to make and process the time measurements.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Counter, Latches, Clock Multiplier

The center of the TMU is a master synchronous counter that counts continuously at a rate of 1.2 GHz. This is the master timing generator for the whole TMU and defines the basic timing interval of 833 ps, which is further subdivided with Interpolator circuitry. The output bits of the counter are connected to five sets of latches, which can latch and hold the counter state on command from each of the channels. In this way, when an event occurs, the counter time is recorded in the particular channel's latches. The latch output is converted to CMOS levels and passed to the respective channel's FIFO buffer, which is 15 samples deep. The counter 1.2-GHz clock is derived from the MCLK input to the TMU at 200 MHz. This MCLK input is critical to the accuracy of the TMU, and any error in frequency is reflected as errors in time measurement. Likewise, jitter propagates to the counter and other circuits and adds noise to the measurement accuracy. The 200-MHz clock is the input to a clock multiplier. The clock multiplier uses delay-lock loop (DLL) techniques and combinatorial logic to construct a six-times clock from the reference input. This 1.2-GHz clock is passed to a high-power clock buffer, which drives all the circuitry in the master counter and many other circuits in the TMU.

7.3.2 Channels, Interpolator

There are four event channels and one sync channel. The event channels are identical, and the sync channel contains most of the event channel circuitry, but without a FIFO. An input pulse to the sync channel serves as the reference time zero for the TMU. An event input to a channel is compared to the sync time reference, and the time delay is calculated as the time difference modified by a calibration value. An event input follows the following signal path: the event input edge sets a fast latch (hit latch). The output of the latch is current-buffered and applied to the interpolator. The interpolator uses DLL techniques to subdivide the counter interval of 833 ps into 64 time intervals of 13 ps each. A large array of fast latches triggered by the hit latch captures the state of the 64 time intervals and logically determines 6 bits of timing data based on where the event occurred in the 833-ps clock interval. These 6 bits are latched and eventually passed to the FIFO, where they become the LSBs of the time-to-data conversion. A synchronizer circuit is also connected to the 64-latch array and removes the possible timing ambiguity between the 64 latches and the master counter. This takes a few 1.2-GHz clock pulses. When this process is complete, a pulse occurs which captures the master counter bits into the channel latches. A subsequent pulse loads all the bits from the interpolator and the counter into the channel FIFO. While this is happening, the hit latch is being reset, and the channel is prepared to accept another event edge. This process is fast enough to accept and measure event edges as close together as 5 ns.

7.3.3 FIFO

Each event channel contains a 15-deep, 40-bit-wide FIFO, which allows for rapid accepting and measurement of event inputs and a user-defined data-output rate of those measurements.

7.3.4 Calibration, ALU, Tag, Shifter

The output of the FIFO is controlled by the shifter, which is a free-running parallel-to-serial register. The shifter generates a load pulse, which transfers the data in the FIFO output into an arithmetic logic unit, which does the sync time and calibration time subtractions and then parallel-loads the result into the output serial register. An LVDS output buffer outputs the clock, data, and strobe signals to transfer the time-measurement data to the user. A TAG bit is appended to the leading edge of the data word. Currently the TAG feature is not implemented. The bit will always be 0 representing data.

7.3.5 Serial Interface, Temperature, Overhead

The TMU functions and options are controlled and read out by a serial interface built in CMOS logic that can operate up to 50 MB/s. There is one central controller which then drives registers, counters, and so on, in each channel. A temperature sensor is located central to the chip and outputs a voltage proportional to the chip temperature. If the chip temperature rises above 141°C, the TMU powers down and outputs an overtemperature alarm signal. The TMU does not restart without a command through the serial interface. A bias circuit provides a regulated current bias and voltage reference for the TMU. The serial controller sequences some of the bias circuits to account for some acquisition times, and thereby, turns on the TMU.

7.4 Device Functional Modes

7.4.1 Serial-Results Interface

The TMU captures time-stamp results and sends them to external logic using an LVDS serial-results port. The serial-results port consists of a clock signal (RCLK), four strobe signals (Rstrobex) and four data signals (Rdatax). The Rstrobex signal indicates that a time-stamp data transfer is about to begin for the corresponding channel.

Table 1 shows the results transfer format and time range.

Table 1. Result Transfer Format and Time Range

RESULT TRANSFER FORMAT	TIME RANGE
40 bits	–7.158 s to 7.158 s

7.4.2 Resister Map Descriptions for All Channels and Central Register

Table 2. Control and Status Register Descriptions for All Channels

Register	Bit	Name	Function	LogicState	Description
00h 20h 40h 60h	0	En_ChX	Enable or disable channel X by powering down the channel. Time to enable a channel is 200 µs.	0	Channel is disabled
				1	Channel is enabled
	1	ChX_IP_EN	Enables or disables the input of channel X. Events are prevented from entering a channel.	0	Input is disabled
				1	Input is enabled
	2	Pol_X	Defines the polarity of the event inputX for the upcoming timestamp generation.	0	Positive edge
				1	Negative edge

Table 3. Control and Status Register Descriptions for All Channels

Register	Bit	Name	Function	Logic State	Description
01h 21h 41h 61h	0	Reserved	Reserved	x	
	1	Unused	Unused	x	
	2	Unused	Unused	x	
	3	Unused	Unused	x	
	4	Unused	Unused	x	
	5	Reserved	Reserved	0	
04h 24h 44h 64h	0	DLL_Lock_X	Indicates the DLL lock status for channel X.	0	DLL locked
				1	DLL not locked
	2	Reserved	Reserved	x	
	3	FIFO_Full_X	Indicates that the FIFO is full. Timestamps arriving while FIFO is full are lost.	0	FIFO not full
				1	FIFO full
	4	FIFO_Empty_X	Indicates that the FIFO is empty.	0	FIFO not empty
				1	FIFO empty

Table 4. Central Control and Status Registers Description

Register	Bit	Name	Function	Logic State	Description
80h	0	TEST_En	Enables or disables factory test routines.	0	Disabled
				1	Enabled
	1	RESET	Reset the device. Device is fully operational after 250 µs.	0	
				1	Reset
	2	Reserved	Reserved	0	
	3	Reserved	Reserved	0	
	4	Reserved	Reserved	0	
	5	Reserved	Reserved	0	
	6	Reserved	Reserved	0	
	7	Reserved	Reserved	1	
	8	Reserved	Reserved	0	
	9	Reserved	Reserved	1	
	10	OT_En	Enables or disables the over temperature alarm circuits.	0	Disabled
				1	Enabled
	11	RST_OT_ALM	Resets the temperature alarm.	0	
				1	Reset alarm state
	12	SYNC_TS_Pol	Defines the polarity of the Sync input for the upcoming timestamp generation.	0	Positive edge
				1	Negative edge
	13	SYNC_IP_ENI	Enables or disables the sync channel	0	Sync disabled
				1	Sync enabled
	14	PWR_DN	Powers down the device	0	Powered up
				1	Powered down
	15	RCLK_En	Enables RCLK	0	Disabled
				1	Enabled
81h	1	Reserved	Reserved	1	N/A
	2	Reserved	Reserved	1	N/A
	3	Quiet_Mod	It disables the RCLK and digital clks internal during timestamp process. Allows for only 16 timestamps.	0	Normal mode
				1	Quiet mode
82h	0	TMU_Ready	Indicates that the internal clks, coarse counter and Sync channel are operational.	0	Device is not ready
				1	Device is ready
	1	OT_ALM	Over temperature alarm. Indicates that the junction temperature is 140°C.	0	No alarm
				1	Alarm is enabled
	2	DLL_Lock_Sync	Indicates the Sync channel DLL lock status.	0	DLL is locked
				1	DLL is not locked
	3	DLL_Lock_1G2	Indicates the lock status of the 1.2-GHz internal clock.	0	DLL is locked
				1	DLL is not locked

7.5 Programming

7.5.1 Host Processor Bus Interface

The THS789 device includes a high-speed serial interface to a host processor. The host interface is used for writing or reading registers that reside in the TMU chip. These registers allow configuration of the device functions. All registers are capable of both read and write operations unless otherwise stated.

7.5.1.1 Serial Interface

The TMU serial interface operates at speeds of up to 50 MHz. Register addresses are 8 bits long. Data words are 16 bits wide, enabling more-efficient interface transactions. The serial bus implementation uses three LVCMOS signals: HCLK, $\overline{\text{Hstrobe}}$, and Hdata. The HCLK and $\overline{\text{Hstrobe}}$ signals are inputs only, and the Hdata signal is bidirectional. The HCLK signal is not required to run continuously. Thus, the host processor may disable the clock by setting it to a low state after the completion of any required register accesses.

When data is transferred into the device, Hdata is configured as an input bus, and data is latched on a rising edge of HCLK. When data is transferred out of the part, Hdata is configured as an output bus, and data is updated on the falling edge of HCLK. $\overline{\text{Hstrobe}}$ is the control signal that identifies the beginning of a host bus transaction. $\overline{\text{Hstrobe}}$ must remain low for the duration of the transaction, and must go high for at least two clock cycles before another transaction can begin.

7.5.1.2 Read vs Write Cycle

The first Hdata bit latched by HCLK in a transaction identifies the transaction type.
First Hdata bit = 1 for read; data flows out of the chip.
First Hdata bit = 0 for write; data flows into the chip.

7.5.1.3 Parallel (Broadcast) Write

Parallel write is a means of allowing identical data to be transferred to more than one channel in one transaction. The second Hdata bit of a transaction indicates whether a parallel write occurs.
Second Hdata bit = 0; data goes to the selected channel.
Second Hdata bit = 1; data goes to all four channels.

7.5.1.4 Address

After the R/$\overline{\text{W}}$ bit and the parallel write bit, the following 8 bits on the Hdata line contain the source address of the data word for a read cycle or the destination address of the data word for a write cycle. Address bits are shifted in MSB first, LSB last.
Third HCLK – Address Bit 7 (MSB)
Tenth HCLK – Address Bit 0 (LSB)

7.5.1.5 Data

The data stream is 16 bits long, and it is loaded or read back MSB first, LSB last. The timing for read and write cycles is different, as the drivers on Hdata alternate between going into high-impedance and driving the line.

7.5.1.6 Reset

$\overline{\text{Reset}}$ is an external hardware signal that places all internal registers and control lines into their default states. The THS789 device resets after a power-up sequence (POR). Hardware reset is an LVCMOS active-low signal and is required to stay low for approximately 100 ns.

$\overline{\text{Reset}}$ places the TMU in a predetermined idle state at power on, and anytime the system software initializes the system hardware. In the idle state, the TMU ignores state changes on the Event inputs and never creates timestamps. The TMU is capable of switching within 250 μs from the idle state to a state that creates accurate timestamps.

Programming (continued)

7.5.1.7 Chip ID

Address (83h) is a read-only register that identifies the product and the die revision. The 16-bit register is divided into two 8-bit sections. The LSB represents the revision history and the MSB represents the last two digits of THS789 device (that is, 80). The first revision (1.0) is as follows:

1000 0000 0001.0000

7.5.1.8 Read Operations

Reading the THS789 device registers via the host interface requires the following sequence:

The host controller initiates a read cycle by setting the host strobe signal, $\overline{\text{Hstrobe}}$, to a low state. The serial Hdata sequence starts with a high R/$\overline{\text{W}}$ bit, followed by (either 1 or 0) for parallel-write bit and 8 bits of address, with most-significant bit (A7) first. The host controller should put the Hdata signal in the high-impedance state beginning at the falling edge of HCLK pulse 10. The THS789 device allows one clock cycle, (r0) for the host to reverse the data-channel direction and begins driving the Hdata line on the falling edge of HCLK pulse 11. The data is read beginning with the most-significant bit (D15) and ending with the least-significant bit (D0).

The host must drive Hstrobe to a high state for a minimum of two HCLK periods beginning at the falling edge of HCLK pulse 27 to indicate the completion of the read cycle. Figure 2 shows the timing diagram of the read operation.

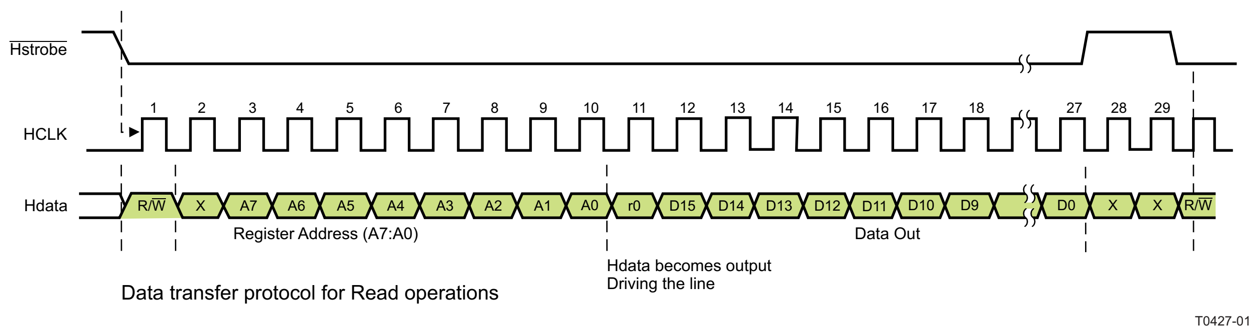


Figure 2. Read Operation

7.5.1.9 Write Operations

Writing into the THS789 device registers via the host interface requires the following sequence:

After the $\overline{\text{Hstrobe}}$ line is pulled low (start condition), the R/$\overline{\text{W}}$ bit is set low, followed by a 0 for the parallel-write bit (single-register write), then the memory address (A7–A0) followed by the data (D15:D0) to be programmed. The next clock cycle (w) is required to allow data to be latched and stored at the destination address (or addresses in the case of a parallel write), followed by at least two dummy clock cycles during which the $\overline{\text{Hstrobe}}$ is high, indicating the completion of the write cycle. Figure 3 and Figure 3 show timing diagrams of write operations.

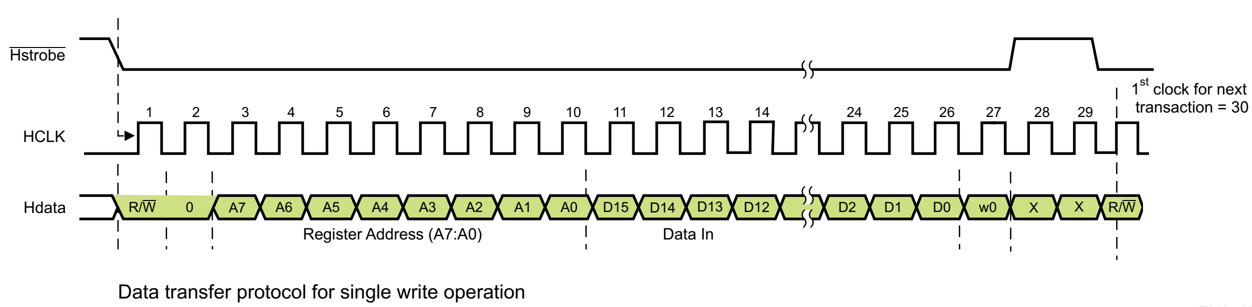


Figure 3. Write Operation

Programming (continued)

7.5.1.10 Write Operations to Multiple Destinations

This is similar to the single-write operation except the parallel-load bit is set to 1.

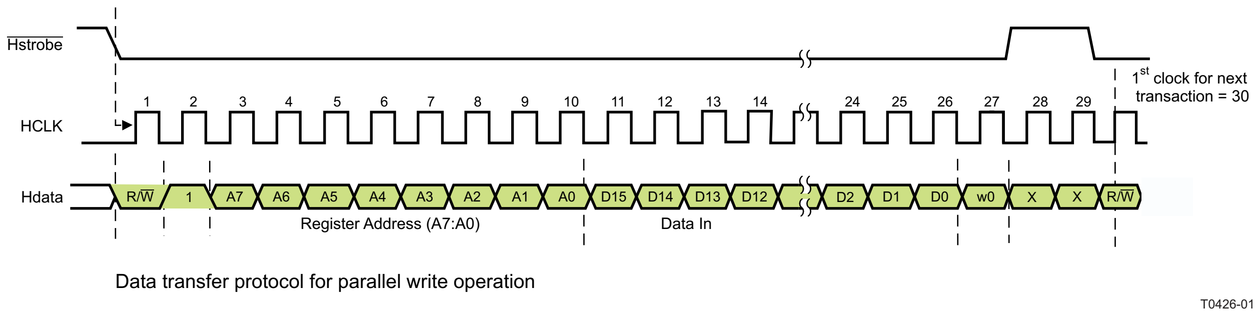


Figure 4. Write Operations to Multiple Destinations

7.5.2 Serial-Results Interface and ALU

7.5.2.1 Event Latches

A selectable rising or falling edge of an event pulse sets the latch. The latch remains set until the interpolator has finished processing the event, at which time the interpolator resets the latch. The latch, however, does not accept another event pulse until the event input returns to its initial state and remains for the initial event-pulse duration. Any event transitions which occur before the interpolator has completed processing the previous event are ignored. For example, assume that *rising edge* is selected. Two rising edges can occur as quickly as 5 ns apart. The falling edge can occur anywhere from 250 ps after the rising edge to 250 ps before the next rising edge. Any other edges or glitches are ignored.

7.5.2.2 FIFO

Timestamps are written to a FIFO at high speed and read for further processing at a lower speed before being sent to the result interface. This FIFO is 15 bits deep and 40 bits wide. There are four FIFOs in THS789 device, one for each channel. There are two status registers (FIFO_Full_x and FIFO_Empty_x), which are set when a FIFO reaches its full capacity and when it is empty, respectively.

Timestamps are taken and loaded into the FIFO as events occur. Timestamps are mathematically processed by an arithmetic logic unit (ALU) which calculates the difference between the event and the sync timestamps and factors in the appropriate calibration value from the calibration register. The ALU operates on the data as it is read out of the FIFO and sent out through the serial-results interface. The serial-results interface controls the output of the FIFO.

7.5.2.3 Result-Interface Operation

The TMU initiates a read cycle by setting the strobe signal, $\overline{\text{Rstrobe}}$, to a low state, indicating that the data transfer is about to begin. The serial Rdata sequence starts with a TAG bit, followed by the 40-bit data (R0 to R39). R39 (MSB) is the sign bit. Following the last data bit (R39), the strobe signal ($\overline{\text{Rstrobe}}$) goes high for two clock cycles, indicating the end of the transaction.

The data is clocked out of the TMU on the rising edge of RCLK. The receiving device clocks the data in on the rising edge of RCLK. Figure 5 shows a 40-bit result on the result interface.

Programming (continued)

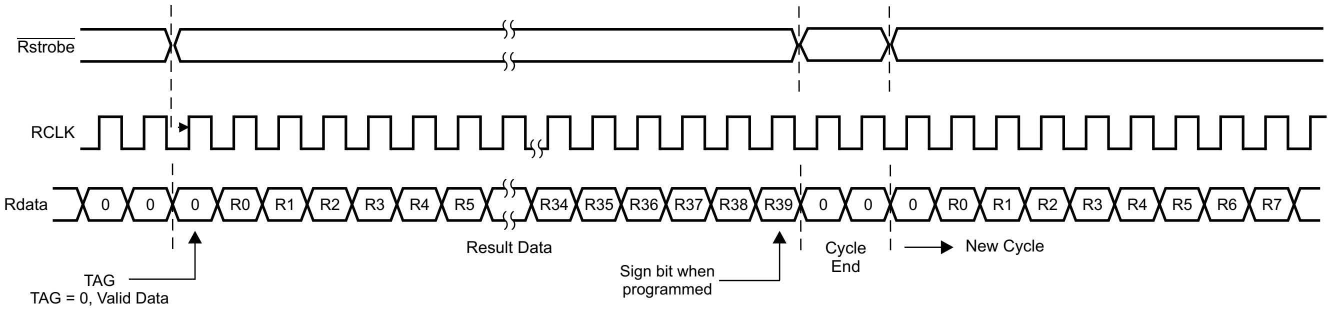


Figure 5. Result-Interface Operation A

NOTE

In Figure 5, only RCLK_P is drawn to indicate the correct edge with respect to data.

NOTE

The THS788/789 TMU generates a result data ready strobe signal (RSTROBEx). RSTROBEx asserts when data is driven out from the serial shift register in channel x. Where x represents channel A,B,C, or D. The RSTROBEx signals intended to drive active low differential signal indicating start and completion of data on the RDATAx serial output. There are some circumstances that cause the RSTROBEx signal to deassert one RCLK cycle early. This behavior remains consistent for each channel after powerup or a reset.

To workaround this potential issue, it is recommended to use leading edge of RSTROBEx assertion, and capture the correct number of results bits independent of the deassertion of RSTROBEx.

7.5.2.4 Serial Results Latency

The event stored in the FIFO will be transferred to ALU and subsequently to the free running results data shift register when the shift register enters a load pulse. The load pulse is generated once per ALU/shift register processing cycle. The load pulse will trigger the ALU and transfer result to the parallel to serial shift register for output. The cycle time of the load pulse is dependent upon the depth of the result transfer register and data rate. Because the results parallel to serial register are free running, the load pulse will be asynchronous to the actual event. So, the latency will depend upon where in the current cycle the load pulse occurred relative to the event being captured into the FIFO.

The worst case for data to be output from serial bus:

$$T_{event} + 5(R_{clkcycles}) + (R_{datalength} + 3) \text{ x } R_{clkcycles} + (R_{datalength} + 3) \times R_{clkcycles} \quad (1)$$

The best case for data to be output from serial bus:

$$T_{event} + 5(R_{clkcycles}) + (R_{datalength} + 3) \times R_{clkcycles}$$

where

- T_{event} = 5 ns (minimum repeat capture time)
- $5(R_{clkcycles})$ = number cycles for FIFO to ALU to Shift register
- $R_{clkcycles}$ is period of R_{CLK} data = 300 MHz, SDR = 3.33 ns
- $R_{datalength}$ = number of results bits = 40 for THS789 device (2)

In the case where R_{CLK} = 300 MHz, with 40-bit serial result:

$$\text{Min Latency} = 5 \text{ ns} + 17 \text{ ns} + (40 + 3) \times 3.33 \text{ ns} = 165 \text{ ns} \quad (3)$$

$$\text{Max Latency} = 5 \text{ ns} + 17 \text{ ns} + (40 + 3) \times 3.33 \text{ ns} + (40 + 3) \times 3.33 \text{ ns} = 308 \text{ ns} \quad (4)$$

Programming (continued)

NOTE

The THS789 device was intended for sync-event, event, event, sync-event ... processing. However, some applications desire the use of a sync pulse that is a fixed period. During a sync period, there could be multiple events, or no events. The TMU can be used effectively for this scenario as well.

For applications using the THS789 device in this fashion, it is important to consider the uncertainty that is introduced by the load pulse timing. Because the load pulse is free running and asynchronous to any events, the latency will vary based on this timing. Additionally, the load pulse is the mechanism that will cause the ALU to grab the current sync value for the result calculation.

If an event is in the FIFO, waiting for the load pulse and a new sync occurs, the ALU will use the new sync value for calculating the result. In this case, the event would precede the sync resulting in a negative result. The system could then offset the result by one sync cycle as the result is negative, indicating that is was captured during a prior sync cycle.

7.5.2.5 TMU Calibration

The TMU calibration process is identical to a normal TMU time-stamp measurement. The process involves measuring a known interval and calculating the difference between the measured value and the actual value. The result is then stored into calibration registers inside the TMU. The TMU takes the stored calibration values and corrects the subsequent time-stamp measurements.

There are four calibration registers for each channel. These are identified as follows:

- A calibration register for positive sync edge and positive event edge
- A calibration register for positive sync edge and negative event edge
- A calibration register for negative sync edge and positive event edge
- A calibration register for negative sync edge and negative event edge

Calibration due to temperature changes following the initial system calibration may be required if temperature variations are significant.

7.5.2.6 Temperature Sensor

A temperature sensor has been located centrally in the THS789 device for monitoring the die temperature. There are two monitor outputs for this feature. An analog voltage proportional to the die temperature is presented at the TEMP pin. Also, an overtemperature alarm output is available at the OT_ALARM pin. The overtemperature alarm (OT_ALARM) is an open-drain output that is activated when the die temperature reaches 141°C.

The overtemperature alarm sets a register bit (OT_ALM) in the central register and may be accessed through the serial interface.

The overtemperature alarm initiates an automatic power down to prevent overheating of the device. The digital blocks remain functional when in automatic power down. Following a power down, the user is required to reset OT_ALM using the serial interface. A register bit (RST_OT_ALM) is used for this purpose.

The temperature-monitoring function and its associated overtemperarture alarm circuit may be disabled by the user, using a register bit (OT_EN). The default for the temperature-monitoring function is disabled.

OT_EN = 1: Temperature-monitoring function is enabled.
OT_EN = 0: Temperature-monitoring function is disabled.

7.6 Register Maps

7.6.1 Register Address Space

Table 5. Channel-A Registers

Address (Hex)	Register	
00h–01h	Control register	R/W
02h–03h	Not used	NA
04h	Status registers	RO
05h	Not used	NA
06h	Not used	R/W
07h	Not used	R/W
08h	Not used	R/W
09h	Not used	R/W
0Ah	Not used	R/W
0Bh	Not used	R/W
0Ch	Positive edge sync and positive edge hit calibration register, 16 bits	R/W
0Dh	Positive edge sync and negative edge hit calibration register, 16 bits	R/W
0Eh	Negative edge sync and positive edge hit calibration register, 16 bits	R/W
0Fh	Negative edge sync and negative edge hit calibration register, 16 bits	R/W
10h–12h	Timestamp register, 40 bits	R
13h–1Fh	Not used	NA

Table 6. Channel-B Registers

Address (Hex)	Register	
20h–21h	Control register	R/W
22h–23h	Not used	NA
24h	Status registers	RO
25h	Not used	NA
26h	Not used	R/W
27h	Not used	R/W
28h	Not used	R/W
29h	Not used	R/W
2Ah	Not used	R/W
2Bh	Not used	R/W
2Ch	Positive edge sync and positive edge hit calibration register, 16 bits	R/W
2Dh	Positive edge sync and negative edge hit calibration register, 16 bits	R/W
2Eh	Negative edge sync and positive edge hit calibration register, 16 bits	R/W
2Fh	Negative edge sync and negative edge hit calibration register, 16 bits	R/W
30h–32h	Timestamp register, 40 bits	R
33h–3Fh	Not used	NA

Table 7. Channel-C Registers

Address (Hex)	Register	
40h–41h	Control register	R/W
42h–43h	Not used	NA
44h	Status registers	RO
45h	Not used	NA
46h	Not used	R/W
47h	Not used	R/W
48h	Not used	R/W
49h	Not used	R/W
4Ah	Not used	R/W
4Bh	Not used	R/W
4Ch	Positive edge sync and positive edge hit calibration register, 16 bits	R/W
4Dh	Positive edge sync and negative edge hit Calibration register, 16 bits	R/W
4Eh	Negative edge sync and positive edge hit Calibration register, 16 bits	R/W
4Fh	Negative edge sync and negative edge hit Calibration register, 16 bits	R/W
50h–52h	Timestamp register, 40 bits	R
53h–5Fh	Not used	NA

Table 8. Channel-D Registers

Address (hex)	Register	
60h-61h	Control register	R/W
62h-63h	Not used	NA
64h	Status registers	RO
65h	Not used	NA
66h	Not used	R/W
67h	Not used	R/W
68h	Not used	R/W
69h	Not used	R/W
6Ah	Not used	R/W
6Bh	Not used	R/W
6Ch	Positive sync edge and positive hit edge, calibration register, 16 bits	R/W
6Dh	Positive sync edge and negative hit edge, calibration register, 16 bits	R/W
6Eh	Negative sync edge and positive hit edge, calibration register, 16 bits	R/W
6Fh	Negative sync edge and negative hit edge, calibration register, 16 bits	R/W
71h-73h	Timestamp register, 40 bits	R
74h-7Fh	Not used	NA

Table 9. Central Registers

Address (hex)	Register	
80h	Control register	R/W
81h	Control register	R/W
82h	Status register	RO
83h	Chip ID	RO
84h	Test key register	R/W
85h	Test1	R/W
86h	Test2	R/W
87h	Reserved	R/W
88h	Reserved	R/W

7.6.2 Register Map Detail

Table 10. Channel A

Register Address	Register Name	Word/Bit																Default Value
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
00h	Control	X	X	0n_A	0	0	0	X	X	X	0	0	0	0	Pol_A	ChA_IP_En	En_ChA	0000h
01h	Control	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	0	0000h
04h	Status	X	X	X	X	X	X	X	X	X	X	X	FIFO_Empty_A	FIFO_Full_A	X	X	DLL_Lock_A	0000h
06h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0000h
0Ch	Calibration:Pos Sync EdgePos Event Edge	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h
0Dh	Calibration:Pos Sync EdgeNeg Event Edge	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h
0Eh	Calibration:Neg Sync EdgePos Event Edge	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h
0Fh	Calibration:Neg Sync EdgeNeg Event Edge	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h
10h	Timestamp	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h
11h		D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	0000h
12h		0	0	0	0	0	0	0	0	D39	D38	D37	D36	D35	D34	D33	D32	0000h

Table 11. Channel B

Register Address	Register Name	Word/Bit																Default Value
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
20h	Control	X	X	0	0	0	0	X	X	X	0	0	0	0	Pol_B	ChB_IP_En	En_ChB	0000h
21h	Control	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	0	0000h
24h	Status	X	X	X	X	X	X	X	X	X	X	X	FIFO_Empty_B	FIFO_Full_B	X	X	DLL_Lock_B	0000h
26h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0000h
2Ch	Calibration:Pos Sync EdgePos Event Edge	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h
2Dh	Calibration:Pos Sync EdgeNeg Event Edge	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h
2Eh	Calibration:Neg Sync EdgePos Event Edge	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h
2Fh	Calibration:Neg Sync EdgeNeg Event Edge	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h

Table 11. Channel B (continued)

Register Address	Register Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default Value
30h	Timestamp	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h
31h		D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	0000h
32h		0	0	0	0	0	0	0	0	D39	D38	D37	D36	D35	D34	D33	D32	0000h

Table 12. Channel C

Register Address	Register Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default Value
40h	Control	X	X	0	0	0	0	X	X	X	0	0	0	0	Pol_C	ChC_IP_En	En_ChC	0000h
41h	Control	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	0	0000h
44h	Status	X	X	X	X	X	X	X	X	X	X	X	FIFO_Empty_C	FIFO_Full_C	X	X	DLL_Lock_C	0000h
46h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0000h
4Ch	Calibration:Pos Sync EdgePos Event Edge	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h
4Dh	Calibration:Pos Sync EdgeNeg Event Edge	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h
4Eh	Calibration:Neg Sync EdgePos Event Edge	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h
4Fh	Calibration:Neg Sync EdgeNeg Event Edge	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h
50h	Timestamp	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h
51h		D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	0000h
52h		0	0	0	0	0	0	0	0	D39	D38	D37	D36	D35	D34	D33	D32	0000h

Table 13. Channel D

Register Address	Register Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default Value
60h	Control	X	X	0	0	0	0	X	X	X	0	0	0	0	Pol_D	ChD_IP_En	En_ChD	0000h
61h	Control	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	0	0000h
64h	Status	X	X	X	X	X	X	X	X	X	X	X	FIFO_Empty_D	FIFO_Full_D	X	X	DLL_Lock_D	0000h
66h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0000h

Table 13. Channel D (continued)

Register Address	Register Name	Word/Bit																Default Value
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
6Ch	Calibration:Pos Sync EdgePos Event Edge	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h
6Dh	Calibration:Pos Sync EdgeNeg Event Edge	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h
6Eh	Calibration:Neg Sync EdgePos Event Edge	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h
6Fh	Calibration:Neg Sync EdgeNeg Event Edge	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h
70h	Timestamp	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000h
71h		D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	0000h
72h		0	0	0	0	0	0	0	0	D39	D38	D37	D36	D35	D34	D33	D32	0000h

Table 14. Central Registers

Register Address	Register Name	Word/Bit																Default Value
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
80h	Control	RCLK_En	PWR_DN	Sync_IP_En	Sync_TS_Pol	RST_OT_ALM	OT_En	1	0	1	0	0	0	0	1	RESET	Test_En	0000h
81h	Control	X	X	X	X	X	X	X	X	X	X	X	X	Quiet_Mod	CNT_Rng1	CNT_Rng0	X	0000h
82h	Status	X	X	X	X	X	X	X	X	X	X	X	X	DLL_Lock_1G2	DLL_Lock_Sync	OT_ALM	TMU_Ready	0000h
83h	Chip ID	ID	ID	ID	ID	ID	ID	ID	ID	Rev	Rev	Rev	Rev	Rev	Rev	Rev	Rev	8010h

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The THS789 device is a high-speed, high-resolution time-measurement unit that measures the difference in time between a signal applied to an event channel and the signal applied to the sync channel. This difference is then transmitted to a result interface in the form of a digital word. Figure 6 shows an example of three time measurements (T1, T2, and T3).

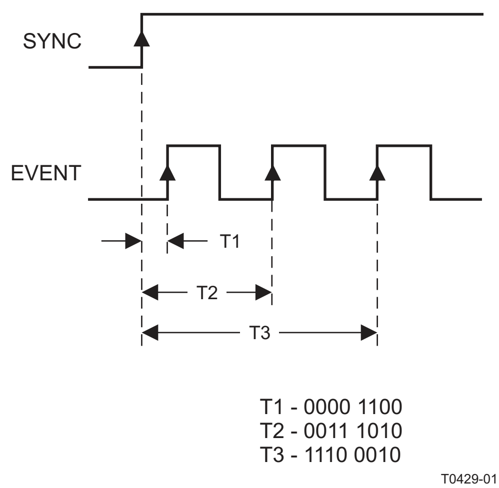


Figure 6. Time-Measurement Example With 8-Bit Words Triggered by Rising Edges

The previous time difference is calculated by an internal ALU that subtracts the timestamps created by the Event signal and the SYNC signal stored in a FIFO. These timestamps are performed by the TDC that is composed by the following: an interpolator, a synchronizer, a 34-bit counter, and a 1.2-GHz clock. It is important to note that the event and sync channels share the same TDC. When a valid edge is applied to the event channel, the TDC uses the value in the counter and stores it in the FIFO. Then the ALU uses the value of the event and the value of the sync, stored in the FIFO already, and subtracts them. After the operation is done, the final value is shifted out to the result interface for retrieval.

All the programming to the THS789 device is achieved through an LVCMOS host-serial interface. With this interface, the user has the ability to set up the THS789 device for time measurements. It also provides the user with different modes to retrieve the results.

Results are available through an LVDS-compatible high-speed serial interface. Data-word length and speed are programmable to cover a wide range of data rates. Each channel has it own output to maximize data throughput. All of the data ports (RdataA, -B, -C, and -D) are synchronized to a global clock.

8.2 Typical Application

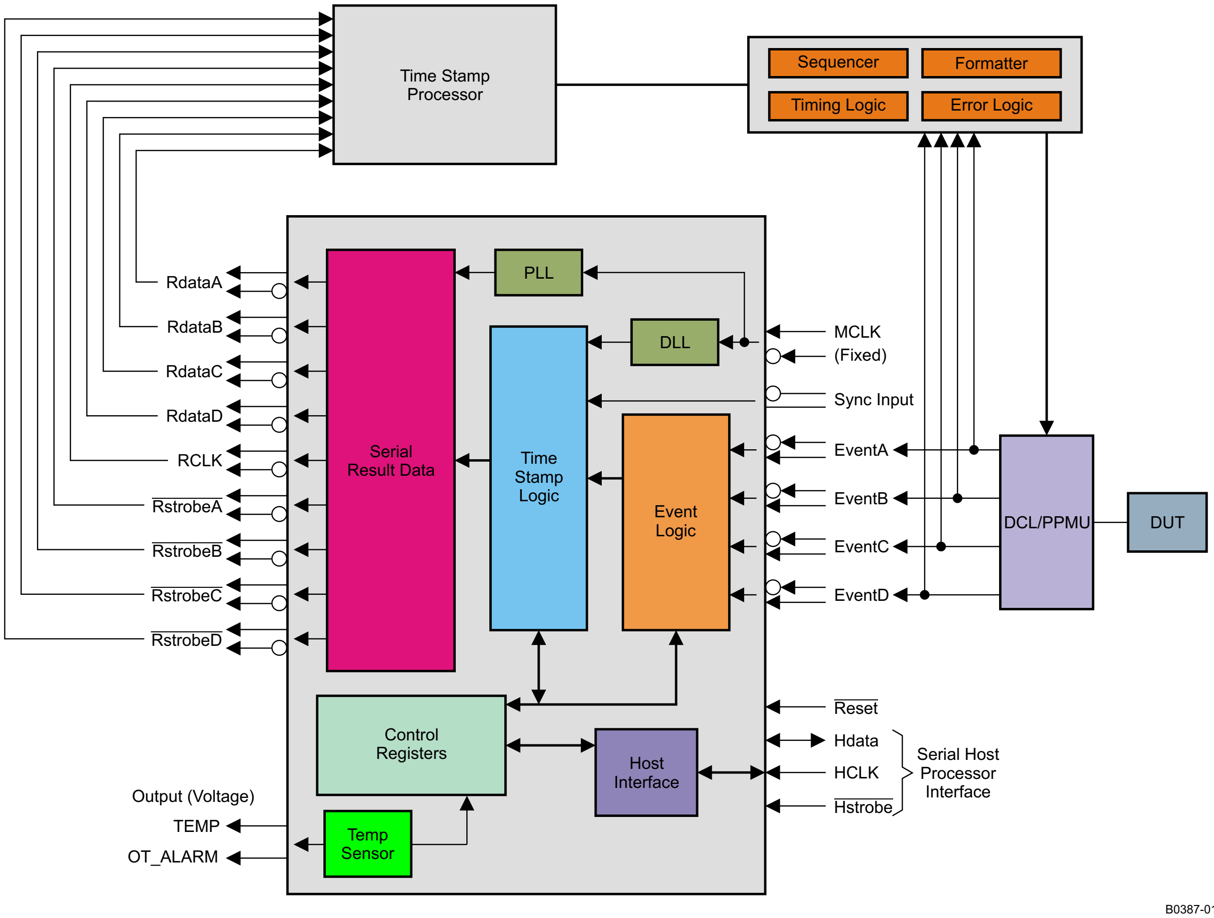


Figure 7. Example of Application Diagram in ATE Environment

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 15 as the input parameters.

Table 15. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Results interface size	40 bit
Results time range	–7.158 to 7.158 s
Rclock	300 MHz
DDR mode	Off
Temperature monitor	On
Connect CD/Connect AB	Off
Counter size	34 bit
REGISTER WRITE (80h)	0xA680
REGISTER WRITE (81h)	0x0003

8.2.2 Detailed Design Procedures

8.2.2.1 Time Measurement

Time measurements in the THS789 device follow the timing of Figure 8. This diagram illustrates that time measurements are valid as long as events do not happen at speeds higher than 200 MHz. If an event happens at less than 5 ns from the previous one, then this event is ignored. The same applies to the SYNC signal. Even though the minimum period is 5 ns, the pulse duration of both Event and SYNC signals can be as low as 200 ps.

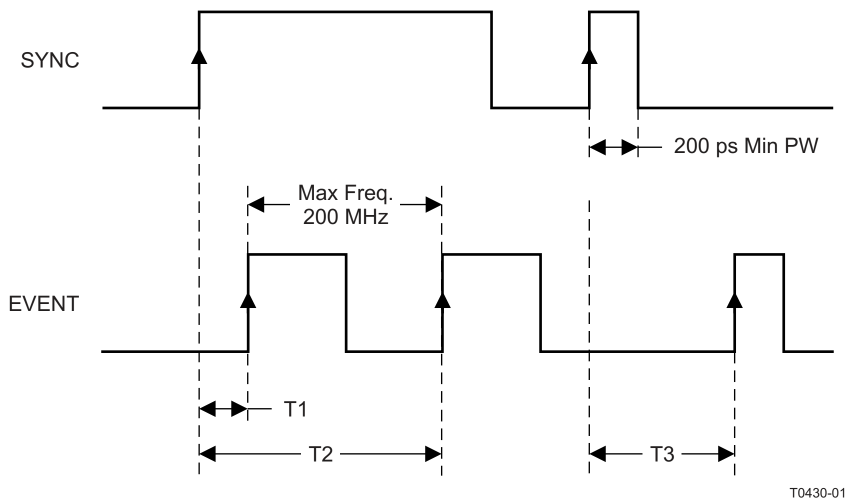


Figure 8. Time-Measurement Example at Maximum Retrigger Rate and Minimum Pulse Duration

The TH788 is capable of making time measurements using any combination of rising-falling edge between Event and SYNC. The example in Figure 8 uses rising edges only to trigger the time measurement. Table 16 describes what registers bits must be programmed to achieve the desired combination. Registers to be programmed are 00h, 20h, 40h, and 60h for event channels and 80h for the sync channel. The examples in Figure 9 illustrate the other three combinations. All of the channels can be programmed individually with respect to the sync channel.

Table 16. Trigger Polarity Programmability

REGISTER BITS		TRIGGER POLARITY FROM SYNC TO EVENT
SYNC_TS_Pol	Pol_X	
0	0	Pos to Pos
0	1	Pos to Neg
1	0	Neg to Pos
1	1	Neg to Neg

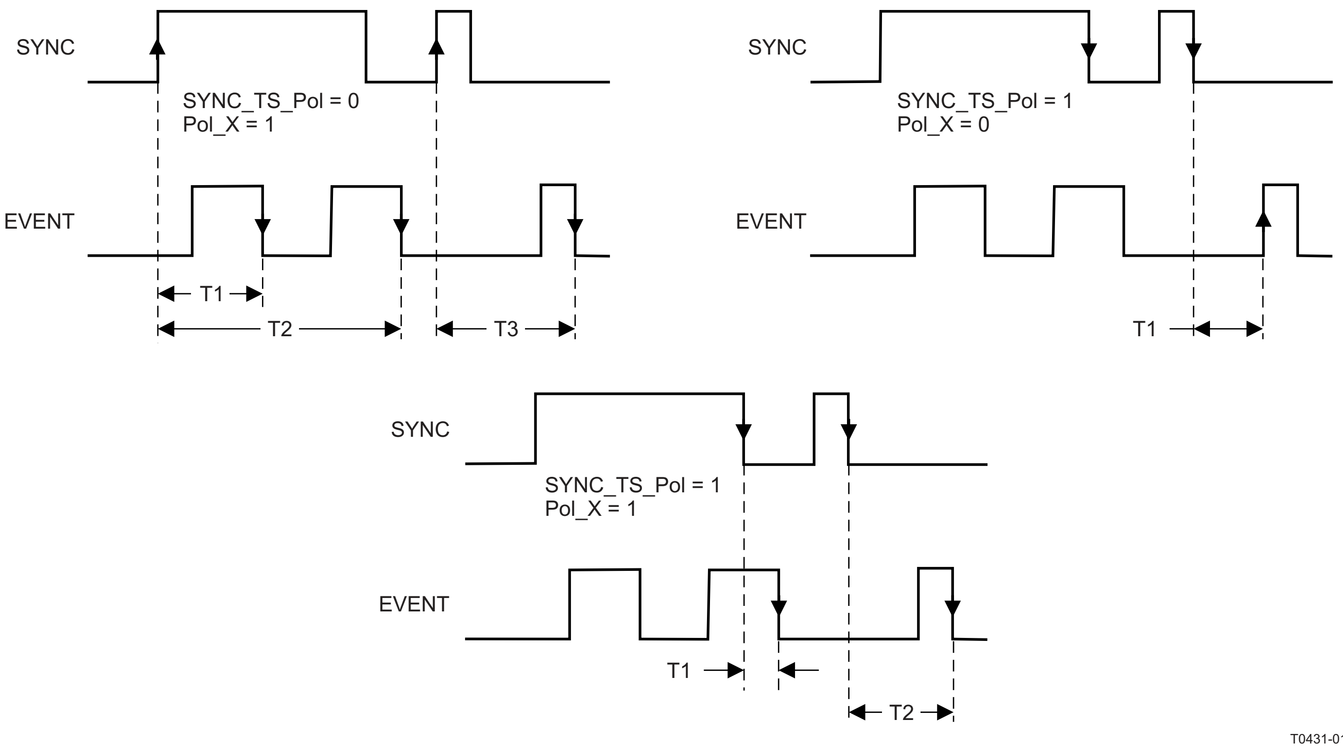


Figure 9. Time-Measurement Examples With Different Edge Polarities

8.2.2.2 Output Clock to Data/Strobe Phasing

The output of each channel is an Rdata and Rstrobe signal. The RCLK for all the channels is a common output. Operating at 300 MHz, these signals must be handled carefully. Particularly important are the termination and phase alignment of the signals at the receiving circuitry. Termination has been discussed previously. Phase alignment is now discussed: The two outputs from each channel are clocked out through identical flip-flops with the same internal clock. Data and strobe output edges from a particular channel match well (< 50 ps). The match channel-to-channel is not as good due to the greater wiring distances internal to the TMU. However, the total time difference is below 125 ps. Because the RClock is a common output, the wiring lengths from the four channels must be matched and controlled to achieve good setup and hold times at the input to the receiving circuit. The RClock rising edge is adjusted internal to the TMU to be close to the center of the eye diagram of the data/strobe signals. (The internal clock has a good 50/50 duty cycle. The rising edge clocks out the data/strobe. The falling edge is inverted and used as the RClock after appropriate adjustments for the internal propagation delay times.) The receiving circuitry requirements for setup and hold timing must be carefully examined for the proper timing. Delays may be added to the PCB microstrips to adjust timing. A good rule is 125 ps of delay per inch of microstrip length.

8.2.2.3 Master Clock Input and Clock Multiplier

All of the internal timing of the TMU is derived from the 200-MHz master clock. Therefore, its quality is critical to the accurate operation of the TMU. Absolute accuracy of the master clock linearly affects the accuracy of the measurements. This imposes little burden upon the master clock, as accurate oscillators are easy to procure or distribute. However, the jitter of the master clock is also highly critical to the single-event precision of the TMU and should be absolutely minimized (< 3-ps RMS). A carefully selected crystal oscillator can meet this requirement. However, jitter can build up quite quickly in a clock distribution scheme and must be carefully controlled. Be careful that the LVDS input to the master clock is not badly distorted or that the rise and fall times are slow (> 0.6 ns).

Discussion of the clock multiplier follows: The TMU operates from a master-clock frequency of 1200 MHz, which implies a measurement period of 0.833 ns. The master counter runs from this frequency, and all the other clocks are divided down from this main clock. An interpolator allows finer precision in time measurement, as discussed elsewhere. The clock multiplier is the circuit that takes the 200-MHz master-clock reference and generates from that the high quality 1200-MHz clock. The clock multiplier consists of five major sections: First is the delay-lock loop (DLL), which is a series connection of 12 identical and closely matched variable time-delay circuits. A single control voltage connects to each of the delay elements. The master 200-MHz clock connects to the input of the DLL. Because the period of 200 MHz is 5 ns, if the control voltage is adjusted to make the time delay of the DLL equal to 5 ns, the input and the output of the delay line is exactly phase matched. A phase detector connected to the input and the output of the delay line can sense this condition accurately, and a feedback loop with a low-offset-error amplifier is included in the clock multiplier to achieve this result. These are the second and third circuit blocks. With 12 equally spaced 200-MHz clock phases, select out six equally spaced 833-ps-wide pulses with AND gates and combine these pulses into a single 1200-MHz clock waveform with a six-input OR gate. The last circuit element is a powerful differential signal buffer to distribute the 1200-MHz clock to the various circuit elements in the TMU. The DLL feedback loop is fairly narrowband, so some time is required to allow the DLL to initialize at start-up (about 100 µs, typical). The DLL is insensitive to the duty cycle of the input 200-MHz clock. Duty cycles of 40/60 to 60/40 are acceptable. What matters most is as little jitter as possible.

8.2.2.4 Temperature Measurement and Alarm Circuit

Chip temperature of the TMU is monitored by a temperature sensor located near the center of the chip. A small buffer outputs a voltage proportional to the absolute temperature of the TMU. The buffer drives a load of up to 100 pF typical (50 pF minimum) and open circuit to 10 kΩ to ground resistive. The output voltage slope is 5 mV, typical. Therefore, the output voltage equation is as follows:

$$\text{Output Voltage} = (\text{Temperature in °C} \times 5\ \text{mV}) + 1.365\ \text{V} \quad (5)$$

Also included in the TMU is an overtemperature comparator. At approximately 140°C, the alarm goes active, and at approximately 7°C below this temperature, the alarm becomes inactive (hysteresis of 7°C prevents tripping on noise and comparator oscillations). If the alarm goes active, the chip powers down and sets a bit in the serial register.

An alarm output pin is provided that is an open-drain output. Connect this output through a pullup resistor to the 3.3-V power supply. The resistor must be at least 3.3 kΩ. This creates a slow-speed, low-voltage CMOS digital output with a logical 1 being the normal operating state and a logical 0 being the overtemperature state.

8.2.2.5 LVDS-Compatible I/Os

The Event, SYNC, and master-clock inputs are LVDS-compatible input receivers optimized for high-speed and low-time-distortion operation. The Rdata, Rstrobe, and RCLK outputs are similarly LVDS-compatible output drivers optimized for high-speed/low-distortion operation, driving 50-Ω transmission lines. Typically, LVDS data transmission is thought of in terms of 100-Ω twisted-wire-pair (TWP) transmission lines. TWP is not applicable to printed wiring boards and high-speed operation. Therefore, the THS789 device interfaces were designed to operate most effectively with 50-Ω, single-ended transmission lines. Instead of a current-mode output with its correspondingly high output impedance, a more-nearly impedance-matched voltage-mode output driver is used. This minimizes reflections from mismatched transmission line terminations and the resulting waveform distortion. The input receivers do not include the 100-Ω terminating resistor, which must be connected externally to the THS789 device. This was done to accommodate daisy-chaining the THS789 inputs. Input offset voltage was minimized, and the fail-safe feature in the LVDS standard was eliminated in order to minimize distortion.

8.2.2.6 LVDS-Compatible Inputs

The four event inputs, the sync input and the master-clock input all use the same input interface circuitry. Figure 10 is a simplified schematic diagram of the LVDS-compatible receiver input stage. The input signal is impedance-transformed and level-shifted with a PNP emitter-follower and translated into ECL-like differential signals with a common-emitter amplifier. There is no internal termination resistor and no internal pullup or pulldown resistors. Unused inputs may be tied off by connecting both input terminals to ground. If the input terminals are left floating, they are protected by ESD clamps from damage; however, noise may be injected into the THS789 device and may degrade accuracy. The peak input voltage limits are 0.6 V to 1.7 V. Outside of these limiting voltages, parts of the input circuit may saturate and distort the timing.

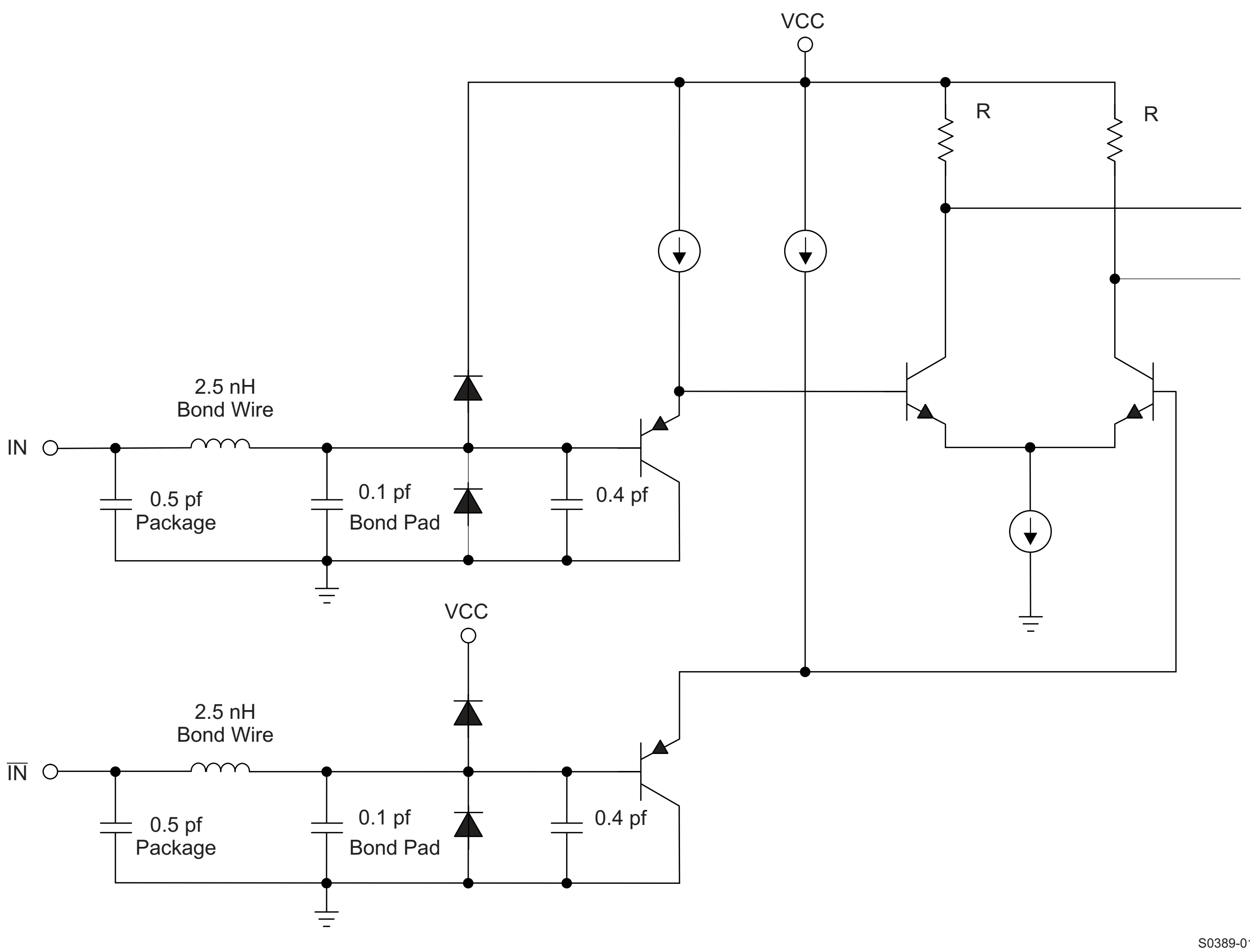


Figure 10. Simplified Schematic of the LVDS Input

Figure 11 shows the typical input connections. The transmission line lengths must be matched from the driver to the THS789 input [< 0.5 inch (1.27 cm) difference] and terminated in a 100-Ω resistor placed close [< 0.25 inch (0.635 cm)] to the TMU input pins. The resistor total tolerance should be below 5%. The power dissipation is below 5 mW, so small surface-mounted resistors are preferred.

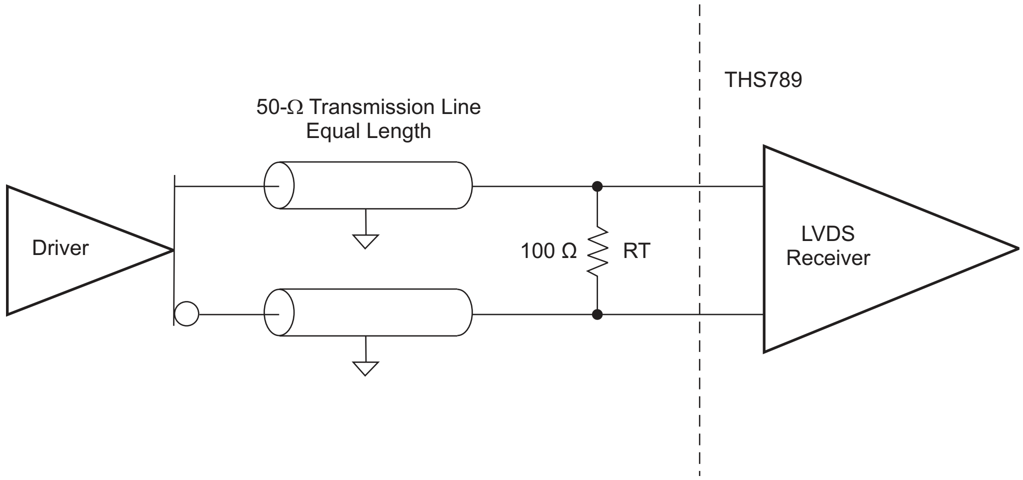


Figure 11. Typical Input Connection to the THS789

8.2.2.7 LVDS-Compatible Outputs

Figure 12 shows a typical wiring diagram of an LVDS output. The transmission line lengths must be matched. A termination resistor may be required if the chosen receiver does not have an internal resistor. Concerning termination resistors: LVDS was originally conceived with twisted-wire pairs of approximately 100-Ω line-to-line impedance. The 100-Ω resistor between lines is simple and effective to terminate such a line. For the higher-speed operation of the THS789 device, use a pair of 50-Ω transmission lines, such as microstrip on the PC board. The same 100-Ω resistor line-to-line termination works well, because the line signals are equal and opposite in phase. This results in the center of the 100-Ω resistor having a constant voltage equal to the common-mode voltage and each side having an apparent 50-Ω termination. An improvement in the termination can be achieved by splitting the 100 Ω into two 50-Ω resistors and ac-grounding (bypassing) the center to ground with a 1000-pF (not critical) capacitor. The termination improvement is usually small and increases the room and parts count. It is the best approach as long as the PCB layout high-frequency performance is not compromised by the higher parts count. As mentioned previously, the driver is optimized to drive 50-Ω transmission lines and provides a driving-point impedance approximating 50 Ω to suppress reflections. Figure 8 is a simplified schematic of the output driver. A standard ECL-like circuit drives the outputs through 25-Ω resistors. The combination of the resistors and the emitter-follower output impedance approximates 50 Ω. The output emitter-followers are biased by current sources that are switched to conserve power. A feedback loop varies the voltage on the two RLs to set and maintain the 1.28-V common-mode voltage of the LVDS-compatible outputs. Another feedback loop holds the emitters of the current switches to 0.4 V to keep the 4-mA current source from saturation.

The outputs are short-circuit-proof to a 3.3-V power supply. Shorts to ground should be avoided, as the power dissipation in certain components may exceed safe limits.

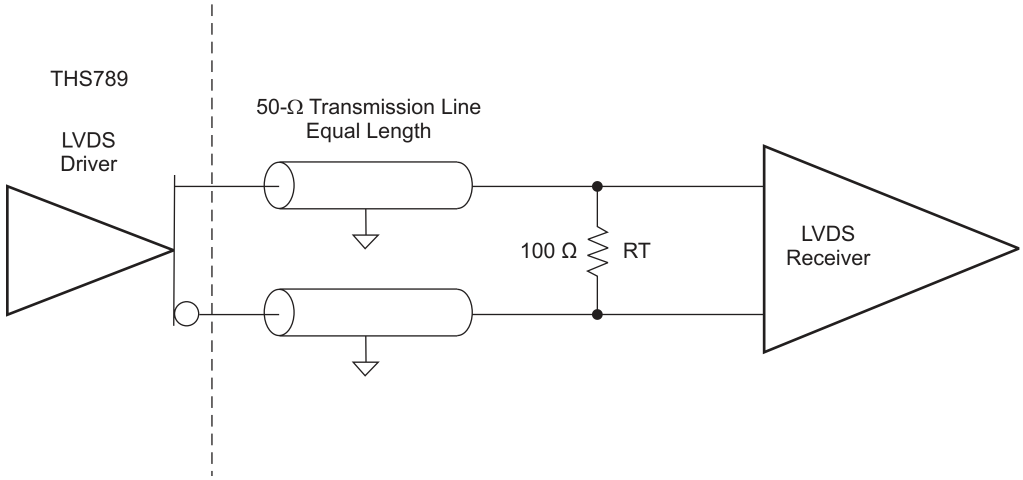


Figure 12. Typical Output Connection to the THS789

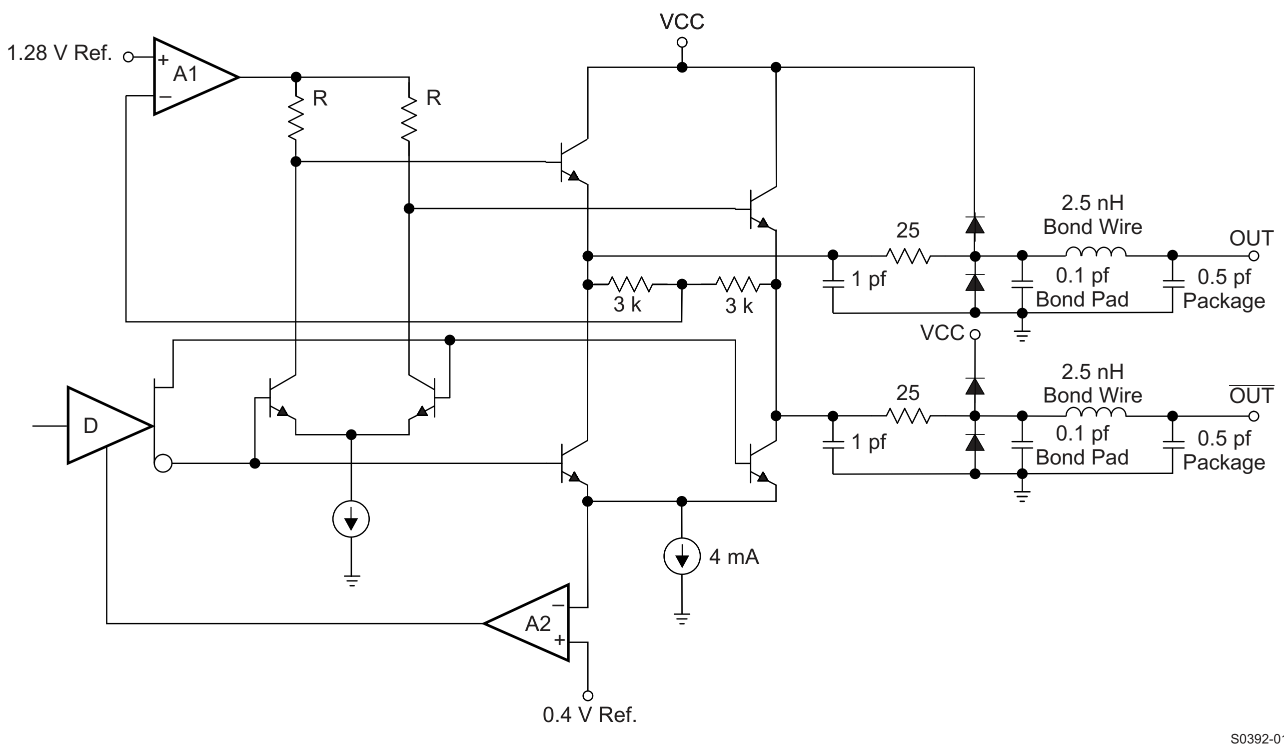


Figure 13. Simplified Schematic of the LVDS Output Driver

8.2.3 Application Curve

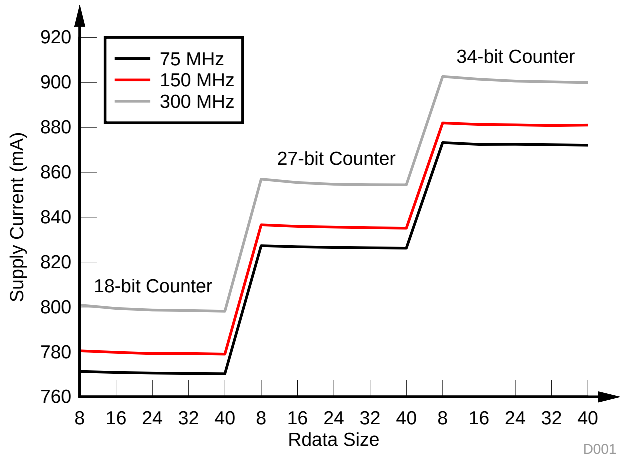


Figure 14. 4-Channel Supply Current vs Rdata, Counter, and Rclock Functional Modes

9 Power Supply Recommendations

All the high-speed time-measurement circuitry in the TMU is implemented in differential emitter-coupled logic (ECL). Besides high speed, a characteristic of differential ECL is good rejection of power-supply noise and variation. However, there is a great deal of CMOS logic, FIFO and output-serial interface circuitry that is an excellent source of power-supply current noise. Therefore, to maintain the best accuracy, the TMU power supply must be low-impedance. This is accomplished in the usual ways by careful layout, good ground and power planes, short traces to the power and ground pins, and capacitive bypassing. TI recommends placing a quality, low inductance, high-frequency bypass capacitor of approximately 0.01 µF close to each power pin. The 0402 size works well. Additional bypass capacitors of larger value should be placed near the TMU, making low-inductance connection with the power and ground planes. With a typical power-supply sensitivity of 30 ps/V, a 1% power supply shift yields a 1-picosecond additional error, making power-supply regulation important for the best accuracy.

10 Layout

10.1 Layout Guidelines

Figure 15 and Figure 16 show typical layout examples for this device.

Use 100-Ω terminating resistors for all LVDS inputs. TI recommends placing all the LVDS input resistors as close as possible to the device (the six pairs of pads are shown in Figure 16 on the left and right sides). The other pads found on the bottom side image are the pairs of decoupling capacitors (0.1 µF and 0.01 µF) for the multiple V_{DD} pins. As noted before, keep the distance between these caps, V_{DD}, and Ground as short as possible.

Keep all differential signals as close as possible to the same length to reduce inaccuracies in timestamp measurement.

10.2 Layout Example

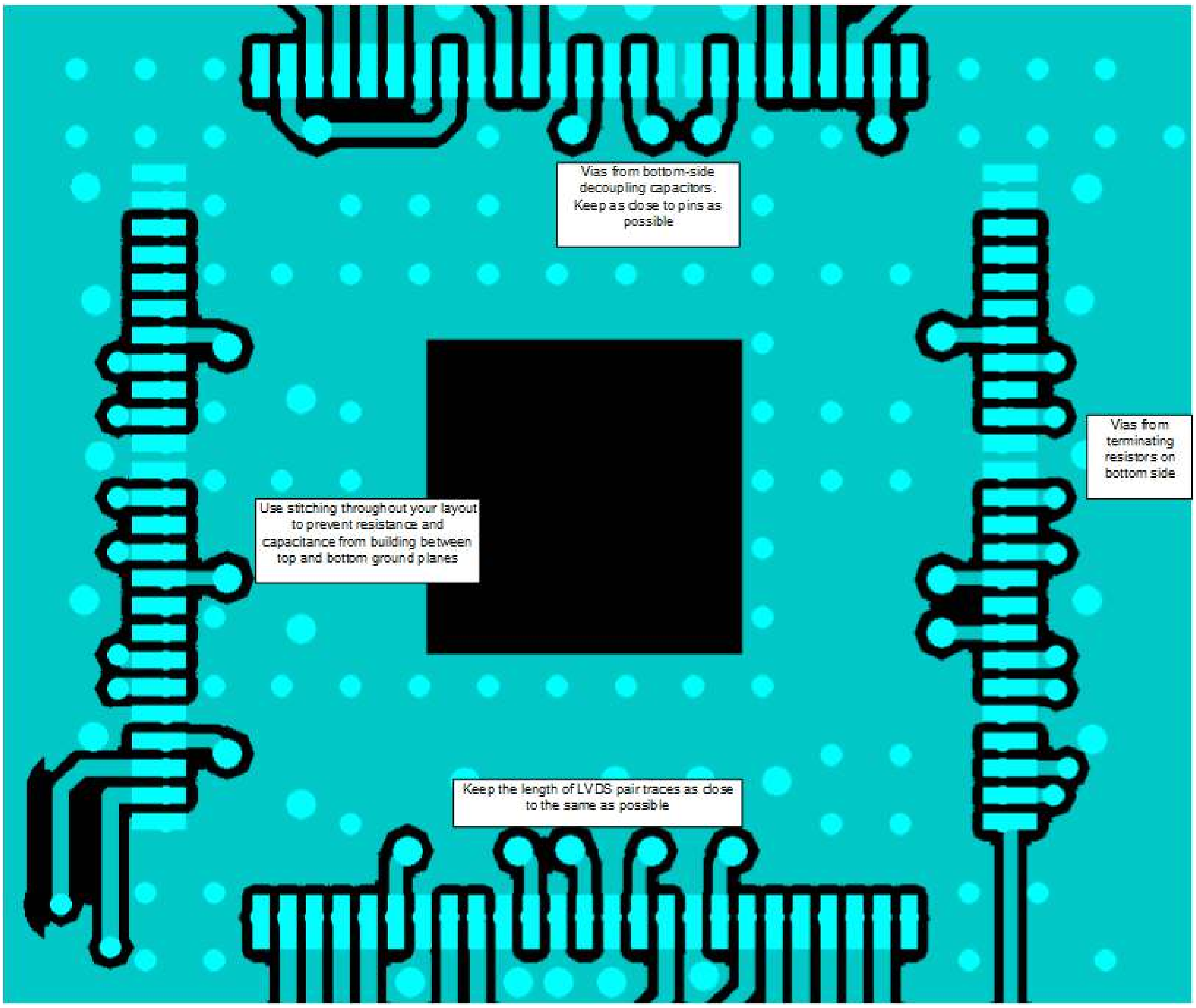


Figure 15. Top (Device-Side) Layer Example

Layout Example (continued)

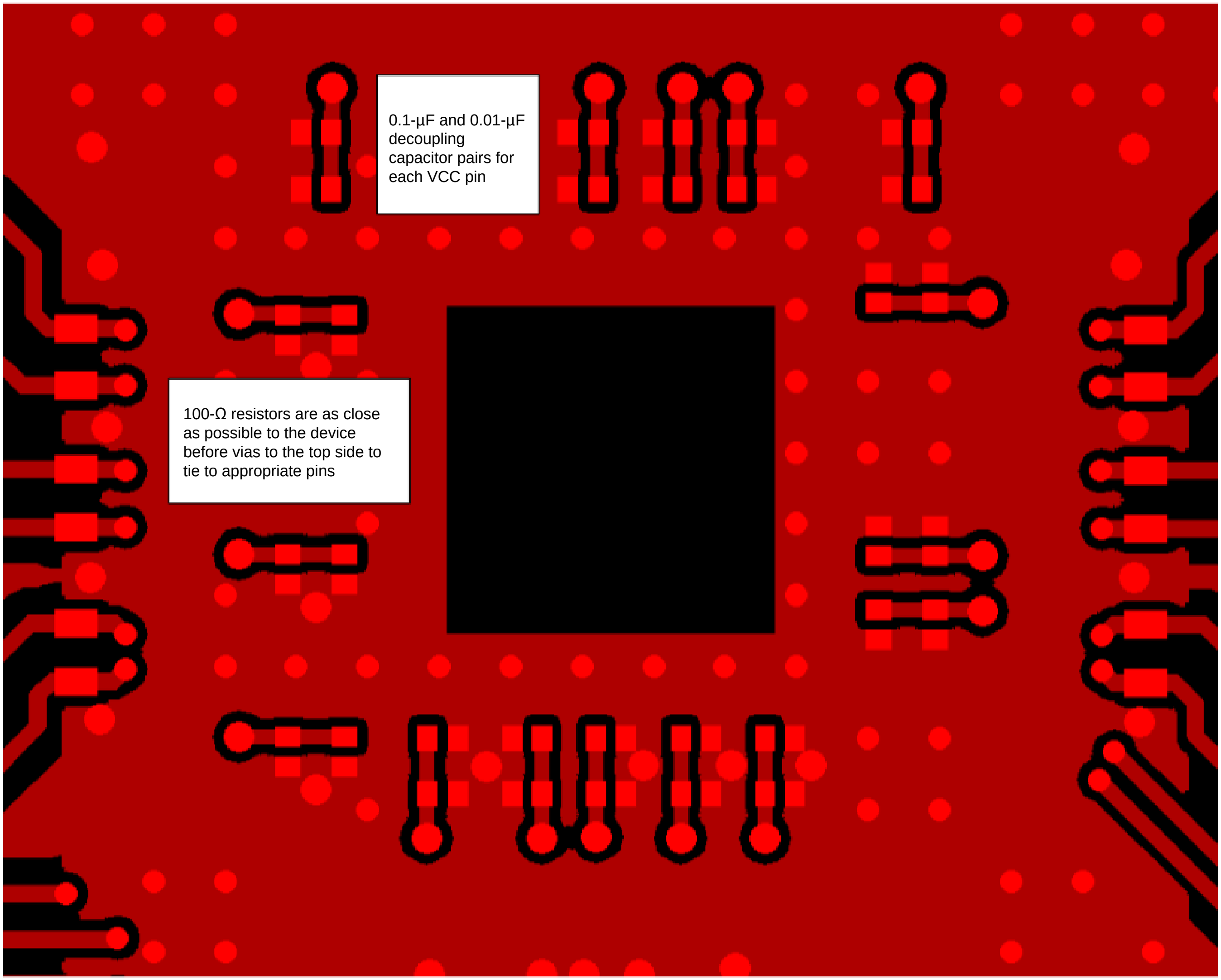


Figure 16. Bottom (Signal Termination and Power Decoupling) Layer Example

10.3 Thermal Considerations

The TMU package provides a thermally conductive heat slug at the top for connection to an additional heatsink. The TMU can be placed into many different modes for optimization of performance versus power dissipation, and a table has been provided to help determine the power required. The heat sink should be carefully considered in order to keep the TMU temperature within required limits and to promote the best temperature stability. The TMU time measurement drift with temperature is an excellent 0.1 ps/°C. A good heat sink design takes advantage of the low temperature drift of the TMU.

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS789PFD	NRND	HTQFP	PFD	100	90	RoHS & Green	NIPDAU	Level-4-260C-72 HR	0 to 70	THS789PFD	

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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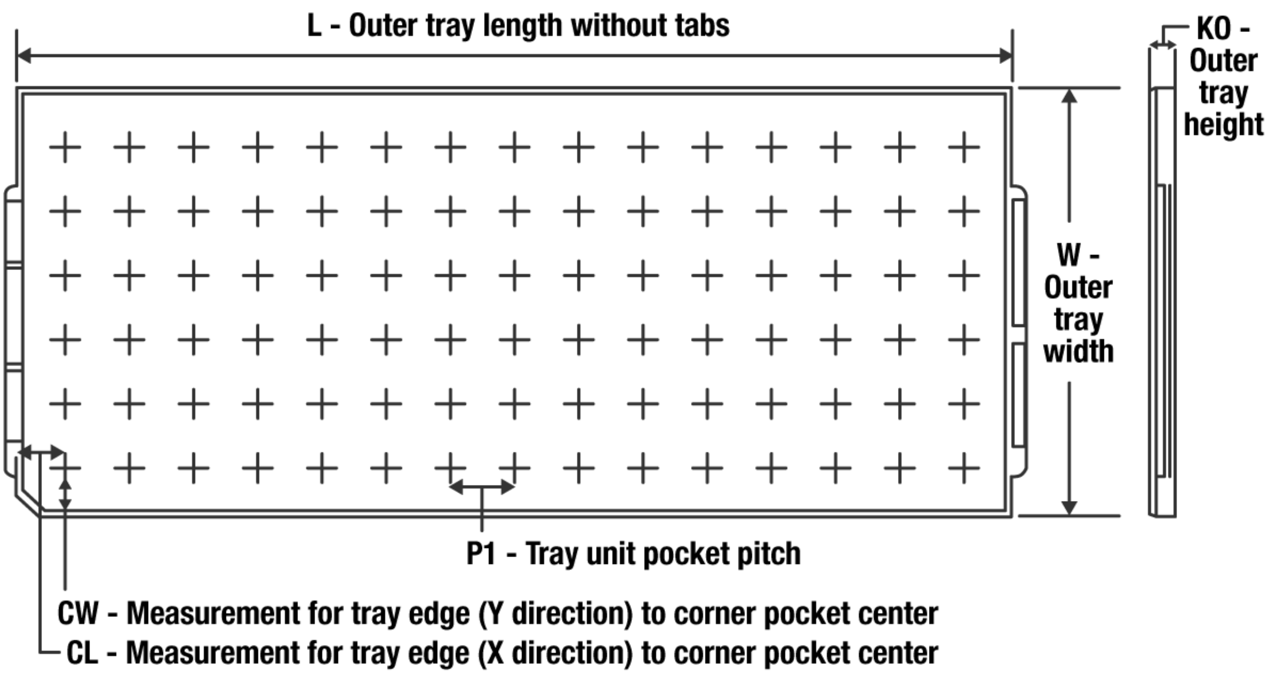
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY

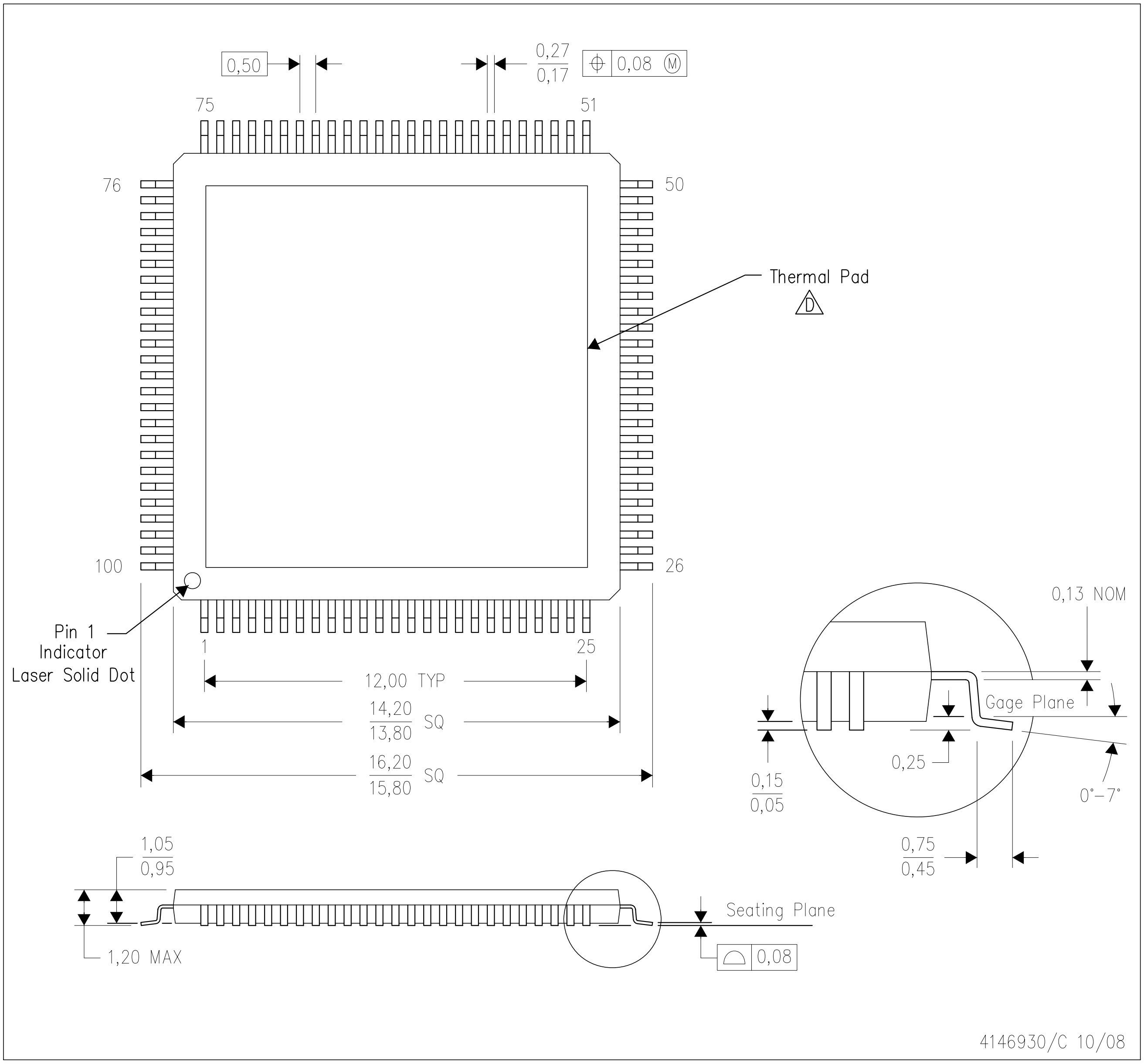


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
THS789PFD	PFD	HTQFP	100	90	6 X 15	150	315	135.9	7620	20.3	15.4	15.45

PFD (S-PQFP-G100) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

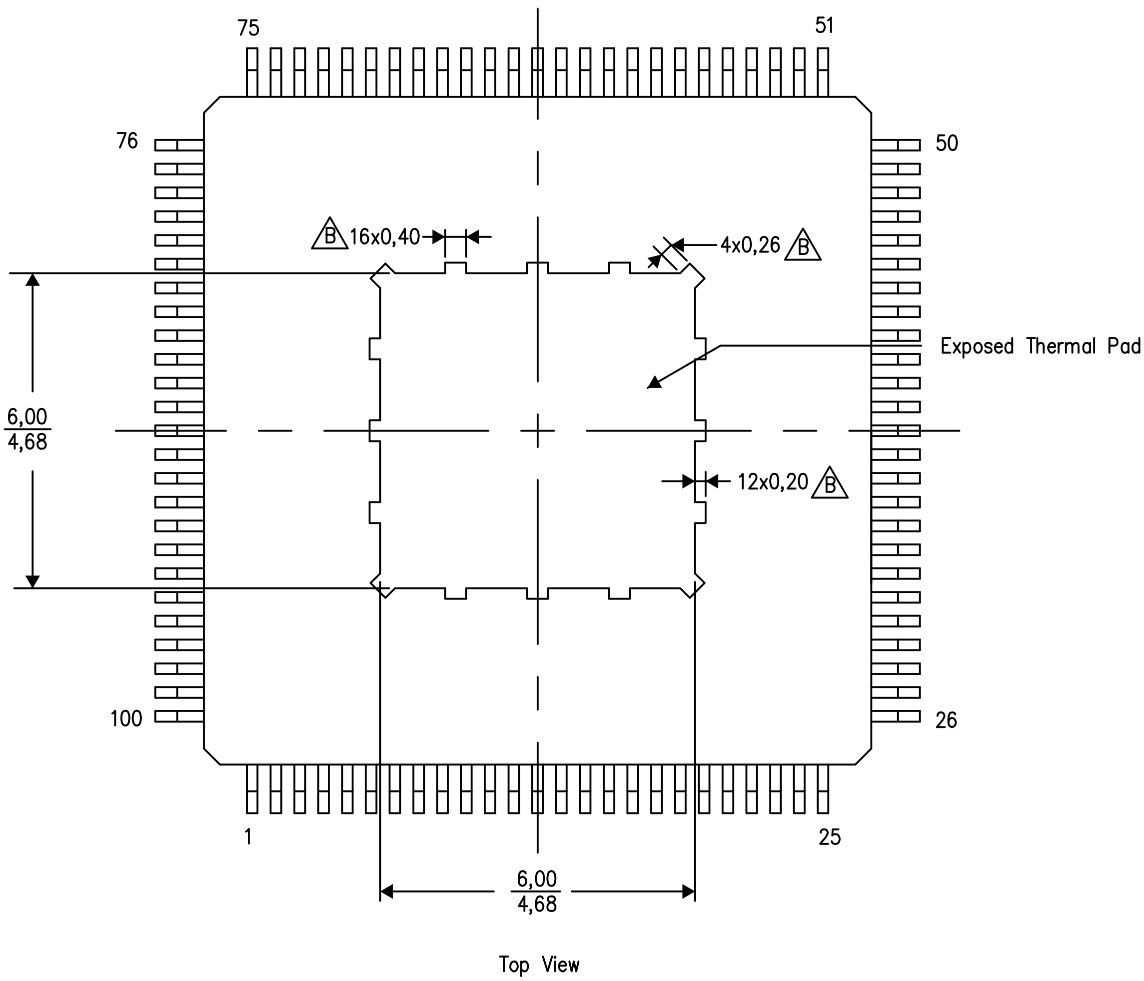
PFD (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4211595–2/B 06/14

NOTE: A. All linear dimensions are in millimeters

B. Tie strap features may not be present.

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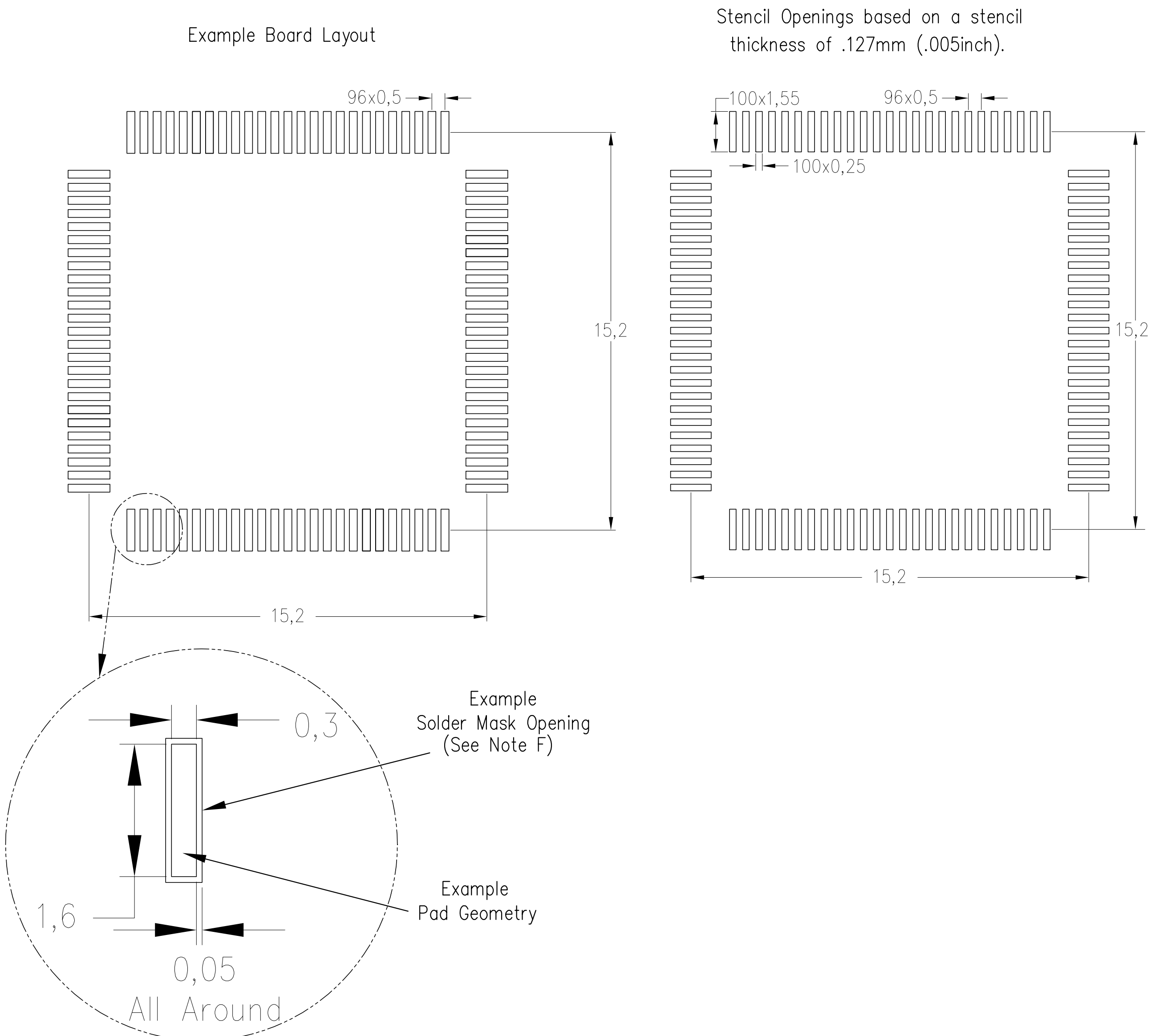
PFD (S-PQFP-G100) PowerPAD™ PLASTIC QUAD FLATPACK



4211596/A 03/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265