

1.8V Operating Voltage 3rd Overtone Quartz Crystal Oscillator IC with Input Tolerant Function

■ GENERAL DESCRIPTION

The NJU6227 series is a C-MOS quartz crystal oscillator IC realized excellent frequency stability for 3rd Overtone (up to 160MHz) oscillation, and consists of an oscillation amplifier, a 3-state output buffer, a built-in LDO and a input tolerant circuit.

The operating voltage is from 1.62V to 3.63V (x3, x4, x5, x6: from 2.25V to 3.63V), and the LDO holds down the characteristic change of the oscillation amplifier for operating voltage variation, and has been stabilized oscillation frequency (Frequency stability $\pm 1\text{ppm}@V_{DD}\pm 10\%$).

The input tolerant circuit ensures that 0 to 3.63 V can be applied to CONT terminal without regard to the supply voltage.

The oscillation stopping current is very low stand-by mode, therefore, it is suitable for the portable items of the communication equipment and the like. The 3-state output buffer is C-MOS compatible. The NJU6227A/D version are available for driving light loads (15pF load) and NJU6227C version are available for driving heavy loads (30pF load).

■ PACKAGE OUTLINE

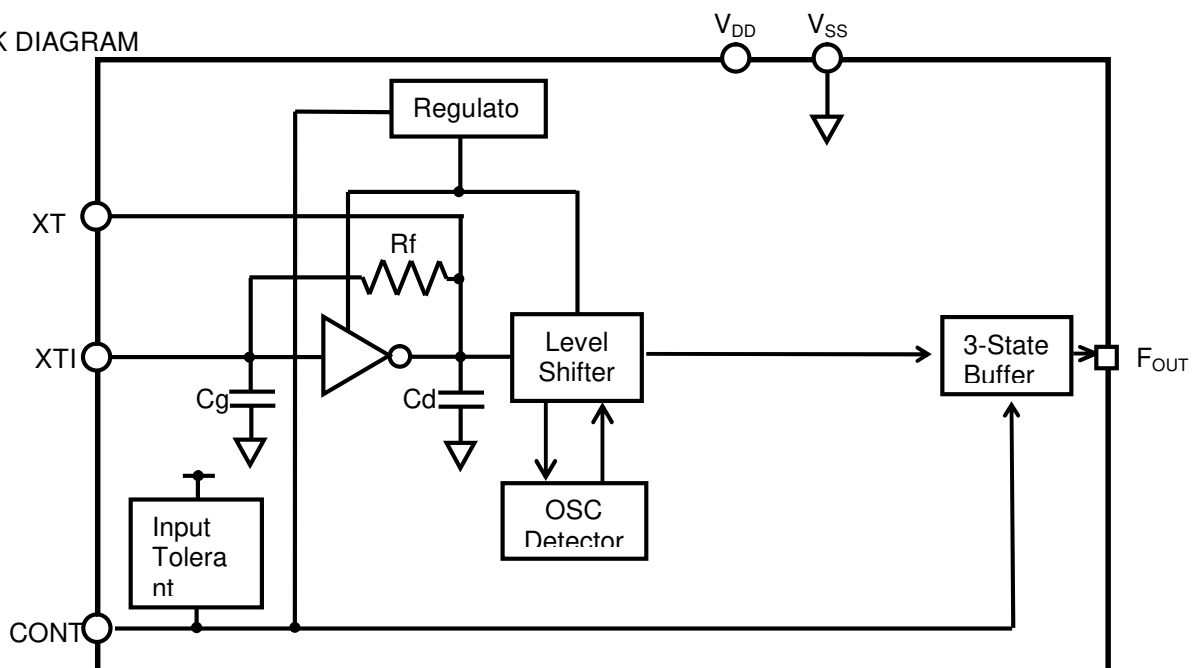


NJU6227xXC-V

■ FEATURES

- Maximum Oscillation Frequency 160MHz(3rd Overtone)
- Frequency Stability $\pm 1\text{ppm}@V_{DD}\pm 10\%$
- Wide Operating Voltage 1.62 to 3.63V(x3, x4, x5, x6 2.25V to 3.63V)
- Built-in LDO
- Input Tolerant Circuit 0 to 3.63V@CONT Term.
- Stand-by Function (Oscillation Stop and High-Z)
- 3-State Output Buffer
- Variable Pull-up Resistance on-Die (CONT Terminal: Pull-up resistance is large at Stand-by Function)
- Oscillation Capacitors Cg and Cd on-Die
- C-MOS Technology
- Package Outline Die/Wafer

■ BLOCK DIAGRAM

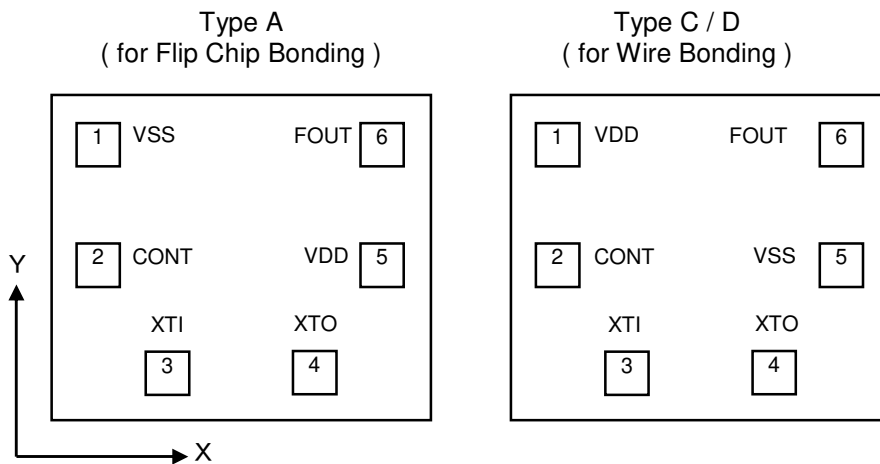


LINE-UP TABLE

Type No.	Recommended Oscillation Frequency	Version		
		Type A	Type C	Type D
NJU6227	40 to 50MHz	A1*	C1	D1
	50 to 60MHz	A2*	C2	D2
	60 to 85MHz	A3*	C3	D3
	85 to 110MHz	A4*	C4	D4
	110 to 130MHz	A5*	C5	D5
	130 to 160MHz	A6*	C6	D6

* Under development and tentative value.

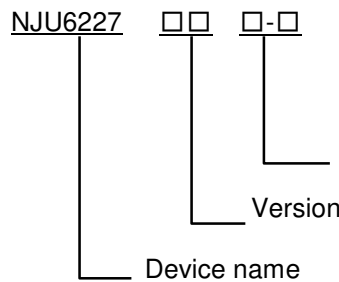
PAD LOCATION



COORDINATES

	X	Y
1	-261.5	198.5
2	-261.5	-21.5
3	-146.5	-211.5
4	144.5	-211.5
5	260.5	-21.5
6	260.5	198.5

PART NUMBER



W-H: Wafer (200μm)
 W-B: Wafer (160μm)
 WS4-V:1/4Wafer(130μm)
 C-V: Chip(130μm)

Starting Point: Die Center Unit[μm]
 Die Size: 0.73x0.63mm
 Die Thickness (C-V): 130±15μm
 Wafer Thickness(WS4-V): 130±15μm
 Wafer Thickness (W-B): 160±20μm
 Wafer Thickness (W-H): 200±20μm
 Pad size: 80x80μm
 Die Substrate: V_{SS} level

VERSION DISCRIMINATION INTERNAL COMPONENTS

PAD layout version of the NJU6227 series is determined by the mask pattern and Notch Number. Frequency version of the NJU6227 series is determined by the internal fuse trimming.

Type Number and PAD layout version are identified externally by the combination of the version name marking (1), the locations of trimmed fuses (3) and The Notch number (2). (Table 1 shows the chip version identification)

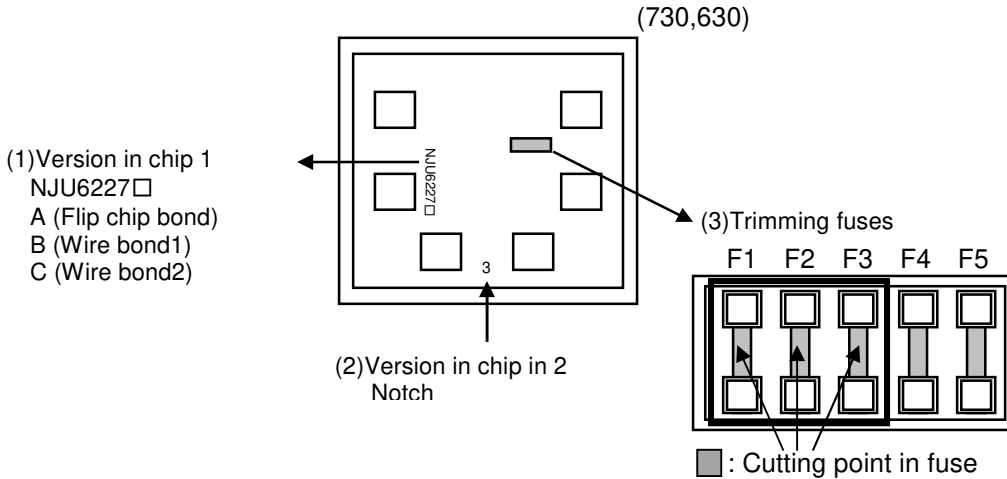


Table1: Frequency version and Cutting point in fuse.

Discrimination 1	Discrimination 2	Type No.	Version name	Mask / Version set by trimming fuses				
				Mask	Trimming fuses			
					Version	F1	F2	F3
NJU6227A	4	NJU6227A	NJU6227A1	A	*	-	-	Untrimmed
			NJU6227A2	A	*	-	*	
			NJU6227A3	A	-	-	-	
			NJU6227A4	A	-	-	*	
			NJU6227A5	A	-	*	-	
			NJU6227A6	A	-	*	*	
NJU6227C	4	NJU6227D	NJU6227D1	D	*	-	-	
			NJU6227D2	D	*	-	*	
			NJU6227D3	D	-	-	-	
			NJU6227D4	D	-	-	*	
			NJU6227D5	D	-	*	-	
			NJU6227D6	D	-	*	*	
NJU6227C	3	NJU6227C	NJU6227C1	C	*	-	-	
			NJU6227C2	C	*	-	*	
			NJU6227C3	C	-	-	-	
			NJU6227C4	C	-	-	*	
			NJU6227C5	C	-	*	-	
			NJU6227C6	C	-	*	*	

Note1) “-”: Uncut, “*”: Cutting

(Ta=+25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V _{DD}	x3, x4, x5, x6 version	2.25		3.63	V
Input Voltage	V _{IN}	CONT	0		3.63	V
Output Voltage	V _{OUT}	F _{OUT}	0		V _{DD}	V
Output Frequency Stability	df/f	V _{DD} ±10%		±1		ppm

Note3) C0 minimum requirement

Version: x1, x2, x3, x4, x5 $1\text{pF} \leq C0 \leq 3\text{pF}$

Version: x6 $1.5\text{pF} \leq C0 \leq 3\text{pF}$

($V_{DD}=1.62$ to $3.63V$ (x3, x4, x5, x6 2.25 to $3.63V$), $V_{SS}=0V$, $T_a=+25^{\circ}C$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	
Operating Current	I_{DD}	x1 version No load CONT=Open $f_{osc}=50MHz$	$V_{DD}=1.8V$	-	2.0	2.6	mA
			$V_{DD}=2.5V$	-	2.4	3.1	
			$V_{DD}=3.3V$	-	3.1	4.0	
		x2 version No load CONT=Open $f_{osc}=60MHz$	$V_{DD}=1.8V$	-	2.4	3.1	
			$V_{DD}=2.5V$	-	2.8	3.6	
			$V_{DD}=3.3V$	-	3.6	4.7	
		x3 version No load CONT=Open $f_{osc}=85MHz$	$V_{DD}=2.5V$	-	6.0	7.8	
			$V_{DD}=3.3V$	-	7.0	9.1	
		x4 version No load CONT=Open $f_{osc}=110MHz$	$V_{DD}=2.5V$	-	6.6	8.6	
			$V_{DD}=3.3V$	-	7.8	10.1	
		x5 version No load CONT=Open $f_{osc}=130MHz$	$V_{DD}=2.5V$	-	6.8	8.8	
			$V_{DD}=3.3V$	-	8.2	10.7	
		x6 version No load CONT=Open $f_{osc}=160MHz$	$V_{DD}=2.5V$	-	7.5	9.8	
			$V_{DD}=3.3V$	-	9.0	11.7	
Oscillation Stopping Current	I_{STB}	CONT= V_{SS} , No load	-	-	10	μA	
Output Voltage	V_{OH}	$I_{OH}=4mA$	$V_{DD}-0.4$	-	-	V	
	V_{OL}	$I_{OL}=4mA$	-	-	0.4	V	
Input Voltage	V_{IH}	CONT Input Tolerant Function	$0.7V_{DD}$	-	-	V	
	V_{IL}	CONT	-	-	$0.3V_{DD}$	V	
Input Current Note4)	I_{IN}	CONT= $3.63V$	-	-	1	μA	
		CONT= $0.8V_{DD}$	-	-	8		
		CONT= $0.2V_{DD}$	-	-	5		
3-state Off Leakage Current	I_{OZ}	CONT= V_{SS} , $F_{OUT}=V_{DD}$ or V_{SS}	-	-	± 0.1	μA	

Note4) Absolute value.

($V_{DD}=1.62$ to $3.63V$ (x3, x4, x5, x6 2.25 to $3.63V$), $V_{SS}=0V$, $T_a=+25^{\circ}C$)

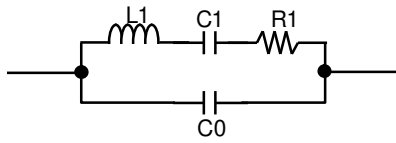
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	
Feedback Resistance	Rf	x1 version	-	12.5	-	kΩ	
		x2 version	-	6.8	-		
		x3 version	-	6.8	-		
		x4 version	-	12.3	-		
		x5 version	--	12.4	-		
		x6 version	-	12.5	-		
Internal Capacitor	Cg/Cd	x1 version	-	7.2/7.2	-	pF	
		x2 version	-	7.2/7.2	-		
		x3 version	-	7.2/7.2	-		
		x4 version	-	5.1/5.4	-		
		x5 version	-	4.2/4.1	-		
		x6 version	-	3.1/3.1	-		
Oscillation Frequency	fosc	Recommendation Note5)	40	-	50	MHz	
			50	-	60		
			60	-	85		
			85	-	110		
			110	-	130		
Output Signal Symmetry	SYM	$C_L=15pF$, @ $V_{DD}/2$	45	50	55	%	
Output Signal Rise Time	tr	NJU6227C $C_L=15pF$ $0.1V_{DD}$ to $0.9V_{DD}$	$V_{DD}=1.8V$	-	2.0	4.0	ns
			$V_{DD}=2.5V$	-	1.1	2.1	
			$V_{DD}=3.3V$	-	0.8	1.7	
		NJU6227A/D $C_L=15pF$ $0.1V_{DD}$ to $0.9V_{DD}$	$V_{DD}=1.8V$	-	2.75	5.5	
			$V_{DD}=2.5V$	-	1.4	2.8	
			$V_{DD}=3.3V$	-	1.1	2.2	
Output Signal Fall Time	tf	NJU6227C $C_L=15pF$ $0.9V_{DD}$ to $0.1V_{DD}$	$V_{DD}=1.8V$	-	1.7	3.4	ns
			$V_{DD}=2.5V$	-	1.0	1.9	
			$V_{DD}=3.3V$	-	0.8	1.5	
		NJU6227A/D $C_L=15pF$ $0.9V_{DD}$ to $0.1V_{DD}$	$V_{DD}=1.8V$	-	2.25	4.5	
			$V_{DD}=2.5V$	-	1.35	2.7	
			$V_{DD}=3.3V$	-	1.05	2.1	
Output Disable time	t_{POZ}	$C_L=15pF$, $R_L=1k\Omega$	-	-	100	ns	
Output Enable Time	t_{PZO}	$C_L=15pF$	-	-	1	ms	

Note5) NJR's standard crystal is used for measurement of the oscillation frequency range and it does not guarantee oscillation. (Refer to EXAMPLE OF CRYSTAL PARAMETERS FOR MEASUREMENT CIRCUIT)

The oscillator circuit is optimized for small sized crystal oscillators.

When using for 7050 and 5032 sized crystal element that have large C0 and parasitic capacitance, additional evaluation is recommended before implementation due to the increased risk of insufficient oscillation margin.

EXAMPLE OF CRYSTAL PARAMETERS FOR MEASUREMENT CIRCUITS

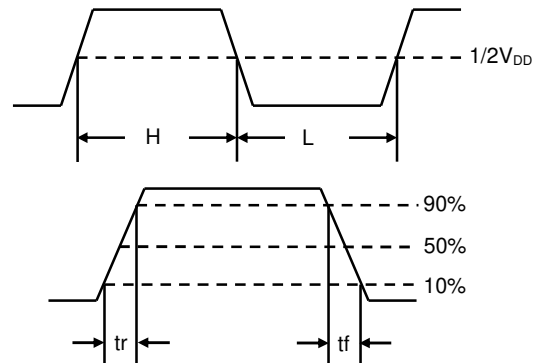
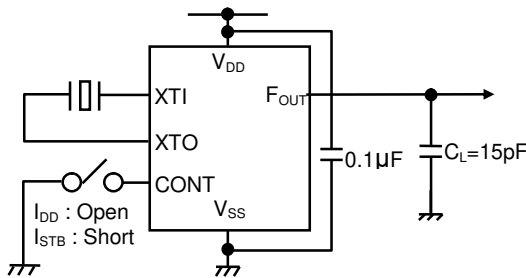


f[MHz]	R1[Ω]	L1[mH]	C1[fF]	C0[pF]
40	34.8	20.8	0.76	2.42
50	67.1	27.5	0.37	1.46
60	33.1	10.7	0.66	2.49
90	42.2	6.68	0.47	2.03
113	30.2	3.52	0.56	3.22
125	30.3	2.61	0.62	3.47
133	24.7	2.11	0.68	3.60
155	38.3	1.55	0.68	3.75

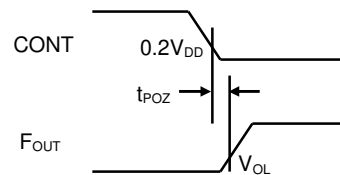
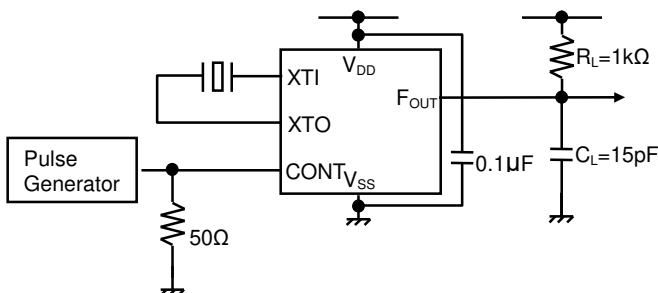
Note6) Please do use as small as possible parasitic capacitance of Crystal and V_{SS} , V_{DD} terminal.
When using for large size package, the parasitic capacitance upward tendency.

MEASUREMENT CIRCUITS

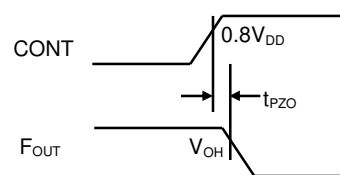
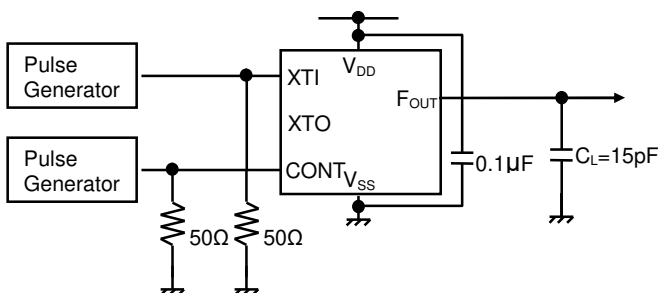
(1) Operating Current ($C_L=0pF$), Stand-by Current, Output Signal Symmetry($C_L=15pF$), Output Signal Rise/Fall Time ($C_L=15pF$)



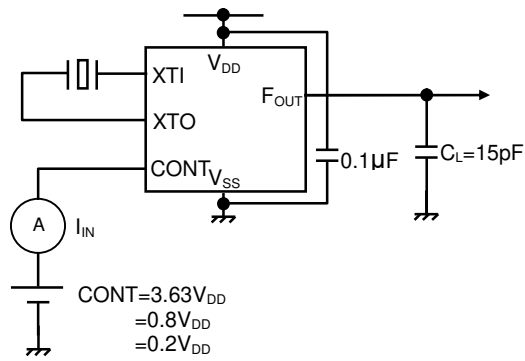
(2) Output Disable Time ($C_L=15pF, R_L=1k\Omega$)



(3) Output Enable Time ($C_L=15pF$)



(4) Input Current ($C_L=15\text{pF}$)



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