

NDD03N50Z

N-Channel Power MOSFET 500 V, 3.3 Ω

Features

- Low ON Resistance
- Low Gate Charge
- ESD Diode–Protected Gate
- 100% Avalanche Tested
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V _{DSS}	500	V
Continuous Drain Current R _{θJC}	I _D	2.6	A
Continuous Drain Current R _{θJC} , T _A = 100°C	I _D	1.7	A
Pulsed Drain Current, V _{GS} @ 10 V	I _{DM}	10	A
Power Dissipation R _{θJC}	P _D	58	W
Gate–to–Source Voltage	V _{GS}	±30	V
Single Pulse Avalanche Energy, I _D = 2.6 A	E _{AS}	120	mJ
ESD (HBM) (JESD22–A114)	V _{esd}	2000	V
Peak Diode Recovery	dv/dt	4.5 (Note 1)	V/ns
Continuous Source Current (Body Diode)	I _S	2.6	A
Maximum Temperature for Soldering Leads	T _L	260	°C
Operating Junction and Storage Temperature Range	T _J , T _{stg}	–55 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

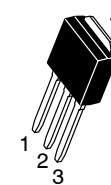
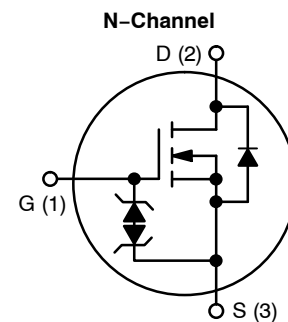
1. I_D ≤ 2.6 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, T_J ≤ 150°C.



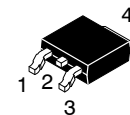
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V _{DSS}	R _{DS(on)} (MAX) @ 1.15 A
500 V	3.3 Ω



**IPAK
CASE 369D
STYLE 2**



**DPAK
CASE 369AA
STYLE 2**

MARKING AND ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

NDD03N50Z

THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	2.2	°C/W
Junction-to-Ambient Steady State	(Note 3) NDD03N50Z (Note 2) NDD03N50Z-1	41 80	

2. Insertion mounted

3. Surface mounted on FR4 board using 1" sq. pad size, (Cu area = 1.127 in sq [2 oz] including traces).

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	500			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	Reference to 25°C , $I_D = 1\text{ mA}$		0.6		V/°C
Drain-to-Source Leakage Current	I_{DSS}	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	25°C		1.0	μA
			150°C		50	
Gate-to-Source Forward Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$			±10	μA

ON CHARACTERISTICS (Note 4)

Static Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 1.15\text{ A}$		2.8	3.3	Ω
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 50\text{ }\mu\text{A}$	3.0		4.5	V
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 1.15\text{ A}$		1.8		S

DYNAMIC CHARACTERISTICS

Input Capacitance (Note 5)	C_{iss}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	219	274	329	pF
Output Capacitance (Note 5)	C_{oss}		28	38	50	
Reverse Transfer Capacitance (Note 5)	C_{rss}		6.0	8.0	10	
Total Gate Charge (Note 5)	Q_g	$V_{DD} = 250\text{ V}, I_D = 2.6\text{ A},$ $V_{GS} = 10\text{ V}$	5.0	10	16	nC
Gate-to-Source Charge (Note 5)	Q_{gs}		1.2	2.3	4.0	
Gate-to-Drain ("Miller") Charge (Note 5)	Q_{gd}		3.2	5.5	8.0	
Plateau Voltage	V_{GP}			6.4		V
Gate Resistance	R_g		1.5	4.5	13.5	Ω

RESISTIVE SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 2.6\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 5\text{ }\Omega$		9.0		ns
Rise Time	t_r			7.0		
Turn-Off Delay Time	$t_{d(off)}$			15		
Fall Time	t_f			7.0		

SOURCE-DRAIN DIODE CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Diode Forward Voltage	V_{SD}	$I_S = 2.6\text{ A}, V_{GS} = 0\text{ V}$			1.6	V
Reverse Recovery Time	t_{rr}	$V_{GS} = 0\text{ V}, V_{DD} = 30\text{ V}$ $I_S = 2.6\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		240		ns
Reverse Recovery Charge	Q_{rr}			0.7		μC

4. Pulse Width $\leq 380\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

5. Guaranteed by design.

NDD03N50Z

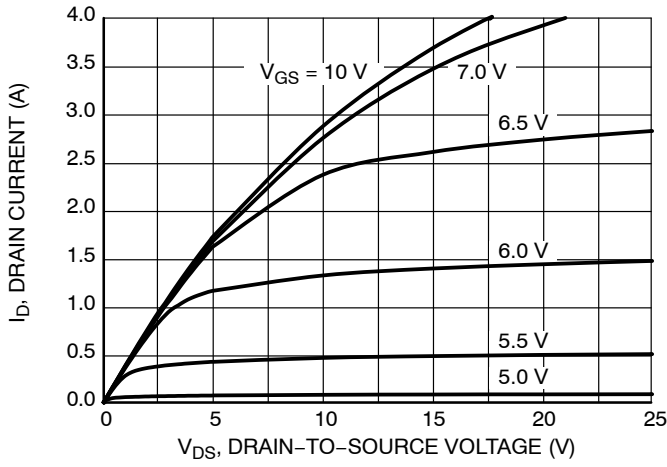


Figure 1. On-Region Characteristics

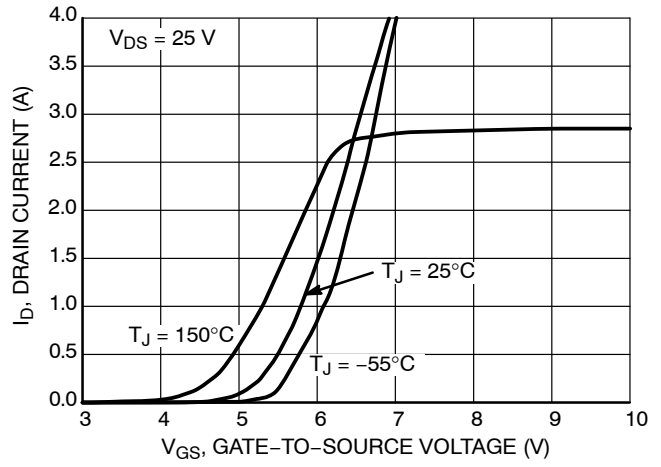


Figure 2. Transfer Characteristics

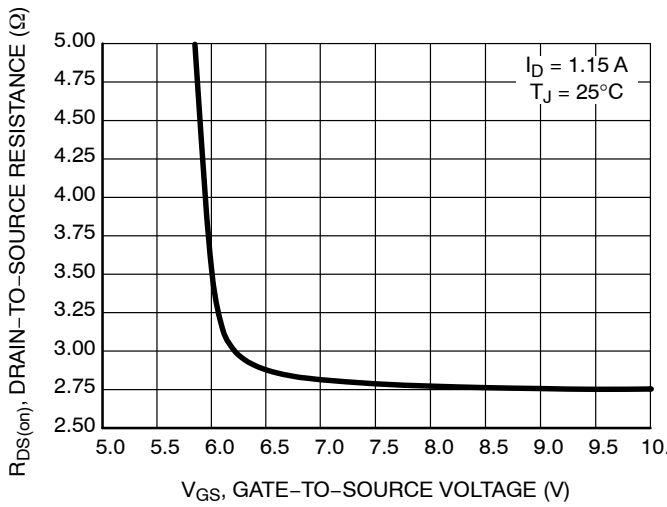


Figure 3. On-Region versus Gate-to-Source Voltage

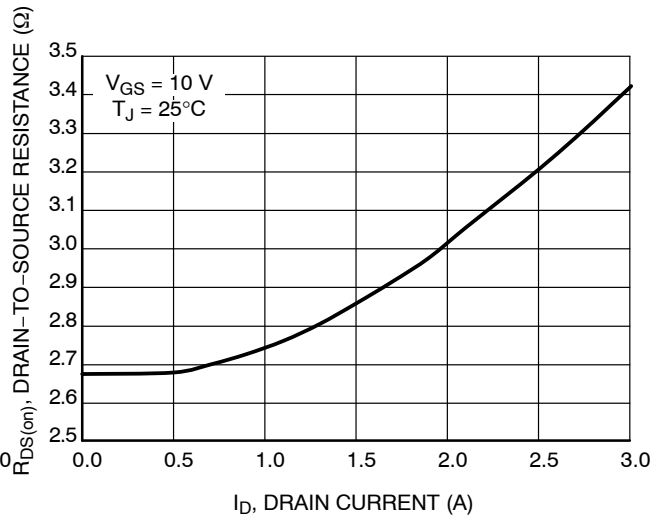


Figure 4. On-Resistance versus Drain Current and Gate Voltage

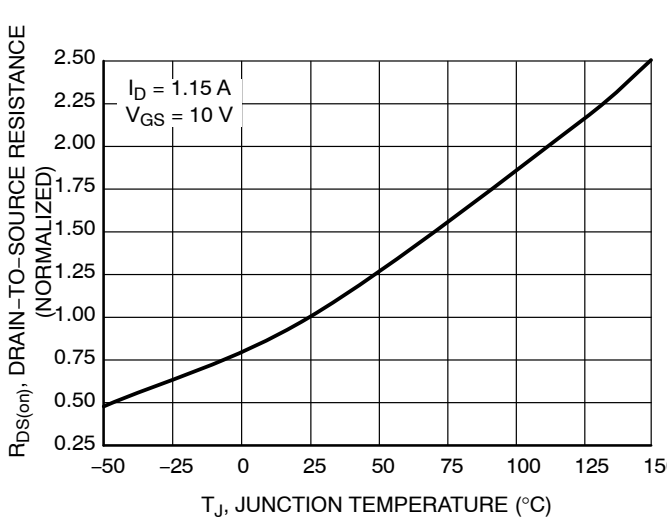


Figure 5. On-Resistance Variation with Temperature

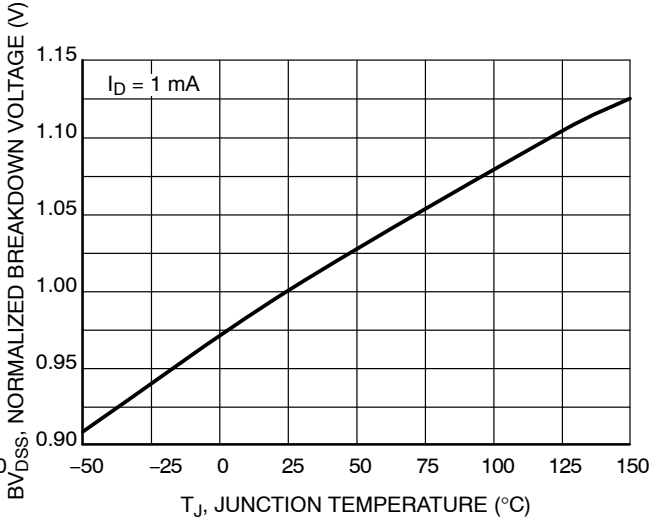


Figure 6. BV_{DSS} Variation with Temperature

NDD03N50Z

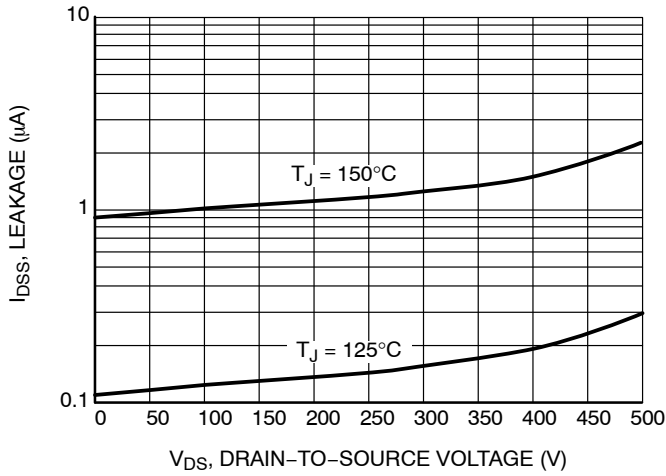


Figure 7. Drain-to-Source Leakage Current versus Voltage

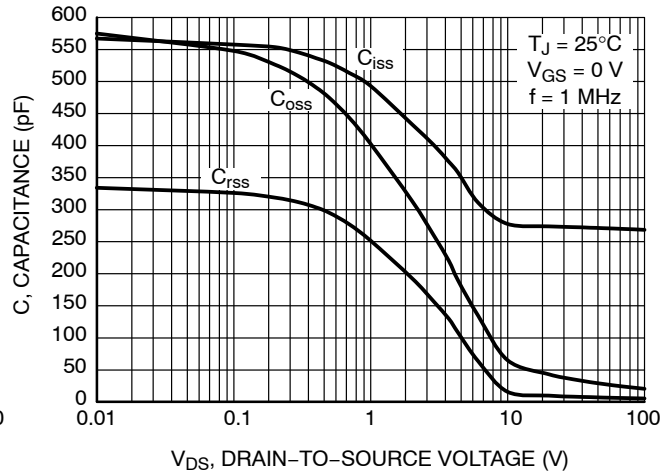


Figure 8. Capacitance Variation

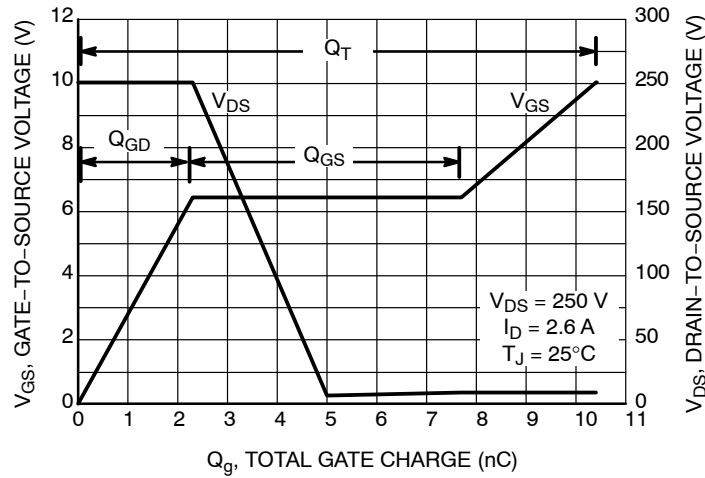


Figure 9. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

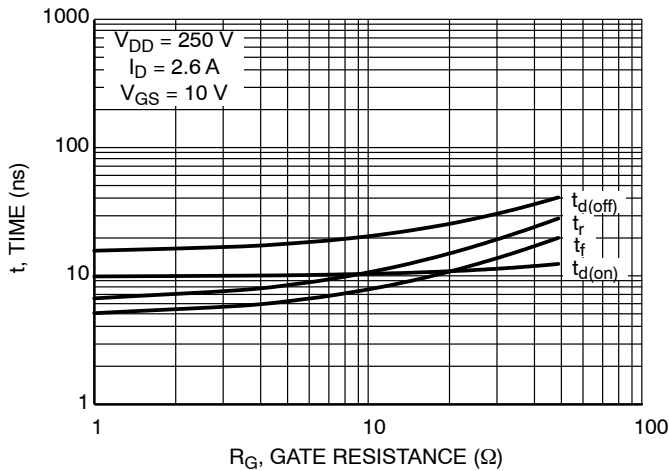


Figure 10. Resistive Switching Time Variation versus Gate Resistance

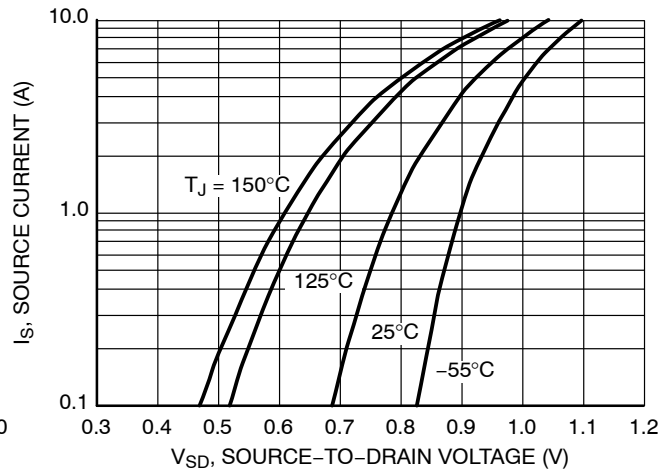


Figure 11. Diode Forward Voltage versus Current

NDD03N50Z

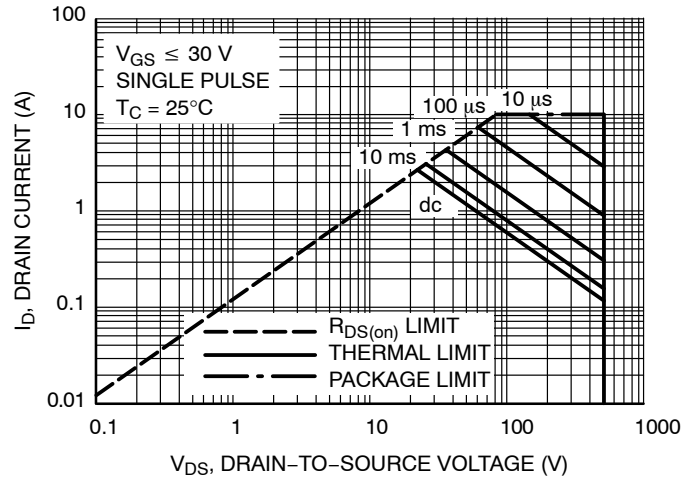


Figure 12. Maximum Rated Forward Biased Safe Operating Area NDD03N50Z

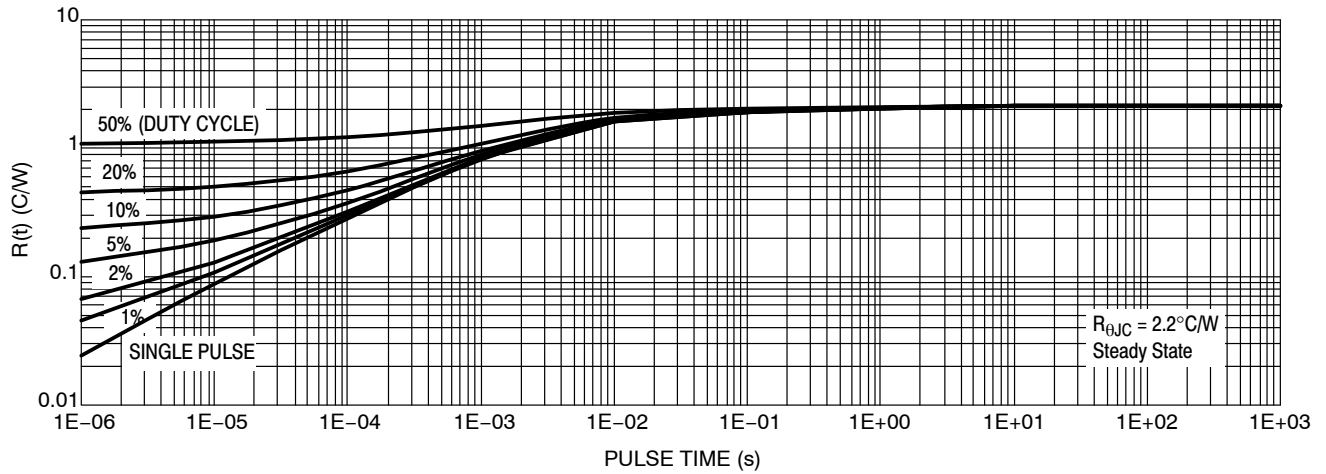


Figure 13. Thermal Impedance (Junction-to-Case) for NDD03N50Z

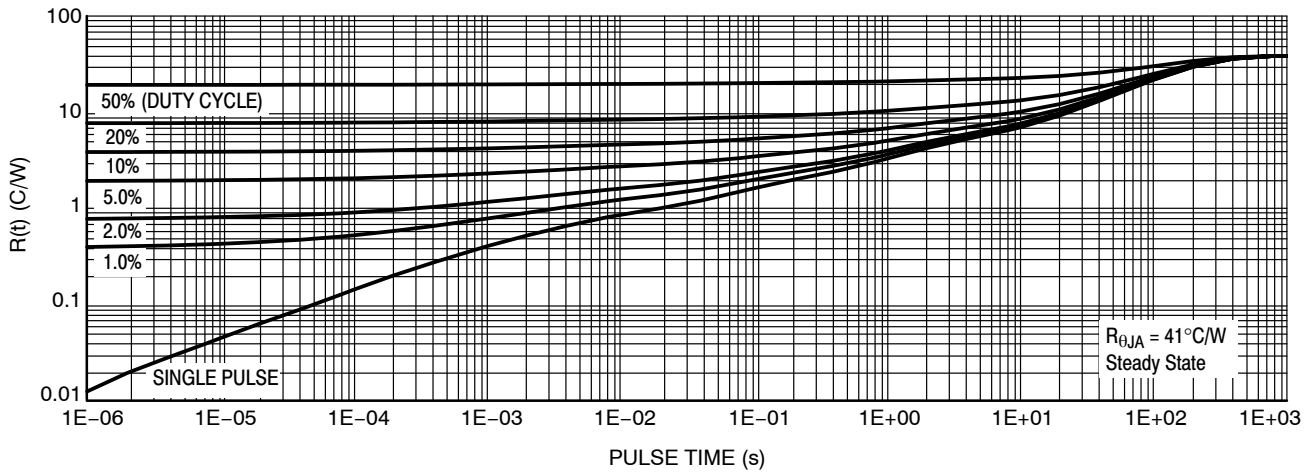


Figure 14. Thermal Impedance (Junction-to-Ambient) for NDD03N50Z

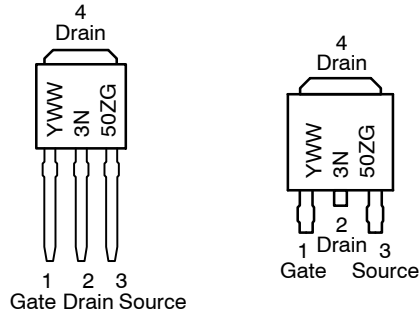
NDD03N50Z

ORDERING INFORMATION

Order Number	Package	Shipping†
NDD03N50Z-1G	IPAK (Pb-Free)	75 Units / Rail
NDD03N50ZT4G	DPAK (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

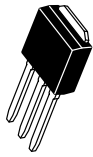


A = Location Code
 Y = Year
 WW = Work Week
 G = Pb-Free Package

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

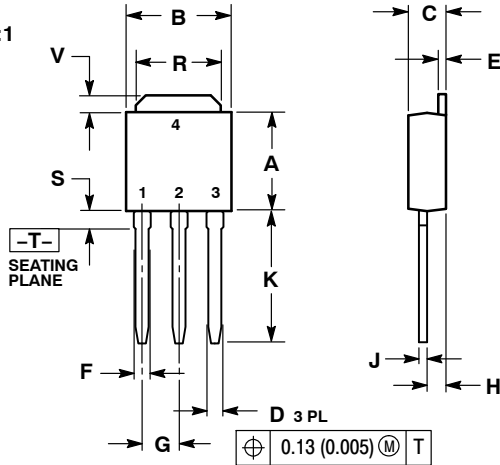
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IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010

SCALE 1:1



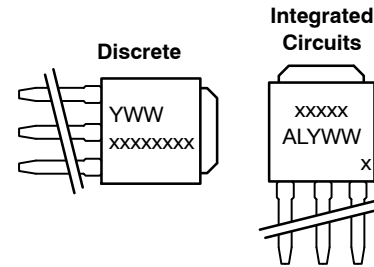
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- | | | | |
|--|---|--|--|
| <p>STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN</p> | <p>STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE</p> | <p>STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE</p> |
| <p>STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE</p> | <p>STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2</p> | <p>STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | |

MARKING DIAGRAMS



- xxxxxxxx = Device Code
- A = Assembly Location
- IL = Wafer Lot
- Y = Year
- WW = Work Week

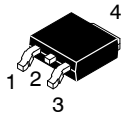
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DESCRIPTION:	IPAK (DPAK INSERTION MOUNT)	PAGE 1 OF 1

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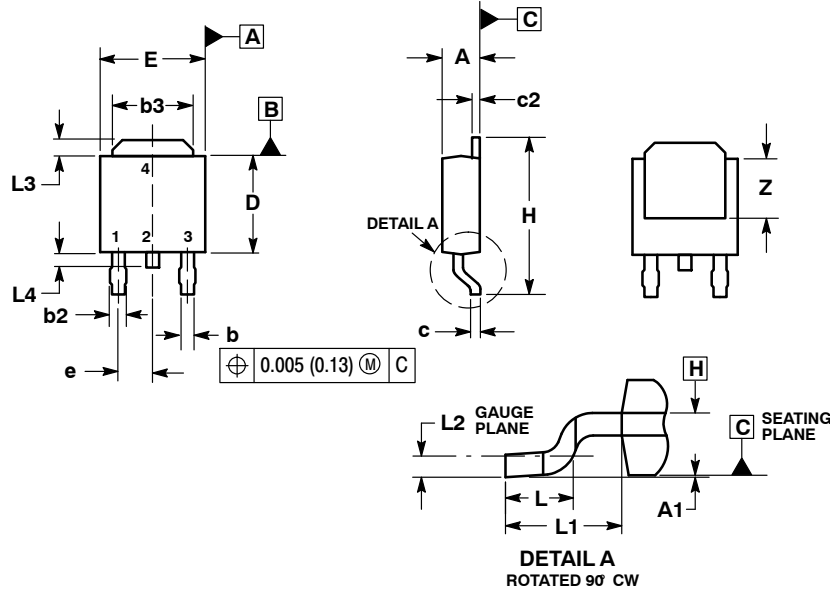
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1



DPAK (SINGLE GAUGE)

CASE 369AA-01

ISSUE B

DATE 03 JUN 2010

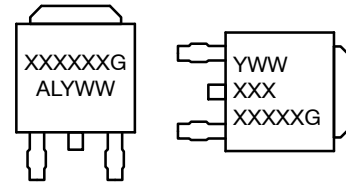
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b₃, L₃ and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b ₂	0.030	0.045	0.76	1.14
b ₃	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c ₂	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L ₁	0.108 REF		2.74 REF	
L ₂	0.020 BSC		0.51 BSC	
L ₃	0.035	0.050	0.89	1.27
L ₄	---	0.040	---	1.01
Z	0.155	---	3.93	---

- | | | | |
|--|---|--|--|
| <p>STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN</p> | <p>STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE</p> | <p>STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE</p> |
| <p>STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE</p> | <p>STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2</p> | <p>STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | |

GENERIC MARKING DIAGRAM*

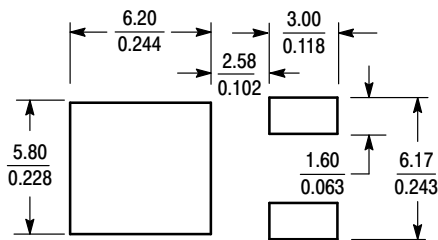


IC Discrete

- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



SCALE 3:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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